

T 6 8 3 1

C<sup>2</sup>-MOS LSI for SPEECH ANALYSIS and SYNTHESIS

The T6831 is a single chip C<sup>2</sup>-MOS LSI for SPEECH ANALYSIS and SYNTHESIS by the ADM (Adaptive Delta Modulation) method, which has an internal 64 Kbit MASK ROM for speech data. And is suitable for human voice and various sound effect.

1. FEATURES

- The T6831 has two functions, SPEECH ANALYSIS (RECORDING) and SPEECH SYNTHESIS (PLAY BACK).
- The internal 64 Kbit MASK ROM for speech data is provided. Some external memory (max. 128 Kbit) can be connected. For SPEECH ANALYSIS function, RAM is necessary as external memory. For long SPEECH SYNTHESIS, external ROM (MASK ROM or PROM) is necessary.
- The T6831 has PHRASE SELECTION function by 6 control inputs. (max. up to 61 phrases)
- 5 stage KEY BUFFERS are provided for easy editing for phrases.
- No memory is consumed by NO-SPEECH (SILENT) PHRASE.
- 4 kinds of BIT RATE (16, 11, 8, 5.5 Kbps) can be selected for each phrase.
- The T6831 has a POWER STAND-BY mode for low power consumption.
- The T6831 has a POWER ON/OFF control output for the external audio circuit.
- On-chip oscillator circuit for 32 KHz crystal is provided.
- 10 bits D/A converter (voltage type) is provided.
- Both MANUAL CONTROL and CPU CONTROL are available.
- Single power supply. (5V typ.)
- Low power consumption. 300 $\mu$ A typ. in synthesis (playing) mode, 500 $\mu$ A typ. in analysis (recording) mode without external load.

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS (Ta=25°C, except Topr and Tstg)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3 ~ +6.0	V
Input Voltage	V <sub>IN</sub>	-0.3 ~ V <sub>DD</sub> +0.3	V
Output Voltage	V <sub>OUT</sub>	-0.3 ~ V <sub>DD</sub> +0.3	V
Operating Temperature	T <sub>opr</sub>	-10 ~ +55	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +125	°C

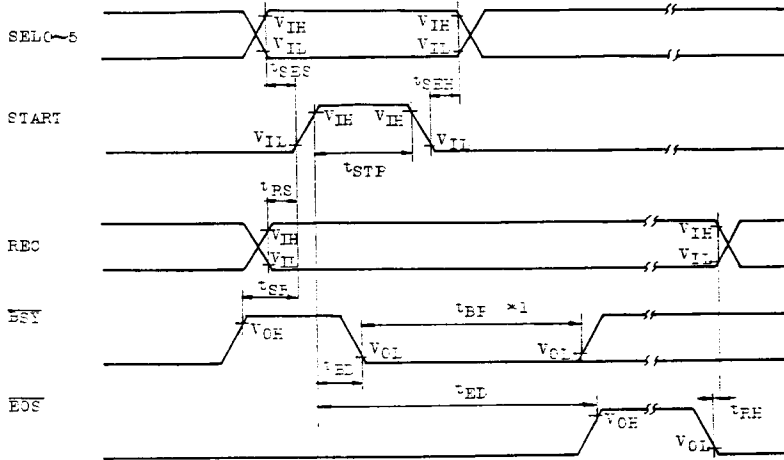
2.2 D.C. CHARACTERISTICS (GND=0V, V<sub>DD</sub>=5V, Ta=25°C, Unless otherwise noted)

CHARACTERISTICS		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage		V <sub>DD</sub>		4.5		5.7	V
Power Consumption		I <sub>DD</sub>	play mode	-	300	-	μA
			rec. mode	-	500	-	
			Stand-by mode	-	-	3	
Oscillator starting time		T <sub>sta</sub>	V <sub>DD</sub> =5V	-	3	-	sec
Input Voltage	SELO ~ SEL5, START, REC, CPUM, APDI, STBY 64K/16K	V <sub>IH</sub>		V <sub>DD</sub> -0.8	-	-	V
		V <sub>IL</sub>		-	-	0.8	
Input Current	ALL INPUTs	I <sub>IH1</sub>	V <sub>IN</sub> =V <sub>DD</sub>	-	-	1	μA
		I <sub>IL1</sub>	V <sub>IN</sub> =0V	-1	-	-	
	SELO ~ SEL5, START	I <sub>IH2</sub> *1	V <sub>IN</sub> =V <sub>DD</sub>	-	150	-	
		I <sub>IL2</sub> *1	V <sub>IN</sub> =0V	-1	-	-	
Output Voltage		V <sub>OH</sub>	without load	V <sub>DD</sub> -0.4	-	-	V
		V <sub>OL</sub>		-	-	0.4	
Output Current	EOS, BSY	I <sub>OH1</sub>	V <sub>OH</sub> =1/2V <sub>DD</sub>	-	-	-0.4	mA
		I <sub>OL1</sub>	V <sub>OL</sub> =0.4V	0.8	-	-	
	Except EOS, BSY	I <sub>OH2</sub>	V <sub>OH</sub> =V <sub>DD</sub> -0.40	-	-	-0.2	
		I <sub>OL2</sub>	V <sub>OL</sub> =0.4V	0.5	-	-	
Output Resistance	DAO	R <sub>OUT</sub>		-	50	-	kΩ
Input Resistance	ADI	R <sub>IN</sub>		-	100	-	

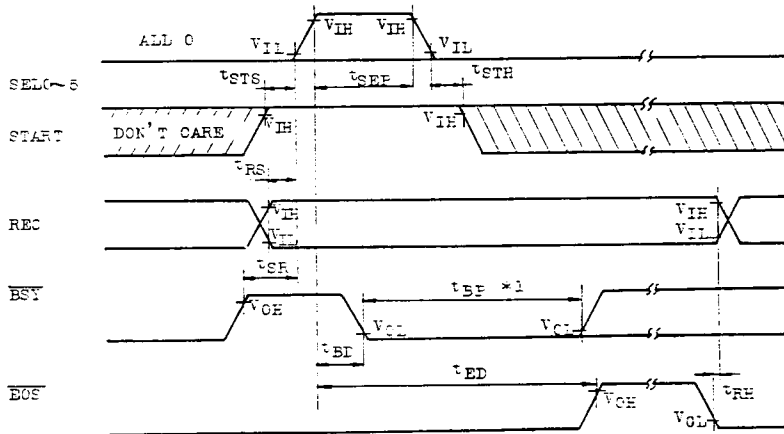
Note 1: Internal pull down resistor option.

2.3 A.C. CHARACTERISTICS ( $V_{DD}=5.0V$ ,  $C_L=15pF$ ,  $T_a=25^\circ C$ )

(1) SPEECH CYCLE 1 (at CPU MODE)



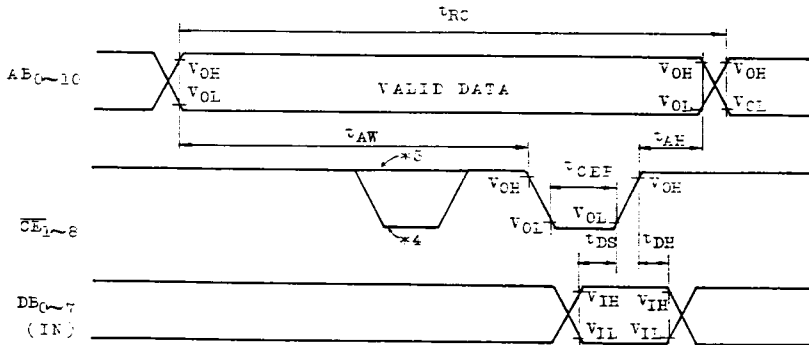
(2) SPEECH CYCLE 2 (at CPU MODE)



ITEM	SYMBOL	MIN.	MAX.	UNIT
SELECT SET UP TIME	$t_{SES}$	2	-	$\mu s$
SELECT HOLD TIME	$t_{SEH}$	2	-	$\mu s$
START PULSE WIDTH *2	$t_{STP}$	4	-	$\mu s$
START SET UP TIME	$t_{STS}$	2	-	$\mu s$
START HOLD TIME	$t_{STH}$	2	-	$\mu s$
SELECT PULSE WIDTH *2	$t_{SEP}$	4	-	$\mu s$
SPEECH RECOVERY TIME	$t_{SR}$	32	-	$\mu s$
REC SET UP TIME	$t_{RS}$	0	-	$\mu s$
REC HOLD TIME	$t_{RH}$	0	-	$\mu s$
BSY DELAY TIME	$t_{BD}$	-	2	$\mu s$
BSY PULSE WIDTH *1	$t_{BP}$	-	800	$\mu s$
EOS DELAY TIME	$t_{ED}$	-	1000	$\mu s$

- NOTE 1. Not key buffer full  
 2. At manual mode 45ms min.

(3) MEMORY READ CYCLE

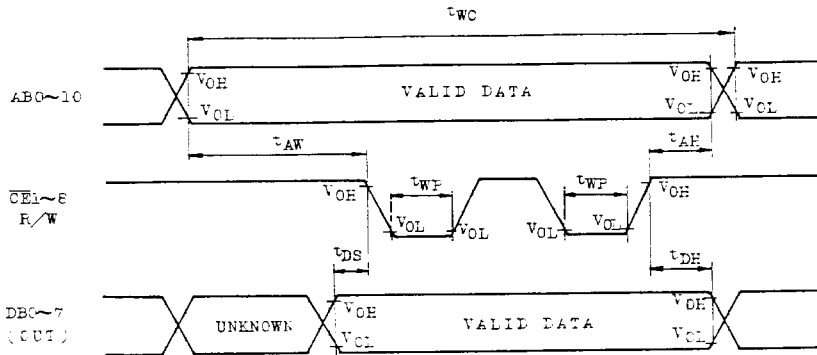


- NOTE 3. At 11 Kbps, 16 Kbps  
 4. At 5.5 Kbps, 8 Kbps

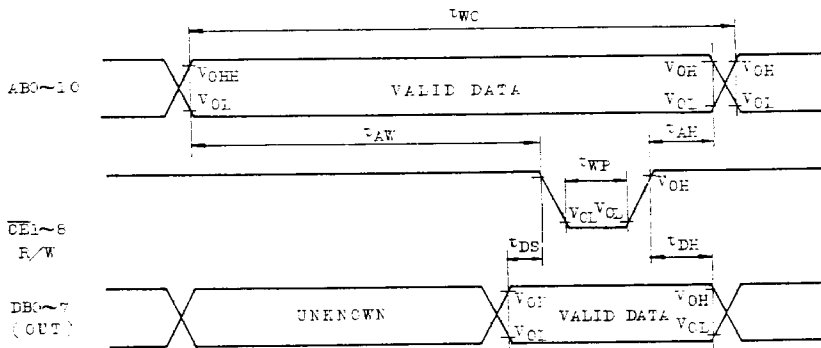
ITEM	SYMBOL	5.5Kbps	8Kbps	11Kbps	16Kbps	UNIT
READ CYCLE TIME (TYP.)	$t_{RC}$	1465(48Tc)	977(32Tc)	732(24Tc)	488(16Tc)	$\mu s$
CE PULSE WIDTH (TYP.)	$t_{CEP}$	15(0.5Tc)				$\mu s$
ADDRESS SET UP TIME(TYP.)	$t_{AW}$	1328(43.5Tc)	870(28.5Tc)	656(22.5Tc)	443(14.5Tc)	$\mu s$
ADDRESS HOLD TIME (TYP.)	$t_{AH}$	122(4Tc)	92(3Tc)	31(Tc)	31(Tc)	$\mu s$
DATA SET UP TIME (MIN.)	$t_{DS}$	2				$\mu s$
DATA HOLD TIME (MIN.)	$t_{DH}$	0				$\mu s$

$T_c=30.5\mu s$  at  $f_{XIN}=32768Hz$

(4) MEMORY WRITE CYCLE 1 (at 5.5 Kbps, 8 Kbps)



(5) MEMORY WRITE CYCLE 2 (at 11 Kbps, 16 Kbps)



ITEM	SYMBOL	5.5Kbps	8Kbps	11Kbps	16Kbps	UNIT
WRITE CYCLE TIME (TYP.)	$t_{WC}$	1465 (48T <sub>c</sub> )	977 (32T <sub>c</sub> )	732 (24T <sub>c</sub> )	488 (16T <sub>c</sub> )	μs
WRITE PULSE WIDTH(TYP.)	$t_{WP}$	15 (0.5T <sub>c</sub> )				μs
ADDRESS SET UP TIME(TYP.)	$t_{AW}$	1293 (42.5T <sub>c</sub> )	837 (27.5T <sub>c</sub> )	685 (22.5T <sub>c</sub> )	441 (14.5T <sub>c</sub> )	μs
ADDRESS HOLD TIME (TYP.)	$t_{AH}$	122 (4T <sub>c</sub> )	92 (3T <sub>c</sub> )	31 (T <sub>c</sub> )	31 (T <sub>c</sub> )	μs
DATA SET UP TIME (TYP.)	$t_{DS}$	15 (0.5T <sub>c</sub> )				μs
DATA HOLD TIME (TYP.)	$t_{DH}$	122 (4T <sub>c</sub> )	92 (3T <sub>c</sub> )	31 (T <sub>c</sub> )	31 (T <sub>c</sub> )	μs

T<sub>c</sub>=30.5μs at f<sub>XIN</sub>=3268Hz

## 3. FUNCTIONAL SPECIFICATIONS

## 3.1 GENERAL DESCRIPTION

- The internal 64 Kbit MASK ROM and the 128 Kbit external memory (RAM or ROM) can be used independently or together.
- Selection of phrases is possible with SEL 0 to SEL 5. (up to 61 phrases)
- When speech analysis (i.e. recording) function is used, the RAM is necessary as an external memory.
- 4 kinds of bit rate (16, 11, 8 and 5.5 Kbps) can be selected for each phrase.
- The T6831 has 5 stages key buffer and terminals of  $\overline{\text{ESY}}$  and  $\overline{\text{EOS}}$  for easy control by manual or CPU.

## 3.2 PIN DESCRIPTIONS

Pin No.	Symbol	Function	Note
33 } 38	SEL 0 } SEL 5	Phrase selection input terminals Possible to select max. 61 phrases. No operation mode and forced stop mode are selected by all "0" or by all "1" respectively.	input active High Note 1 Note 3
39	START	When an one shot signal is given to this terminal, the code set by the SEL 0~5 is taken in to the internal key buffers and the speech is started.	input active High Note 3
43	CPUM	Manual/CPU control selection terminal. By setting this terminal in "H" level CPU control mode selected and by "L" level manual control mode is selected.	input active High
32	$\overline{\text{ESY}}$	$\overline{\text{ESY}}$ indicates that the T6831 is executing the all clear (ACL), is accepted the forced stop instruction, is processing the data immediately after the phrase selec- tion input, or that the key buffers are full.	output active Low

## 3.2 PIN DESCRIPTIONS (Continued)

Pin No.	Symbol	Function	Note
30	$\overline{\text{EOS}}$	$\overline{\text{EOS}}$ indicates the end of speech. It is on "L" level when the speaking of all the speech data (including the data in the key buffers) is completed.	Output active Low
47	REC	Recording/Play back selection input. When the analysis (recording) mode is needed, it should be on "H" level and synthesis (play back) mode is needed, on "L" level.	input active High
46	ADI	Audio signal input (for the rec. mode) The analyzed data corresponding to the input to this terminal appear in DB0 to DB7.	input analogue
45	DAO	A synthesized audio output terminal (for the play back mode). The synthesized audio signal appears in this terminal when the synthesis function is started. This terminal is on "VDD/2" level when the synthesis function is out of use and on "GND" level during the recording or stand-by mode.	output analogue
44	$\overline{\text{ACL}}$	An all clear input. The system is initialized by setting this pin on "L" level or STBY input terminal on "H" level. It's possible to activate the auto clear function by connecting the external capacitor between this terminal and GND.	input active Low Note 2
41 42	APDI APDO	An audio circuit's power down input and output terminals. APDO is on "H" level while the APDI terminal is kept on "H" or $\overline{\text{ACL}}$ is kept on "L" to control the external audio circuit.	APDI: input active High APDO: output active High
40	STBY	A stand-by control input. By keeping it on "H", the power down mode is selected, the on-chip oscillator stops and $\overline{\text{ACL}}$ is activated.	input active High

## 3.2 PIN DESCRIPTIONS (Continued)

Pin No.	Symbol	Function	Note
1 ~ 4 53 ~ 56	DB0 } DB7	Data bus (I/O terminal) for the external memories. These are outputs of the analyzed data in the recording mode and inputs in the play back mode.	input/output active High
5 ~ 15	AB0 } AB10	Address bus for the external memories.	output active High
25	$\phi\Delta$	An output for the test signal	
16 } 23	$\overline{CE1}$ } $\overline{CE8}$	Chip enable outputs for the external memories. When the 16 Kbit memories are used, one of these terminals is set on "L" and the memory corresponding to is selected. When 64 Kbit memories are used, $\overline{CE1}$ and $\overline{CE8}$ are used for the chip enable, and $\overline{CE7}$ , $\overline{CE8}$ as AB11, AB12 respectively.	output active Low as AB11, AB12 active High
27	R/W	A read/write output for the external memories. When the T6831 reads the external memory, R/W is on "H" level and writes one, on "L" level.	output
28 29	XIN XOUT	Input and output terminal of the on-chip oscillator. A 32 KHz crystal and capacitors are connected with them.	
26	64K/16K	An external memory selection input. The 64 Kbit or 16 Kbit memory can be used by keeping it "H" or "L" level respectively.	input
48, 49 50, 51	TSN, TS1 TS2, EV	Inputs for test. These are kept on "L" by internal pull down registers. It's desirable to keep them on "L" at outside of chip for the protection from noise.	input
24, 51 52	V <sub>DD</sub> GND	Power supply terminals, V <sub>DD</sub> is +3 ~ 5V.	

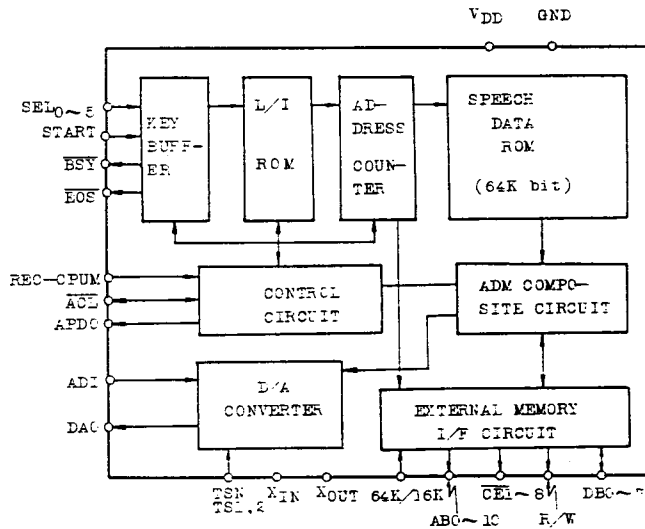
Note 1: When the manual mode is selected by keeping the CPUM on "L", the chattering protection circuit is activated for these terminals and the START input. The chattering protection time is 14 ms.

In the CPU mode, this circuit is released. The hold time of the input signal for these terminals should be set over 4 $\mu$ s.

Note 2: When the external capacitor is connected to the  $\overline{ACL}$ , this terminal is kept on "L" for about 30ms after power on or release stand-by mode.

Note 3: Possible to add internal pull down resistors.

3.3 BLOCK DIAGRAM



In the above diagram, (1) SPEECH DATA ROM and (2) L/I ROM are MASK ROM. Their contents are determined at the time of development.

(1) SPEECH DATA ROM

It stores the speech data made by the ADM analysis desired by a user. Maximum 61 speech phrases can be stored. The total speech time is 8 seconds for the standard bit rate (8 Kbps).

(2) L/I (LABEL INDEX) ROM

It stores the set of data designated by the label No. that is decided by combination of SEL0 ~ SEL5 except 0, 3E and 3F (HEX). The set of data which can be designated are shown below.

- The start address and the end address of the memory area corresponding to the speech phrase.
- The bit rate of the each speech phrase.
- The internal/external memory selection.
- The speech/no-speech phrase selection.

Note: When no-speech phrase is selected the DAO terminal is kept on "V<sub>DD</sub>/2" level without the speech data memory. So it is effective to set the interval between the phrases.

#### 4. SYSTEM CONSTRUCTION

Two system constructions are available, a CPU control type and a manual control type.

##### 4.1 CPU control type

This system consists basically of two chips of a CPU and the T6831. However, if an analysis function is required, an external RAM (max. 128 Kbits) must be connected.

Further, it is possible to make the total speech time longer by connecting the system with general purpose MASK-ROM or PROM (max. 128 Kbit) in place of RAM.

ROM and RAM can be used together for the external memory.  
 In this case the total memory size of them is also max. 128 Kbits.  
 In Fig.4.1 connection diagram, the basic operation is divided into the following two ways:

- (1) CPU → T6831

CPU sets the input signals STBY, APDI, REC, START and SEL0 to SEL5.

- (2) CPU ← T6831

The T6831 sends the  $\overline{EOS}$  and  $\overline{BSY}$  signal to the CPU. The  $\overline{EOS}$  (End Of Speech) goes to "L" level when all of the speeches (contents of key buffer) come to an end, and it indicates the end of the speech to the CPU. The  $\overline{BSY}$  indicates the period that the T6831 can not be controlled by the CPU. If a control signal is set from the CPU to the T6831, in this period ( $\overline{BSY}$  is on "L"), the T6831 does not accept and performs uncertain operation.

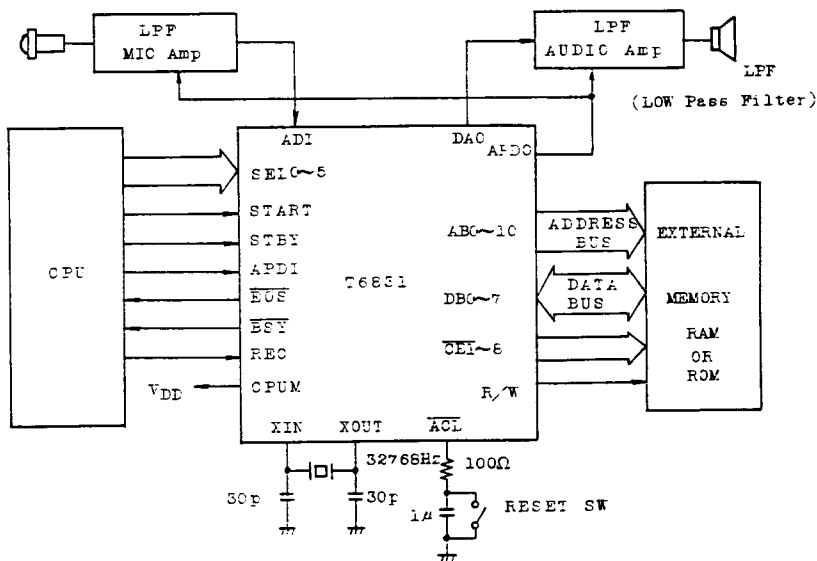
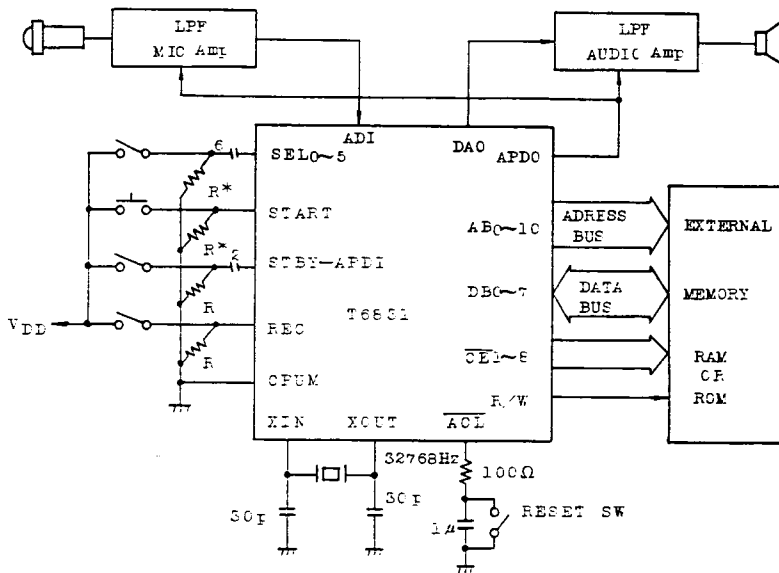


Fig.4.1 Connection diagram

4.2 Manual control type

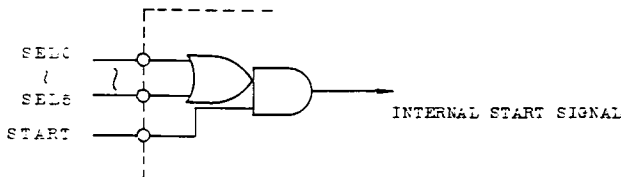
The system comprises the T6831 only or with the external memory (RAM or ROM).



Note: If it's selected internal pull down option, these resistors can be removed.

Fig. 4.2

In manual operation, set up the conditions for STBY, APDI, REC, etc., select phrases by means of SELO to SEL5, and turn on START SW. It's possible to turn on START SW before or after selecting phrases. (See A.C. characteristics)  
 The internal circuit of the START and SELO - SEL5 input terminals are shown below.



APPENDIX A

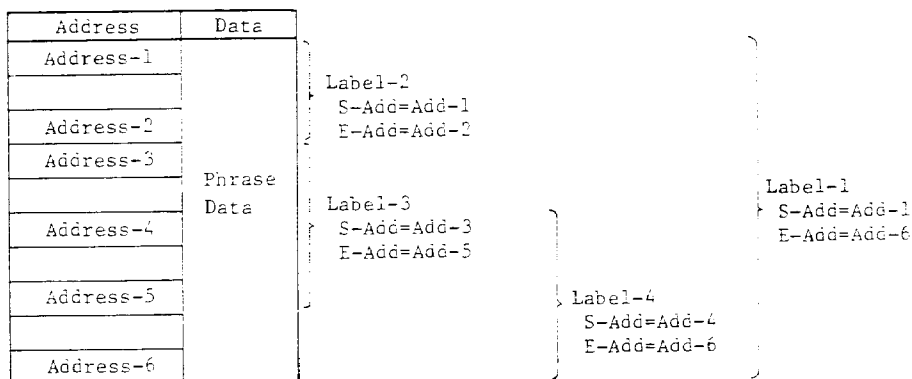
Examples of the use of L/I ROM

"Label" is a name given to each phrase. Labeled phrases are distinguished by code decided by 6 inputs (SEL0 ~ SEL5).

To put it concretely a set of start address and end address of memory, bit rate, selection of internal/external memory and selection of speech/no-speech phrase can be designated for each labeled phrase.

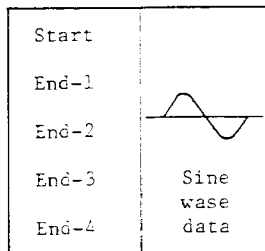
Example 1

The same data stored in the memory can be used for over two labeled phrases.



Multi labeling by different START/END address

Example 2

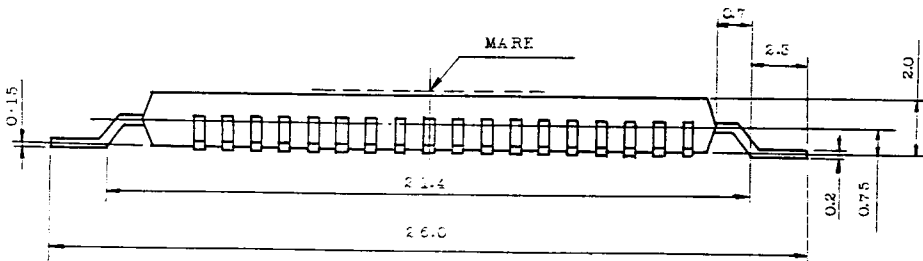
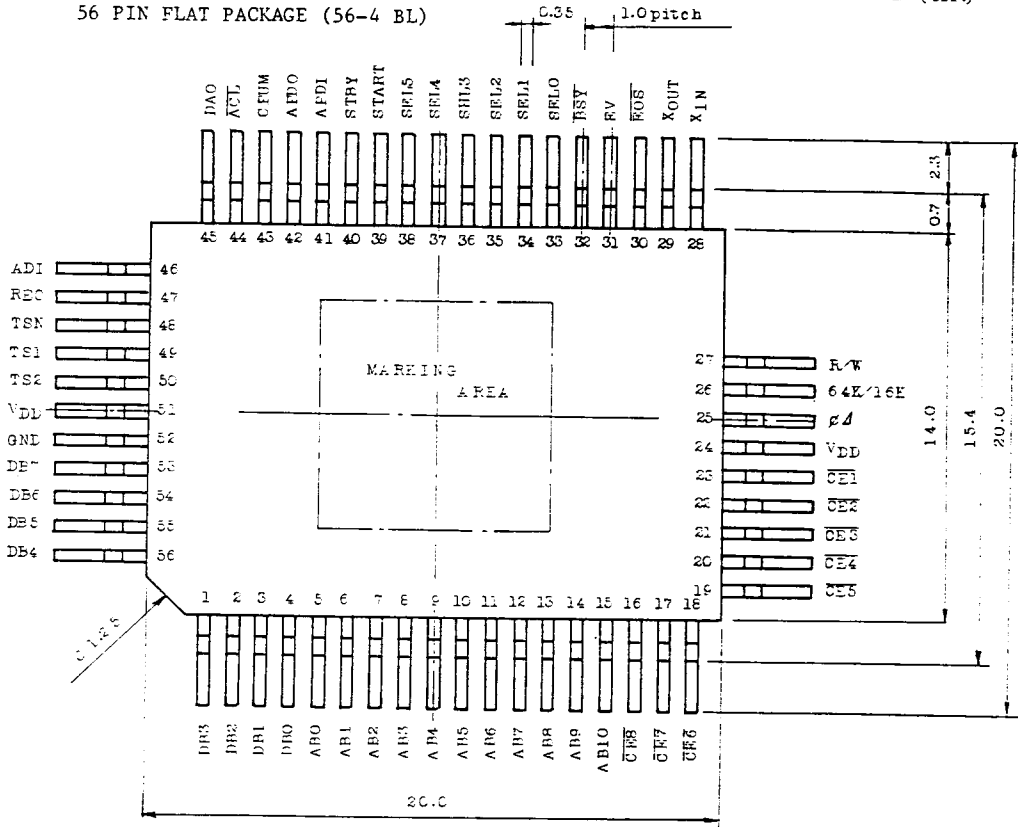


- (1) It's possible to make different length notes (half-note, quarter-note, etc.) with the same bit rate.
- (2) It's possible to make different pitch (440Hz, 880Hz, etc.) with the different bit rate.

#### APPENDIX B PACKAGE OUTLINE

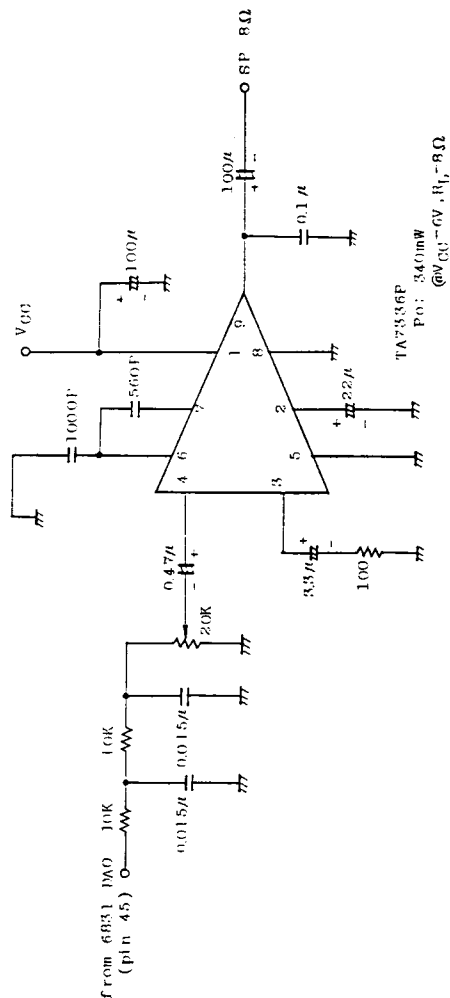
56 PIN FLAT PACKAGE (56-4 BL)

Unit in mm (TYP.)



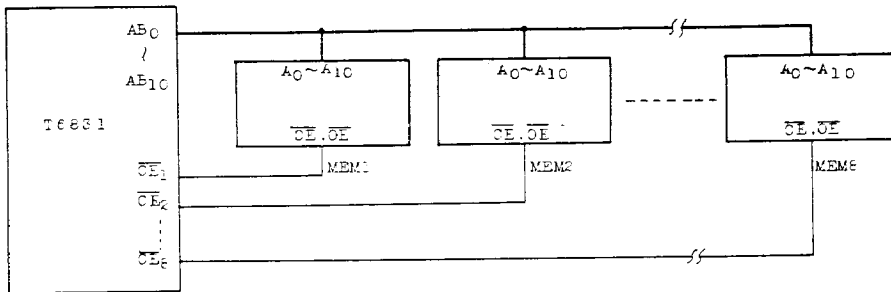


RECOMMENDED AUDIO CIRCUIT  
for PLAY BACK Amp. (tentative)

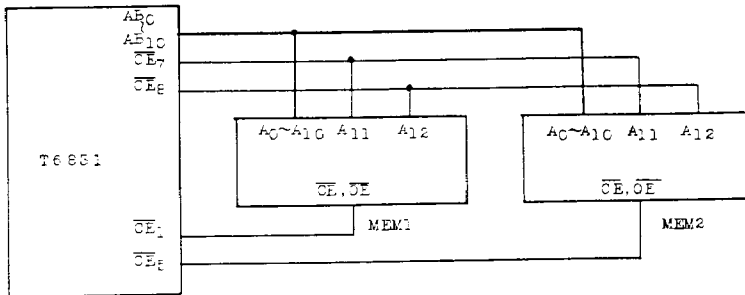


APPENDIX D APPLICATION OF EXTERNAL MEMORY

1. 16Kbit memory (TMM323D or TC5516 total 8 chips max.)



2. 64Kbit memory (TMM2764D or TC5564/TC5565 total 2 chips max.)



NOTE (1) In above figure, the  $\overline{CE}$  and  $\overline{OE}$  of MEM<sub>n</sub> mean the followings.

$\overline{CS}$ , PD/PGM	TMM323D
$\overline{CE}_1$ , $\overline{CE}_2$	TC5516
$\overline{CE}$ , $\overline{OE}$	TMM2764D
$\overline{CE}_1$ , $\overline{OE}$	TC5564/65

The  $\overline{CE}_2$  of the TC5564/65 must be connected with VDD.