

# HD64520F

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## ISDN S-Interface LSI

An S-interface LSI is an LSI that implements ISDN basic user network interface layer 1 control that conforms to the ITU-T I.430 recommendation. This S-interface LSI incorporates drivers and receivers on chip and provides a rich set of additional functions, including B channel selection, loopback testing, and multiframe support. The HD64520F is a low-power LSI that supports phantom power supply (local power supply) operation.

This LSI can be directly connected to an LAPD controller (HD64530), an LAPB controller (HD64540) and a link layer controller (HD64541), which are layer 2 control LSIs, to form a system that implements layer 1 and layer 2 control functions conforming to the ITU-T I.430 and I.441 recommendations.

### Features

- Layer 1 control functions conforming to the ITU-T I.430 recommendations
  - 192 kbps transfer speed
  - Two B plus one D channel organization
  - Synchronization control (timing recovery, frame synchronization)
  - Multiframe control using Q bits
  - E bit (D echo channel bit) output function
  - NT/TE mode operation

Selection between two B channel usage modes (B1/B2 separate usage mode (64 kbps) or B1 + B2 bulk mode (128 kbps))

Selection between internal or external clock synchronization for B channel data I/O

Incoming call detection function

- B channel selection function

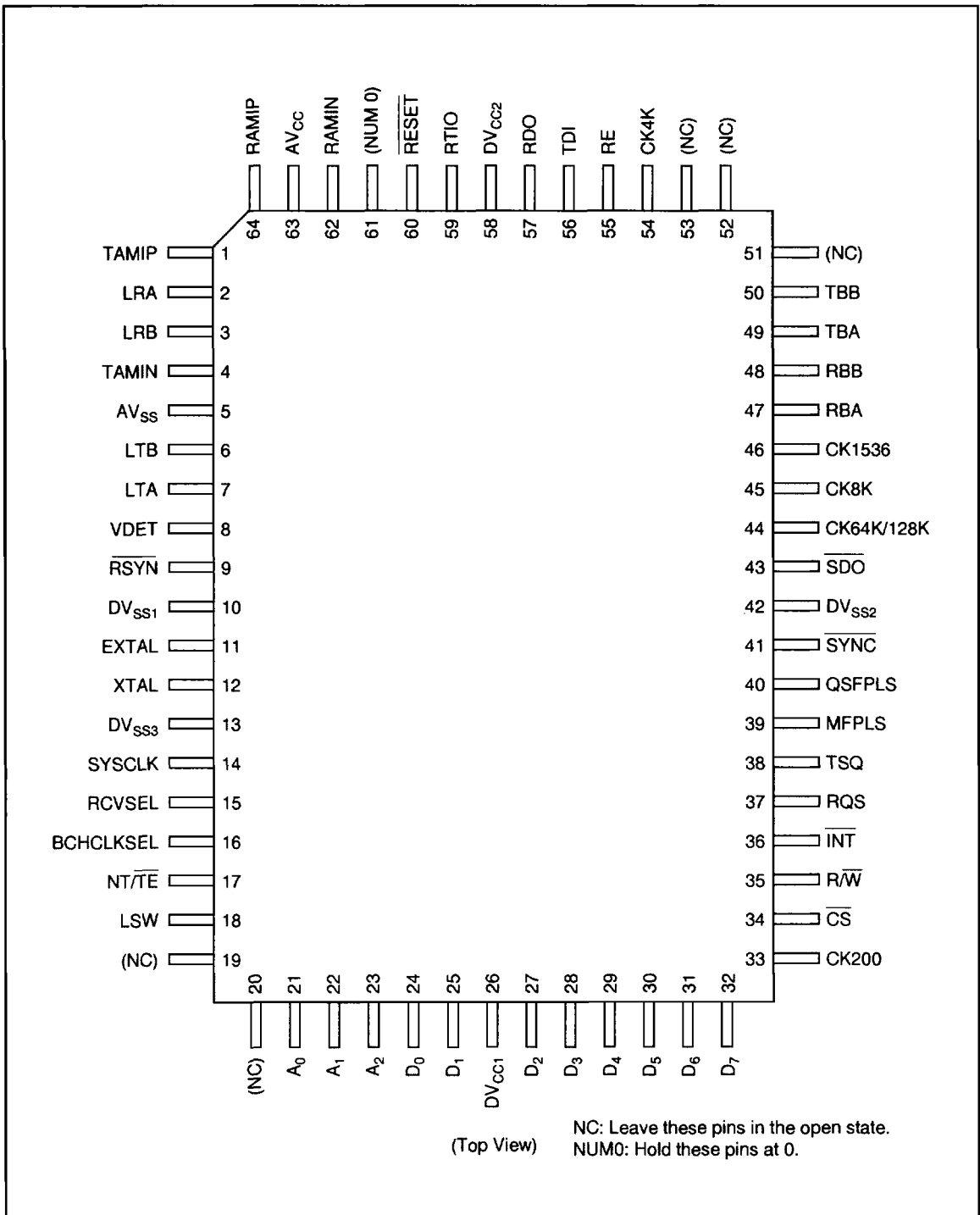
Allows internal switching of the B1 and B2 I/O pins.

- Transmit frame external synchronization mode
- Loopback test function
- Forced INFO1 to INFO4 output function
- Built-in driver/receiver circuits
- Selection of logic block independent mode or driver/receiver independent mode.
- Low power mode (internal low power mode)

Supports phantom power supply (local power supply) operation.

- Built-in crystal oscillator circuit
- TTL and CMOS compatible I/O
- Single-voltage +5 V  $\pm 5\%$  power supply operation
- Package: 64-pin plastic QFP (FP-64B)

Pin Arrangement





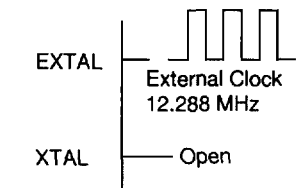
**Pin Functions**

**Power Supply**

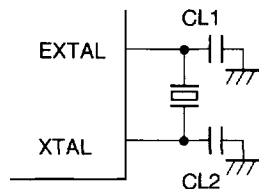
Symbol	Pin No. (QFP)	Function	I/O	Functional description
DV <sub>CC1,2</sub>	26, 58	Digital power supply	Input	Connect to the digital system power supply (+5 V ±5%).
AV <sub>CC</sub>	63	Analog power supply	Input	Connect to the analog system power supply (+5 V ±5%).
DV <sub>SS1,2,3</sub>	10, 42, 13	Digital ground	Input	Connect to the digital system ground.
AV <sub>SS</sub>	5	Analog ground	Input	Connect to the analog system ground.

**Clock**

Symbol	Pin No. (QFP)	Function	I/O	Functional description
XTAL	12	Crystal oscillator connections	Output	Connect a 12.288 MHz crystal oscillator.
EXTAL	11	Crystal oscillator connections	Input	Connect a 12.288 MHz crystal oscillator. Alternatively, an external clock signal may be input to this pin.



(A) External Input Mode



(B) X'tal Mode

Oscillator Frequency:  
12.288 MHz  
Rf = 1 M to 10 MΩ  
Cl, CO: 22 to 30 pF

SYSCLK	14	System clock	Output	Supplies the system clock (6.144 MHz) to peripheral devices. Note that this pin outputs a low level in clock stop mode.
CK1536	46	1.536 MHz clock	I/O	Inputs the 1.536 MHz transmit side reference clock in NT mode. Outputs the 1.536 MHz internally generated clock in TE mode.
RTIO	59	D channel data transmit timing clock	Output	Outputs a 16 kHz signal. The duty will not be 50%.
CK8K	45	B channel frame timing	I/O	Inputs and outputs the frame timing generation signal for the TBA and TBB input and the RBA and DBB output signals. This clock does not stop in output mode, even on a reset.

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### Clock (cont)

Symbol	Pin No. (QFP)	Function	I/O	Functional description
CK64K/128K	44	B channel bit timing	I/O	Inputs and outputs the bit timing generation signal for the TBA and TBB input and the RBA and RBB output signals. This clock does not stop in output mode, even on a reset. The 64 kHz and 128 kHz systems are switched by the bulk set bit in the B channel selection register (04H). B1/B2 separate usage mode: 64 kHz clock B1 + B2 bulk mode: 128 kHz clock
CK200	33	200 Hz clock	Input	In transmit frame external synchronization mode (when bit 3 (TXSEL) in the mode set register (MSR) is 1), the beginning of each multiframe is sent in synchronization with the rising edge of this clock.
CK4K	54	4 kHz clock	Input	In transmit frame external synchronization mode (when bit 3 (TXSEL) in the mode set register (MSR) is 1), the beginning of each transmit circuit frame is sent in synchronization with the rising edge of this clock.

### System Interface

Symbol	Pin No. (QFP)	Function	I/O	Functional description
$\overline{\text{RESET}}$	60	Reset	Input	The HD64520F is reset when a low level is applied to this pin. This pin is a Schmitt input.
$\overline{\text{R/W}}$	35	Read/write	Input	This pin is valid when $\overline{\text{CS}}$ is low. Data read from the internal registers is enabled when this pin is high, and data write is enabled when this pin is low.
$\overline{\text{INT}}$	36	Interrupt request output	Output	This pin goes low when any bit in the interrupt source register is set to 1. However, if the bit corresponding to the interrupt in the interrupt mask register is set to 1, this pin will remain high. This pin is an open drain output.
$\overline{\text{CS}}$	34	Chip select	Input	Setting this pin low allows external systems to read or write the HD64520F internal registers.

**Address Bus**

Symbol	Pin No. (QFP)	Function	I/O	Functional description
A <sub>0</sub> to A <sub>2</sub>	21 to 23	Address bus	Input	Address pins used to select one of the six internal registers.

**Data Bus**

Symbol	Pin No. (QFP)	Function	I/O	Functional description
D <sub>0</sub> to D <sub>7</sub>	24, 25, 27 to 32	Data bus	I/O	Eight bit bidirectional bus. Used to read from and write to the internal registers.

**Mode Selection**

Symbol	Pin No. (QFP)	Function	I/O	Functional description												
RCVSEL	15	Reception timing selection	Input	In NT mode this pin selects the received AMI signal reception timing as follows: Low-level input: Reception synchronization mode. Receive side operation based on a clock phase synchronized to the received AMI signal by the DPLL circuit. High-level input: Transmit synchronization mode. Receive side operation with timing synchronized to a 192 kHz signal divided from the transmit side 1.536 MHz reference clock. Input a low level in TE mode. The mode set register (MSR) bit 5 (RCVSEL) must be held at 0 when switching this setting with this pin.												
BCH CLK SEL	16	B channel clock selection	Input	The input/output modes of the CK8K and CK64K/128K pins are switched at the same time. Note that the mode set register (MSR) bit 6 (Bch CLK SEL) must be held at 0 when switching this setting with this pin.												
				<table border="1"> <thead> <tr> <th></th> <th>Synchronization clock</th> <th>CK64K/CK8K</th> <th>128K</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Internal oscillator clock</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>High</td> <td>External input clock</td> <td>Input</td> <td>Input</td> </tr> </tbody> </table>		Synchronization clock	CK64K/CK8K	128K	Low	Internal oscillator clock	Output	Output	High	External input clock	Input	Input
	Synchronization clock	CK64K/CK8K	128K													
Low	Internal oscillator clock	Output	Output													
High	External input clock	Input	Input													

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### Mode Selection (cont)

Symbol	Pin No. (QFP)	Function	I/O	Functional description
NT/ $\overline{TE}$	17	NT/TE mode selection	Input	On a low level input, the HD64520F operates in TE mode. On a high level, the LSI operates in NT mode. Note that the mode set register (MSR) bit 7 (NT/TE) must be held at 0 when switching this setting with this pin.

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### Circuit Interface

Symbol	Pin No. (QFP)	Function	I/O	Functional description
LRA, LRB	2, 3	Circuit receive side pins A and B	Input	The received circuit AMI signal is input to the LRA and LRB pins. Either input polarity may be used, regardless of the received circuit AMI signal polarity. The bit rate is 192 kbps.
LTA, LTB	7, 6	Circuit transmit side pins A and B	Output	The transmitted circuit AMI signal is output from the LTA and LTB pins. The LTA pin corresponds to the positive polarity side of the transmitted circuit AMI signal, and the LTB corresponds to the negative side. The bit rate is 192 kbps.
RAMIN, RAMIP	62, 64	Received AMI positive/negative	I/O	Digital output for the signal after reception of the received circuit AMI signal by the receiver circuit in normal operating mode or in receiver/driver independent mode. These pins are used as the digital input for the received AMI signal in logic block independent mode.
TAMIP, TAMIN	1, 4	Transmitted AMI positive/negative	I/O	Digital output for the transmitted AMI signal in normal operating mode or in logic block independent mode. These pins are used as the digital input for the driver circuit that outputs the transmitted circuit AMI signal in receiver/driver independent mode.

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Layer 2 Interface

Symbol	Pin No. (QFP)	Function	I/O	Functional description															
RDO	57	Receive side D channel data output	Output	Receive side D channel output (for data preceding HDLC format decomposition). Data output is synchronized with the RTIO timing.															
TDI	56	Transmit side D channel data input	Input	Transmit side D channel data input (for data following HDLC format assembly). Data input is synchronized with the RTIO timing.															
RE	55	Receive side echo bit output	Output	Outputs the receive side echo bit. Data output is synchronized with the RTIO timing.															
TBA, TBB	49, 50	Transmit side B channel data input A and B	Input	<p>These pins can be set up for B1 channel or B2 channel input using the B channel selection register (04H) B1Enable, B2Enable, and EXChange bits. A binary 1 is output on the corresponding channel on the circuit when disabled. The pins are assigned as follows after a reset:</p> <p>TBA ... Transmit side B1 channel data input  TBB ... Transmit side B2 channel data input</p> <p>Bulk mode is set with the bulk set bit in the B channel selection register (04H). The pins have the following functions in bulk mode.</p> <table border="1"> <thead> <tr> <th>Pin</th> <th>Mode</th> <th>Bulk mode</th> </tr> </thead> <tbody> <tr> <td>RBA*</td> <td>Receive side</td> <td>Receive side B1 + B2 output</td> </tr> <tr> <td>RBB</td> <td>B1 output/ receive side B2 output</td> <td></td> </tr> <tr> <td>TBA*</td> <td>Transmit side</td> <td>Transmit side B1 + B2 input</td> </tr> <tr> <td>TBB</td> <td>B1 input/ transmit side B1 input</td> <td></td> </tr> </tbody> </table> <p>CK8K 8 kHz clock 8 kHz clock  CK64K/ 64 kHz clock 128 kHz clock  128K</p> <p>Bit rate 64 kbps, 2 channels 128 kbps, 1 channel</p> <p>Note: Channel allocation of the RBA, RBB, TBA, and TBB pins is controlled by the B channel selection register.</p>	Pin	Mode	Bulk mode	RBA*	Receive side	Receive side B1 + B2 output	RBB	B1 output/ receive side B2 output		TBA*	Transmit side	Transmit side B1 + B2 input	TBB	B1 input/ transmit side B1 input	
Pin	Mode	Bulk mode																	
RBA*	Receive side	Receive side B1 + B2 output																	
RBB	B1 output/ receive side B2 output																		
TBA*	Transmit side	Transmit side B1 + B2 input																	
TBB	B1 input/ transmit side B1 input																		

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## Layer 2 Interface (cont)

Symbol	Pin No. (QFP)	Function	I/O	Functional description
RBA, RBB	47, 48	Receive side B channel data output	Output	These pins can be set up for one of three modes, B1 channel output, B2 channel output, or a binary 1 output (when disabled), using the B channel selection register (04H) B1Enable, B2Enable, and EXChange bits. The pins are assigned as follows after a reset: RBA ... Receive side B1 channel data output RBB ... Receive side B2 channel data output
RQS	37	Receive side Q bit/ S bit data output	Output	Outputs the receive side Q bit in NT mode and the receive side S bit in TE mode.
TSQ	38	Transmit side S bit/ Q bit data input	Input	Inputs the transmit side S bit in NT mode and the transmit side Q bit in TE mode.

## Layer 1 Control

Symbol	Pin No. (QFP)	Function	I/O	Functional description
VDET	8	Voltage detection	Input	Voltage detection input. The LSI detects power when a high level is input. The LSI transmits a layer 1 INFO0 signal when a voltage is not detected. This pin is a Schmitt input.
LSW	18	Layer 1 start	Input	Layer 1 start signal input. Layer 1 is started when a high level is input. In NT mode, layer 1 is stopped when a low level is input to this pin. Note that a 1 must be written to the status command register (SCR) bit 2 (LSW) if this pin is to be used to start and stop layer 1.
RSYN	9	Reception synchronization established signal output	Output	Outputs the receive side frame synchronization established signal. In compliance with the ITU-T I.430 recommendations, this pin outputs a low level when frame synchronization is established. In NT mode there are 3 anterior stages and 3 posterior stages. In TE mode there are 2 anterior stages and 3 posterior stages. This does not depend on the received A bit.

Layer 1 Control (cont)

Symbol	Pin No. (QFP)	Function	I/O	Functional description
SYNC	41	Synchronization established signal output	Output	Outputs the receive side frame synchronization established signal. Outputs the same signal as the $\overline{\text{RSYN}}$ pin in NT mode. In TE mode, output starts when three consecutive A bits with a value of 1 are detected after $\overline{\text{RSYN}}$ goes low. $\overline{\text{INFO2}}$ is reported by $\overline{\text{RSYN}} = \text{low}$ and $\overline{\text{SYNC}} = \text{high}$ , and $\overline{\text{INFO4}}$ is reported by $\overline{\text{RSYN}} = \text{low}$ and $\overline{\text{SYNC}} = \text{low}$ .
$\overline{\text{SDO}}$	43	Call detection signal output	Output	Outputs a low level when the received AMI signal is detected. This pin goes high to report the absence of a received signal when the no input state continues for over 1.75 to 2.00 ms. This pin goes high in clock stop mode. It outputs a low level immediately following a reset.
MFPLS	39	M bit frame pulse	Output	The output changes state in response to a frame with an M bit with the value 1. The high level periods in this signal correspond to periods between a Q1/S1 frame and a Q4/S4 frame (frames with the M bit = 1).
QSFPLS	40	Q bit/S bit frame pulse	Output	Outputs a high level for all frames from Q1/S1 through Q4/S4.

Other

Symbol	Pin No. (QFP)	Function	I/O	Functional description
(NC)	19, 20, 51, 52, 53	User unused (open)	—	Make no connections to these pins.
(NUM 0)	61	User unused (hold at 0)	—	Hold this pin at the logic 0 level.

## Internal Registers

**Table 1 Internal Registers**

Address	Register	Abbreviation	R/W	Initial value
00H	Mode set register	MSR	R/W	00H <sup>1</sup>
01H	Interrupt source register	ISR	R	04H <sup>2</sup>
02H	Interrupt mask register	IMR	R/W	FFH
03H	Status command register	SCR	R	05H <sup>3</sup>
			W	00H
04H	B channel selection register	BCHSLR	R/W	0CH
05H	Test function register	TFR	R/W	03H

- Notes: 1. The corresponding bit is set to 1 when a high level input occurs on the NT/ $\overline{TE}$  pin, the BCH CLK SEL pin, or the RCV SEL input pin.  
 2. The initial value will be 06H if the VEDT pin is high.  
 3. The initial value will be 07H if the VEDT pin is high.

## Register Functions

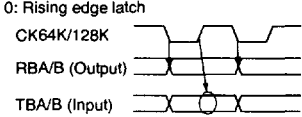
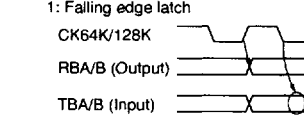
### 1. Mode Set Register (MSR)

This register sets the operating mode.

Bit:	7	6	5	4	3	2	1	0
Symbols:	NT/TE	Bch CLK SEL	RCV SEL	RESEL	TXSEL	MFSEL	BAch SEL	Dch SEL
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Function	Functional description												
7	NT mode/ TE mode switching	Switches between NT mode and TE mode. 0: TE mode; 1: NT mode Note that the NT/ $\overline{TE}$ pin must be held low is this bit is used. When the NT/TE pin is high, this bit will be 1 on read regardless of its set value.												
6	B channel clock selection	Selects the B channel data I/O clock. The I/O modes of the CK8K and CK64K/CK128K pins are switched at the same time. The initial value is 0. Note that the BCH CLK SEL pin must be held low is this bit is used. When the BCH CLK SEL pin is high, this bit will be 1 on read regardless of its set value.												
		<table border="1"> <thead> <tr> <th>Input</th> <th>Synchronization clock</th> <th>CK8K</th> <th>CK64K/128K</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Internal oscillator clock</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>1</td> <td>External input clock</td> <td>Input</td> <td>Input</td> </tr> </tbody> </table>	Input	Synchronization clock	CK8K	CK64K/128K	0	Internal oscillator clock	Output	Output	1	External input clock	Input	Input
Input	Synchronization clock	CK8K	CK64K/128K											
0	Internal oscillator clock	Output	Output											
1	External input clock	Input	Input											

1. Mode Set Register (MSR) (cont)

Bit	Function	Functional description
5	Circuit reception timing selection	<p>In NT mode, selects the circuit receive side signal reception timing as follows:</p> <p>0: Reception synchronization mode. Receive side operation using a clock phase synchronized by the DPLL circuit to the circuit receive side signal.</p> <p>1: Transmit synchronization mode. Receive side operation using timing synchronized with a 192 kHz signal divided from the transmit side reference clock (1.536 MHz).</p> <p>This bit must be set to 0 in TE mode.</p> <p>Note that the RCVSEL pin must be held low is this bit is used.</p> <p>When the RCVSEL pin is high, this bit will be 1 on read regardless of its set value.</p>
4	Echo bit reception timing selection	<p>Selects the D channel clock timing when the echo bit (RE) is used by the layer 2 LSI.</p> <p>0: Normal mode.</p> <p>1: LAPD controller (HD64530) dedicated mode.</p>
3	Transmit frame external synchronization selection	<p>0: Internal timing synchronization mode</p> <p>1: External timing synchronization mode (synchronization with the 4 kHz and 200 Hz clocks)</p>
2	Multiframe control method selection	<p>0: Q/S bit transmission is performed by reading to and writing from the status command register (SCR) bits 4 to 7 (Q1/S1 to Q4/S4 on read, S1/Q1 to S4/Q4 on write).</p> <p>1: Q/S bit transmission is performed using the TSQ input and RQS output pins.</p>
1	B channel data latch timing selection	<p>Selects the data and clock timing for the BA channel (RBA and TBA) and the BB channel (RBB and TBB) as follows:</p> <div style="display: flex; justify-content: space-around;"> <div style="width: 45%;"> <p>0: Rising edge latch</p> <p>CK64K/128K </p> <p>RBA/B (Output)</p> <p>TBA/B (Input)</p> </div> <div style="width: 45%;"> <p>1: Falling edge latch</p> <p>CK64K/128K </p> <p>RBA/B (Output)</p> <p>TBA/B (Input)</p> </div> </div>
0	D channel data latch timing selection	<p>Selects the data and clock timing for the D channel (RDO and TDI) in the same manner as the B channel data latch timing selection bit.</p>

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## 2. Interrupt Source Register (ISR)

This register indicates the interrupt requested. A value of 1 indicates that the corresponding interrupt was requested.

The interrupt request output pin ( $\overline{INT}$ ) will remain low if the corresponding bit in the interrupt mask register (IMR) is 0.

Bit:	7	6	5	4	3	2	1	0
Symbols:	—*	—*	—*	Q/S	SYNC	IDET	VDET	SDO
Initial value:	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R

The initial value will be 06H if VEDT pin is high.

Bit	Function	Functional description
7 to 5	Reserved bits	Unused
4	Q bit/S bit received interrupt bit	An interrupt is generated when new receive side Q1 to Q4 bits (NT mode) or S1 to S4 bits are received in bits 4 to 7 of the status command register (SCR). An interrupt is not generated if the MFSEL pin is high.
3	Synchronization established/lost state change interrupt bit	An interrupt occurs when the status command register (read) bit 3 (SYNC) changes from 0 to 1 (synchronization established) or from 1 to 0 (synchronization lost).
2	Signal detected/not detected state change interrupt bit	An interrupt is generated when the status command register (read) bit 2 (IDET) changes from 0 to 1 (signal detected) or from 1 to 0 (signal not detected).
1	Voltage detected/not detected state change interrupt bit	An interrupt is generated when the status command register (read) bit 1 (VDET) changes from 0 to 1 (voltage detected) or from 1 to 0 (voltage not detected).
0	Received AMI signal detected interrupt bit	An interrupt is generated when a received AMI signal is detected, even in clock stopped mode. The SDO pin transitions from high to low at the same time.

Note\*: The value read from these bits is always 0.

## 3. Interrupt Mask Register (IMR)

This register masks interrupt sources. The bits correspond to the bits in the interrupt source register.

0: Mask cleared, 1: Mask set

Bit:	7	6	5	4	3	2	1	0
Symbols:	—*	—*	—*	Q/S	SYNC	IDET	VDET	SDO
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note \*: Data may be written but has no effect on HD64520F operation.

4. Status Command Register (SCR)

When read, this register returns the LSI status, and when written issues a command to the LSI.

Bit:	7	6	5	4	3	2	1	0
Symbols:	Q4/S4	Q3/S3	Q2/S2	Q1/S1	SYNC	IDET	VDET	CLK Status
Initial value:	0	0	0	0	0	1	0	1
R/W:	R	R	R	R	R	R	R	R

The initial value will be 07H if the VDET pin is high.

Bit:	7	6	5	4	3	2	1	0
Symbols:	S4/Q4	S3/Q3	S2/Q2	S1/Q1	TA	LSW	CLK STP Enable	CLK STP Release
Initial value:	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W

Bit	Function	Read/Write	Functional description
7 to 4	Receive side Q bit/ S bit display	Read	These bits display the values of the received Q bits (NT mode) or S bits (TE mode).
	Transmit side S bit/ Q bit setting	Write	These bits set the values of the transmitted S bit (NT mode) or Q bits (TE mode).
3	Synchronization establishment	Read	In NT mode a 1 indicates the frame synchronization established state due to a violation. In TE mode a 1 indicates that after the establishment mentioned above, A bits with the value 1 were received three times consecutively.
	A bit value setting	Write	In NT mode, sets the A bit value. Unused in TE mode.
2	Signal detection	Read	A 1 indicates that AMI pulses for 2 bits were detected, and a 0 indicates that the no AMI pulse state was detected for at least 64 continuous bits. Initialized to 1 by a reset, regardless of whether or not a signal is detected.
	Layer 1 start	Write	Controls the layer 1 start signal. 1: Layer 1 start, 0: layer 1 stop. However, LSW must be set to 0 if the LSI transitions to the synchronization established (SYNC = 1) state in TE mode. Note that the LSW input pin must be held at the high level if this bit is used.

## 4. Status Command Register (SCR) (cont)

Bit	Function	Read/Write	Functional description
1	Voltage detection	Read	Indicates the voltage detection state. 0: Not detected, 1: Detected.
	Clock stop mode enable	Write	Controls clock stop mode. Setting this bit to 1 enables setting up clock stop mode. The LSI enters the clock stop state when the IDET = 0 state is detected when this bit is 1. When the LSI enters the clock stop state it automatically clears this bit to 0. This bit is set to 0 by a reset.
0	Clock status	Read	Indicates the operating state of the internal system clock. 1: Clock operating state, 0: Clock stopped state
	Clock stop mode release	Write	Controls clock stop mode. Setting this bit to 1 clears clock stop mode. When the LSI enters the clock operating state it automatically clears this bit to 0. This bit is set to 0 by a reset. Clock stop mode is also automatically cleared by setting the $\overline{SDO}$ pin low (at this time the ISR register bit 0 will be 1).

## 5. B Channel Selection Register (BCHSLR)

This register is used to allocate the B1 and B2 channels to the RBA/RBB pins and the TBA/TBB pins. It is also used to set up bulk

mode. A loopback test can also be setup by setting the LB2 to LBK0 bits. The initial value is 0CH.

Bit:	7	6	5	4	3	2	1	0
Symbols:	LBK2/ BULK2	LBK1/ BULK1	LBK0/ BULK0	EX- Change	B2 Enable	B1 Enable	—*	—*
Initial value:	0	0	0	0	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note \*: The value read from these bits is always 0.

### • B1/B2 independent usage mode

B7	B6	B5	B4	B3	B2	TB1	TB2	RBA	RBB
0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	TBA	1	RB1	1
0	0	0	0	1	0	1	TBB	1	RB2
0	0	0	0	1	1	TBA	TBB	RB1	RB2
0	0	0	1	0	0	1	1	1	1
0	0	0	1	0	1	TBB	1	1	RB1
0	0	0	1	1	0	1	TBA	RB2	1
0	0	0	1	1	1	TBB	TBA	RB2	RB1

Notes: 1. The asterisk indicates the value immediately following a reset.

2. TB1 and TB2 indicate the B1 and B2 channel data in the transmit frame, and RB1 and RB2 indicate the B1 and B2 channel data in the receive frame.

• Bulk mode

<b>B7</b>	<b>B6</b>	<b>B5</b>	<b>B4</b>	<b>B3</b>	<b>B2</b>	<b>TB1 + TB2</b>	<b>RBA</b>	<b>RBB</b>
0	0	1	0	0	0	1	1	1
0	0	1	0	1	1	TBA	RB1 + RB2	×
0	0	1	1	0	0	1	1	1
0	0	1	1	1	1	TBB	×	RB1 + RB2

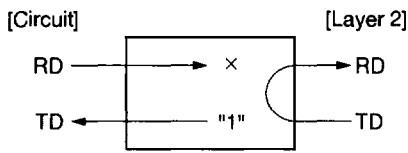
- Notes: 1. The crosses indicate ignored bits.  
 2. Of the TBA and TBB pins, the unused one must be held at 0 or 1.

• Loopback mode

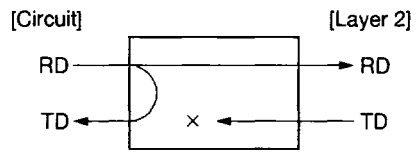
<b>B7</b>	<b>B6</b>	<b>B5</b>	<b>B4</b>	<b>B3</b>	<b>B2</b>	<b>Loopback geometry</b>
0	1	0	×	×	×	D channel local loop
0	1	1	×	×	×	D channel remote loop
1	0	0	0	0	0	BA/BB local loop
1	0	1	0	×	1	B1 remote loop
1	1	0	0	1	×	B2 remote loop
1	1	1	0	1	1	D channel remote loop + B1/B2 remote loop
0	0	1	×	1	0	B channel bulk local loop
0	0	1	0	0	1	B channel bulk remote loop A
0	0	1	1	0	1	B channel bulk remote loop B

Note: The crosses indicate ignored bits.

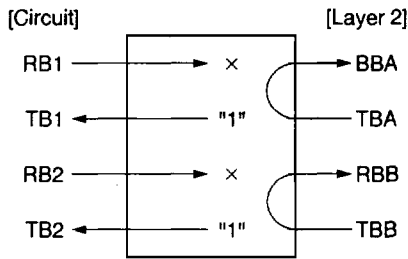
(1) D Channel Local Loop



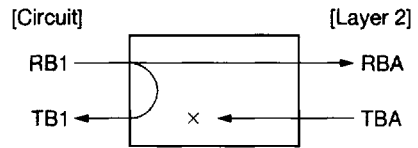
(2) D Channel Remote Loop



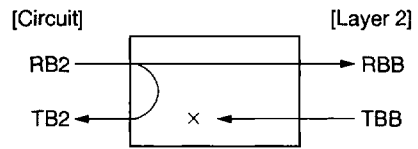
(3) BA, BB Local Loop



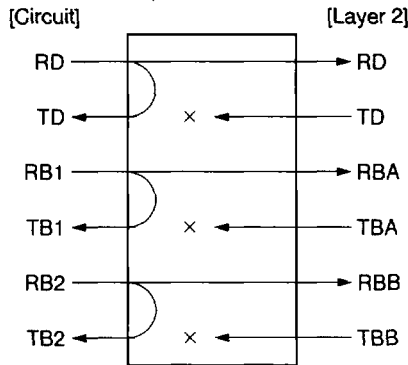
(4) B1 Remote Loop



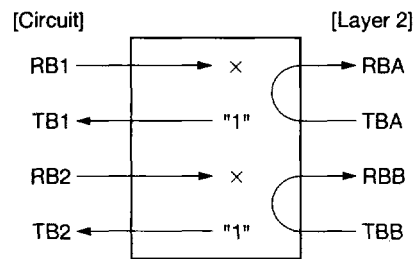
(5) B2 Remote Loop



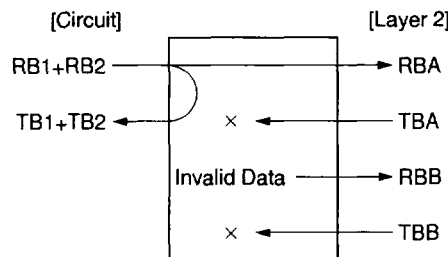
(6) D Channel Remote Loop B + B1, B2 Remote Loop



(7) B Channel Bulk Local Loop



(8) B Channel Bulk Remote Loop A



(9) B Channel Bulk Remote Loop B

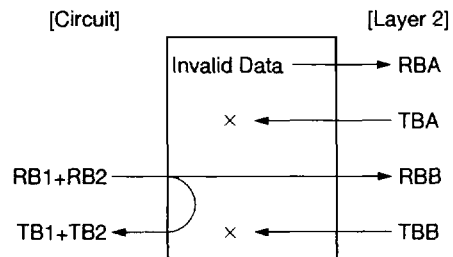


Figure 1. Loopback Geometries

6. Test Function Register (TFR)

This register is used to control the INFO1 to INFO4 forced output function, to select the M

bit polarity, and to set the logic block independent and driver/receiver block independent modes.

Bit:	7	6	5	4	3	2	1	0
Symbols:	ITM2	ITM1	ITM0	—*	—*	MPOL SEL	LGON	DRON
Initial value:	0	0	0	0	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note \*: The value read from these bits is always 0.

• INFO1 to INFO4 forced output function

No.	ITM2	ITM1	ITM0	INFO signal
1	0	0	0	Normal operation
2	0	0	1	INFO1
3	0	1	0	INFO2
4	0	1	1	INFO3
5	1	0	0	INFO4

Note: The INFO signal according to the settings in the table is always output, regardless of whether the LSI is operating in NT or TE mode.

• M bit polarity selection function

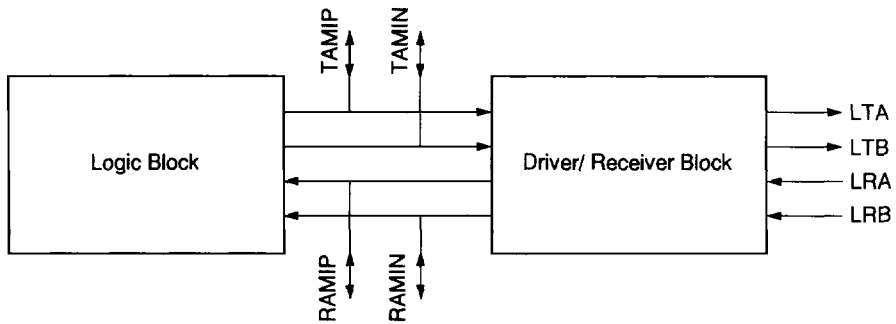
Setting	Multiframe No.	M bit
0	1	1
	A value other than 1	0
1	1	0
	A value other than 1	1

• Logic block independent and driver/receiver block independent modes

These are modes that allow the HD64520F internal logic block or the driver/receiver block

to be operated independently. The table lists the functions of the LRA/B, LTA/B, RAMIP/N, and TAMIP/N pins in these modes.

No.	LGON	DRON	Mode	LRA/B	LTA/B	RAMIP/N	TAMIP/N
1	1	1	Normal operation	Analog input	Analog output	Digital output	Digital output
2	1	0	Logic block independent	Unused	High impedance	Digital input	Digital output
3	0	1	Driver/receiver block independent	Analog input	Analog output	Digital output	Digital input



## Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power-supply voltage	$V_{CC}^*$	-0.3 to +6.7	V
Input voltage	$V_{in}^*$	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	-20 to +75	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

Note: Values referenced to  $V_{SS} = 0$  V.

Using this LSI at levels that exceed the absolute maximum ratings may permanently damage the LSI. In normal operation, it is desirable that this LSI be used within the recommended operating condition. Exceeding those conditions may adversely influence LSI reliability.

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power-supply voltage	$V_{CC}^*$	4.75	5.00	5.25	V
Operating temperature	$T_{opr}$	-20	25	75	°C
Input voltage	$V_{in}$	-0.3	—	$V_{CC} + 0.3$	V

Note: Values referenced to  $V_{SS} = 0$  V.

**Electrical Characteristics**
**DC Characteristics** ( $V_{CC} = 5\text{ V} \pm 5\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless specified otherwise)

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input high-level voltage $\overline{\text{RESET}}$ , EXTAL, and VDET pins	$V_{IH1}$	$V_{CC} - 0.6$	—	$V_{CC} + 0.3$	V	
Input high-level voltage Pins other than $\overline{\text{RESET}}$ , EXTAL, and VDET	$V_{IH2}$	2.2	—	$V_{CC} + 0.3$	V	
Input low-level voltage $\overline{\text{RESET}}$ , EXTAL, and VDET pins	$V_{IL1}$	-0.3	—	0.6	V	
Input low-level voltage Pins other than $\overline{\text{RESET}}$ , EXTAL, and VDET	$V_{IL2}$	-0.3	—	0.8	V	
Output high-level voltage All output pins	$V_{OH}$	2.4	—	—	V	$I_{OH} = -200\ \mu\text{A}$
	$V_{OH}$	$V_{CC} - 1.2$	—	—	V	$I_{OH} = -20\ \mu\text{A}$
Output low-level voltage All output pins	$V_{OL}$	—	—	0.5	V	$I_{OL} = 2.2\ \text{mA}$
Input leakage current Input pins other than XTAL and EXTAL	$ I_{IL} $	—	—	10	$\mu\text{A}$	$V_{in} = 0.5$ to $V_{CC} - 0.5$
Three-state leakage current	$ I_{TL} $	—	—	10	$\mu\text{A}$	$V_{in} = 0.5$ to $V_{CC} - 0.5$
Current drain (normal operating mode)	$I_{CC}$	—	17	22	mA	With a ITU-T I.430 recommendation $50\ \Omega$ load resistance. System clock $f = 12.288\ \text{MHz}$
Current drain (clock stop mode)	$I_{CCSTP}$	—	—	800	$\mu\text{A}$	
Pin capacitance	$C_P$	—	—	15	pF	

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## AC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test condition
Receive data to transmit data delay	Rtd	—	2.0	—	bit	Figure 2
Crystal oscillator frequency deviation	D <sub>XTL</sub>	-100	—	+100	p.p.m	I.430 8.1.2
Timing extraction jitter	J	-7	—	+7	%	I.430 8.2.2
Total phase deviation	TPD	-7	—	+15	%	I.430 8.2.3
Allowable loop delay	D <sub>rt</sub>	10	—	14	μS	I.430 A2.1.2, figure 3
Receive side input potential difference (between the LRA and LRB pins)	V <sub>LR</sub>	0.3	—	V <sub>CC</sub> + 0.3	V	Figure 13
Receive side input impedance	Z <sub>LR</sub>	—	5	—	kΩ	
Transmit side output potential difference (between the LTA and LTB pins)	V <sub>LT50</sub>	1.35	—	1.65	V	R <sub>L</sub> = 200 Ω (It is equal to R <sub>L</sub> = 50 Ω of I.430). Figure 13.
	V <sub>LT400</sub>	1.35	—	2.2	V	R <sub>L</sub> = 1.6 kΩ (It is equal to R <sub>L</sub> = 400 Ω of I.430). Figure 13.
	V <sub>LT56</sub>	—	—	0.15	V	R <sub>L</sub> = 22.4 kΩ (It is equal to R <sub>L</sub> = 5.6 kΩ of I.430). Figure 13.
Transmit side output impedance	Z <sub>LT0</sub>	—	24	—	Ω	Binary 0 output
	Z <sub>LT1</sub>	—	5	—	kΩ	Binary 1 output
Transmit pulse rise time	t <sub>LT<sub>r</sub></sub>	—	150	—	ns	Figure 13
Transmit output limiting current	I <sub>LT</sub>	—	—	10	mA	

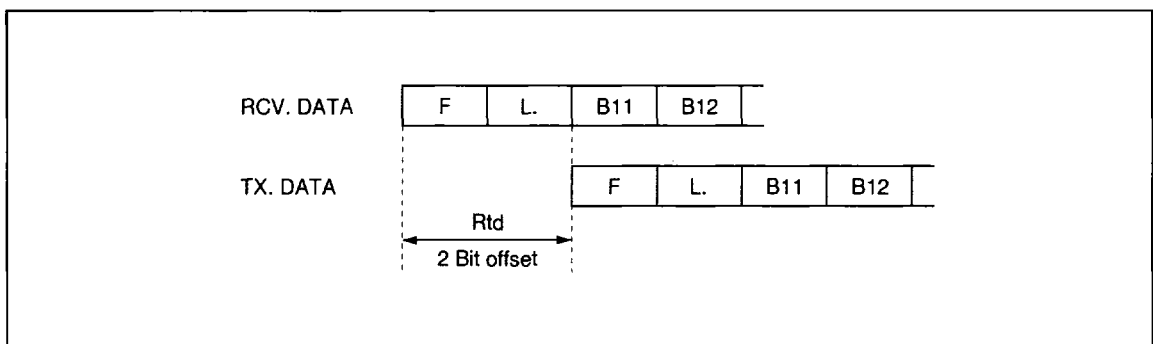
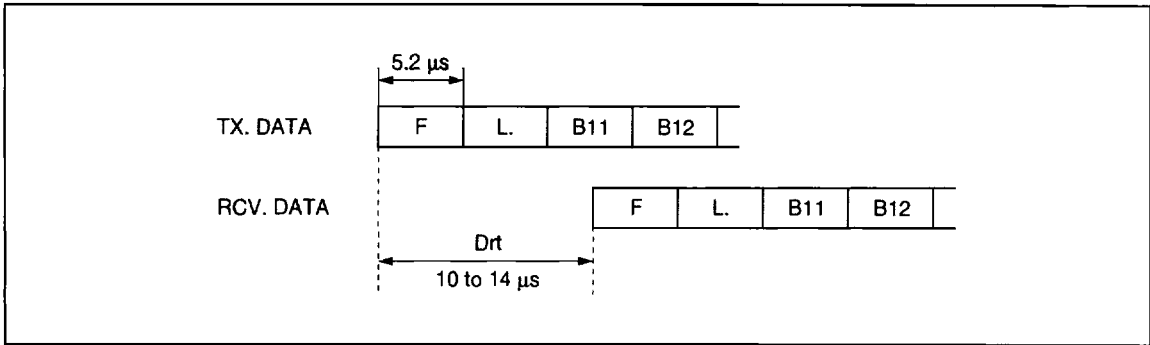


Figure 2. TE Mode Transmit Data Offset



**Figure 3. Allowable Receive Side Data Delay for Short Distance Reception Operation Bus Geometries in NT mode**

**B Channel Interface**

Item	Symbol	Min	Typ	Max	Unit	Test condition
Clock cycle time (normal mode)	t <sub>BCYCN</sub>	15.623	—	15.627	μs	Figure 4 (f = 64 kHz)
Clock cycle time (bulk mode)	t <sub>BCYCB</sub>	7.811	—	7.814	μs	Figure 5 (f = 128 kHz)
Clock duty	Duty	45	50	55	%	Figures 4 and 5, D = t <sub>CH</sub> /t <sub>cyc</sub>
Clock rise time	t <sub>cr</sub>	—	—	50	ns	Figures 4 and 5
Clock fall time	t <sub>cf</sub>	—	—	50	ns	
Frame clock phase difference	t <sub>CD</sub>	-250	—	250	ns	
Receive side data output delay time	t <sub>BD</sub>	—	—	1	μs	
Transmit data setup time	t <sub>BS</sub>	3	—	—	μs	
Transmit data hold time	t <sub>BH</sub>	3	—	—	μs	

**D Channel Interface**

Item	Symbol	Min	Typ	Max	Unit	Test condition
Timing clock cycle time	t <sub>RTCYC</sub>	62.49	62.50	62.51	μs	Figure 6 (RTIO pin)
Timing clock rise time	t <sub>RT<sub>r</sub></sub>	—	—	50	ns	
Timing clock fall time	t <sub>RT<sub>f</sub></sub>	—	—	50	ns	
Timing clock positive pulse width	t <sub>RTP</sub>	5.1	—	5.3	μs	
Receive side D channel data output delay time	t <sub>RD</sub>	—	—	1.0	μs	Figure 6 (RDO pin)
Transmit side D channel data input setup time	t <sub>TD</sub>	—	—	2.5	μs	Figure 6 (TDI pin)
Receive side E bit data output confirmation time	t <sub>RED</sub>	-2.0	—	—	μs	Figure 6 (RE pin)

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## Rise and Fall Times

Item	Symbol	Min	Typ	Max	Unit	Test condition
External clock rise time	$t_{EXr}$	—	—	25	ns	Figure 7
External clock fall time	$t_{EXf}$	—	—	25	ns	
Input pin rise time (except for the $\overline{\text{RESET}}$ pin)	$t_{ir}$	—	—	100	ns	Figure 8
Input pin fall time (except for the $\overline{\text{RESET}}$ pin)	$t_{if}$	—	—	100	ns	
Oscillator stabilization time	$t_{OSC}$	—	—	20	ms	—
$\overline{\text{RESET}}$ rise time	$t_{Rr}$	—	—	50	ms	Figure 9
$\overline{\text{RESET}}$ fall time	$t_{Rf}$	—	—	50	ms	
Valid $\overline{\text{RESET}}$ pulse width	$t_{RVALID}$	6	—	—	cycle	

## CPU Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Address setup time	$t_{AS}$	0	—	—	ns	Figure 10
Data output delay time	$t_{DD}$	—	—	80	ns	
Data output hold time	$t_{DH}$	0	—	—	ns	
Address hold time	$t_{AHL}$	20	—	—	ns	
Data setup time	$t_{DSUP}$	150	—	—	ns	
Data hold time	$t_{DHL}$	20	—	—	ns	
R/W pulse width	$t_{RWW}$	200	—	—	ns	

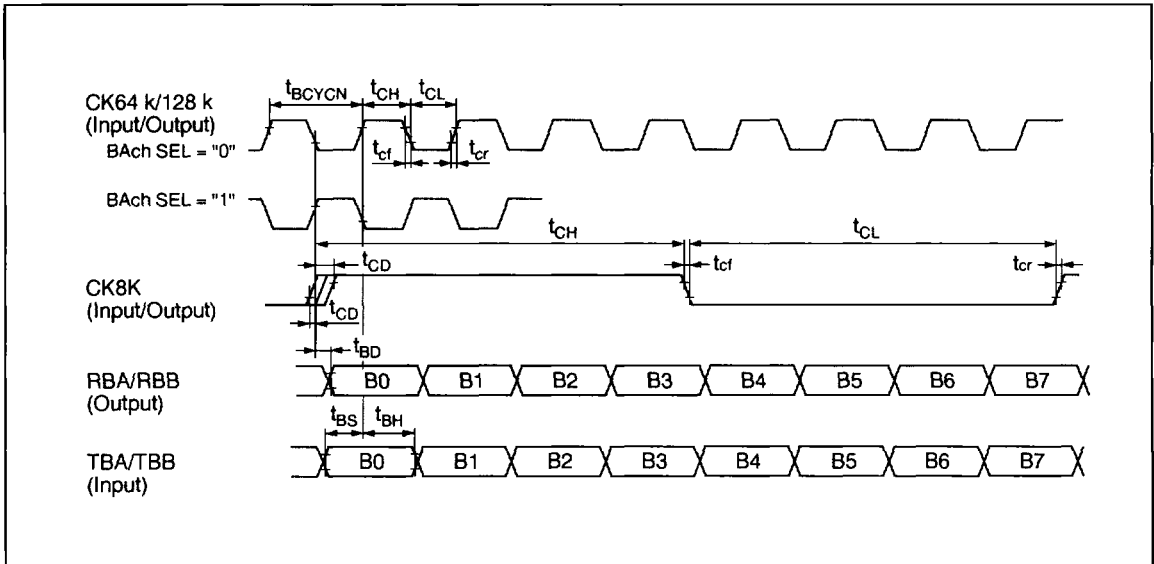
## Multiframe Timing

Item	Symbol	Min	Typ	Max	Unit	Test condition
SCR(W) S1/Q1 to S4/Q4 bit set time	$t_{SQST}$	—	—	50	$\mu\text{s}$	Figure 12
6 SCR(W) S1/Q1 to S4/Q4 bit hold time	$t_{SQHLD}$	75	—	—	$\mu\text{s}$	
7 SCR(R) Q1/S1 to Q4/S4 bit valid output time	$t_{QSVAL}$	0	—	—	ns	
Q/S bit valid output time	$t_{RQSVAL}$	—	—	50	$\mu\text{s}$	
Q/S bit set time	$t_{TSQST}$	—	—	50	$\mu\text{s}$	

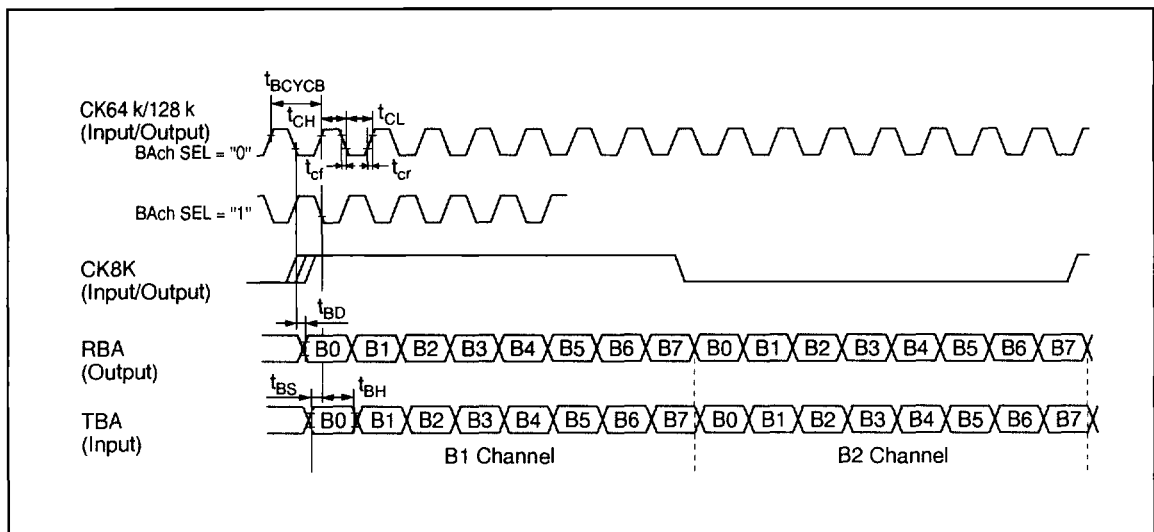
**Transmit Frame External Synchronization Timing**

Item	Symbol	Min	Typ	Max	Unit	Test condition
200 kHz clock setup time	$t_{20SU}$	70	—	250	$\mu s$	Figure 14
4 kHz clock setup time	$t_{4KSU}$	0	—	—	ns	
Line frame output delay time	$t_{LFD}$	13	—	14	$\mu s$	

**Timing Charts**



**Figure 4. B Channel Data I/O Timing (normal mode)**



**Figure 5. B Channel Data I/O Timing (bulk mode)**

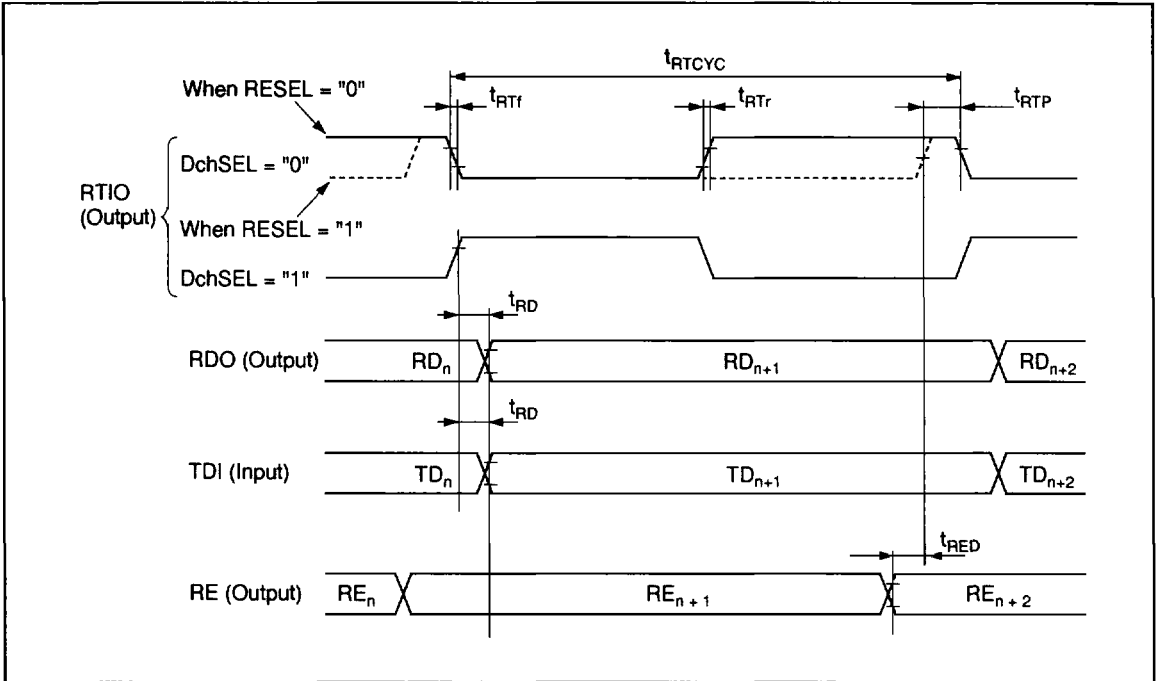


Figure 6. D Channel Data I/O Timing

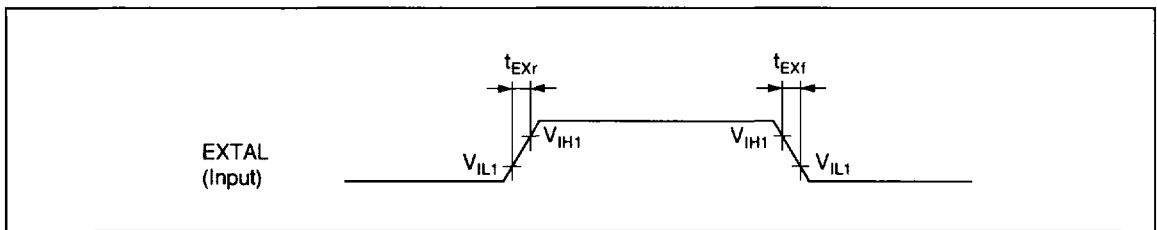


Figure 7. External Clock Input Rise and Fall Times

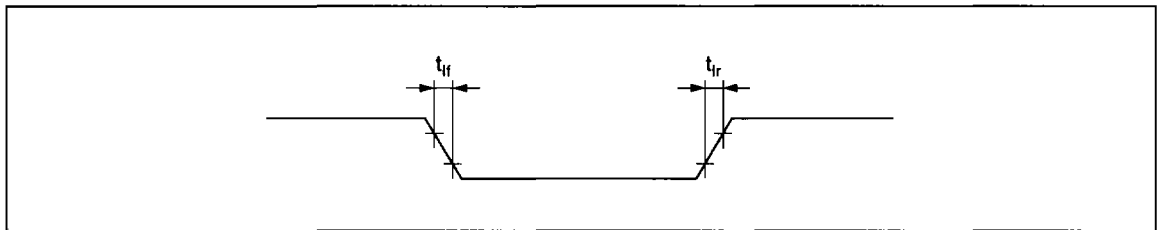


Figure 8. Input Signal Rise and Fall Times (except for the EXTAL and RESET pins)

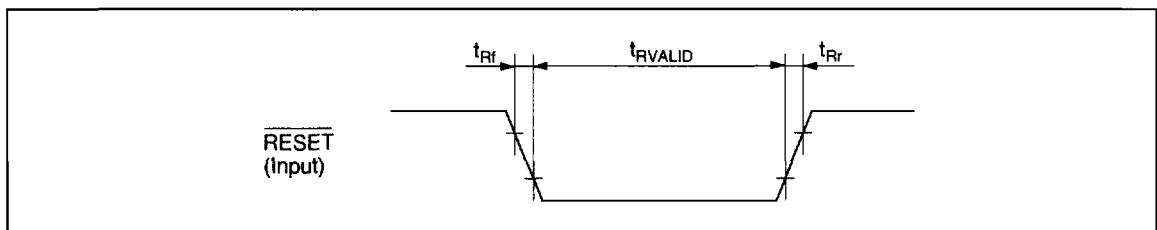


Figure 9. RESET Timing

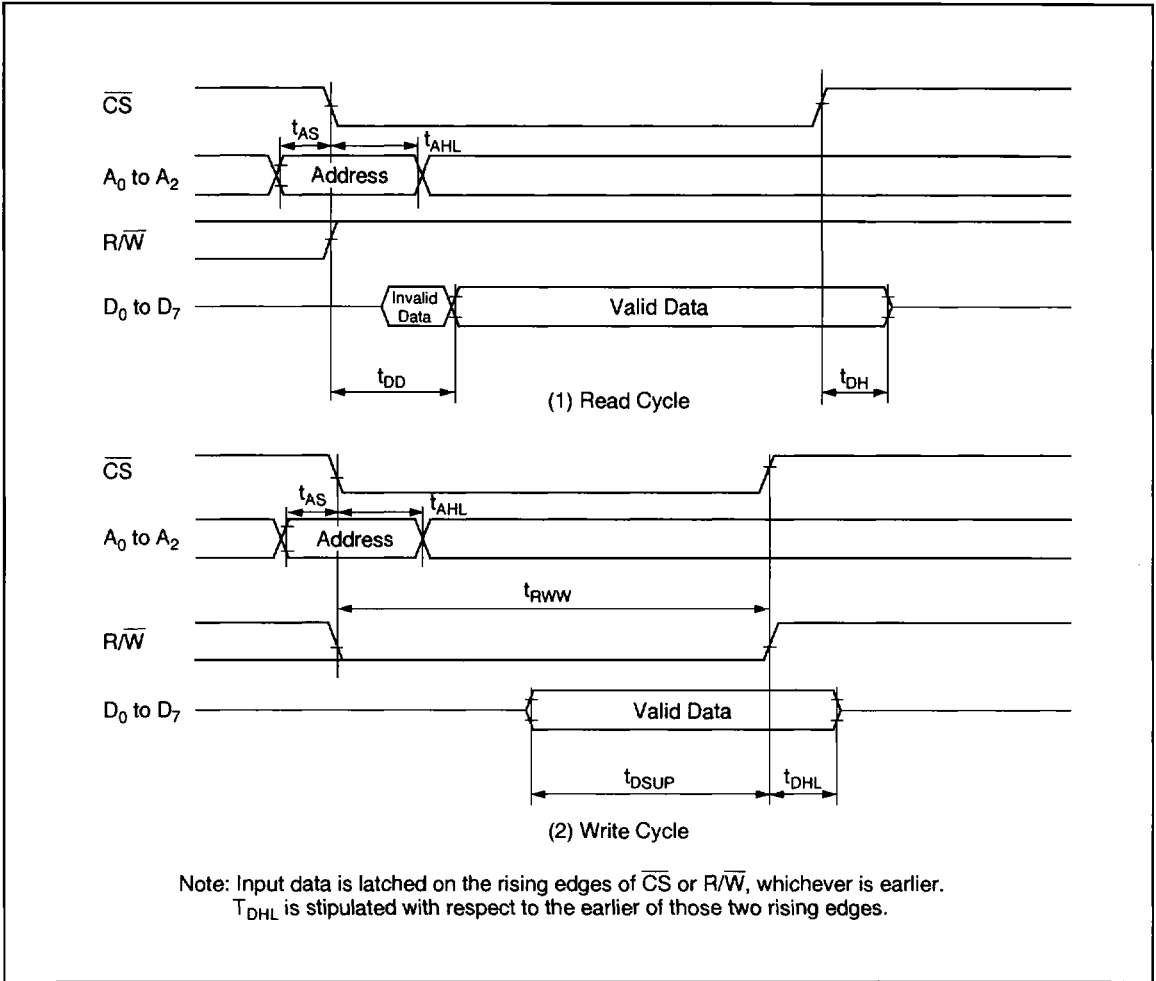


Figure 10. CPU Read/Write Timing

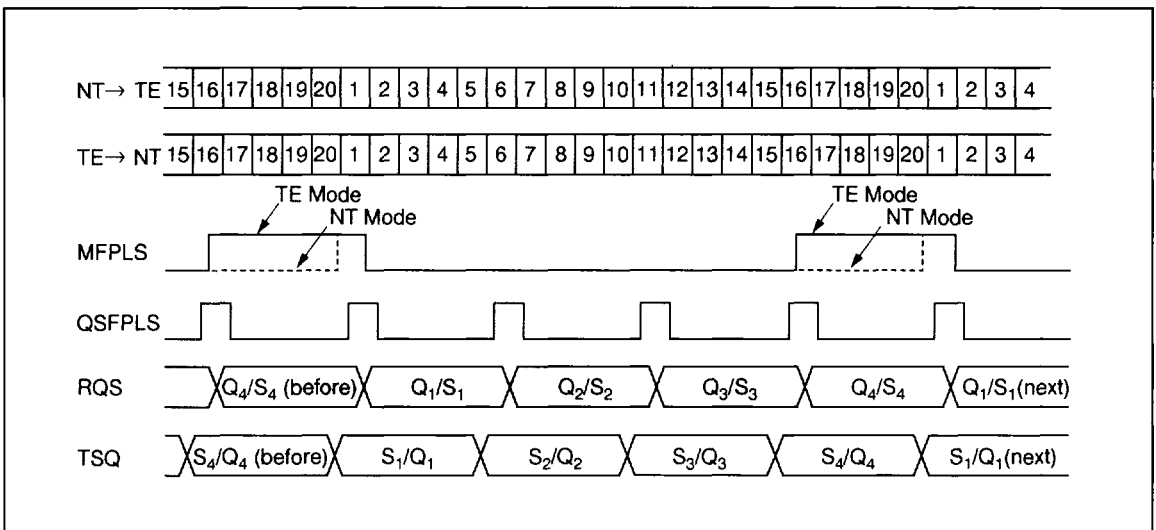


Figure 11. Multiframe Timing (overall)

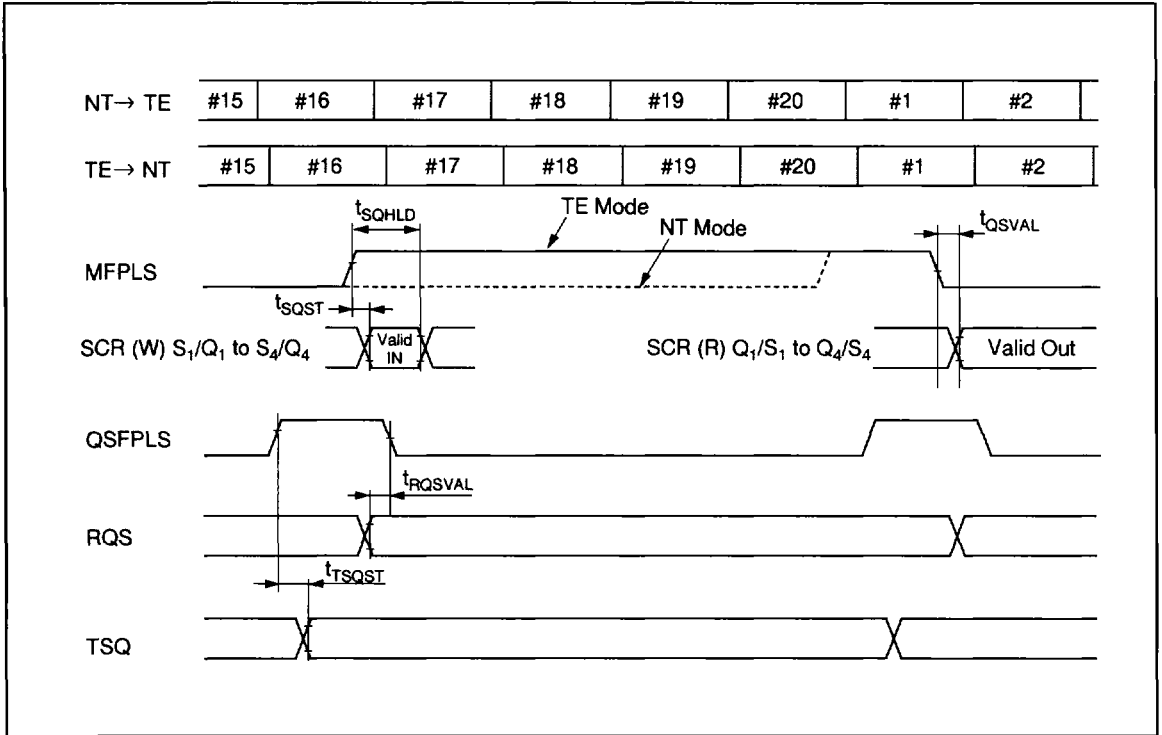


Figure 12. Multiframe Timing

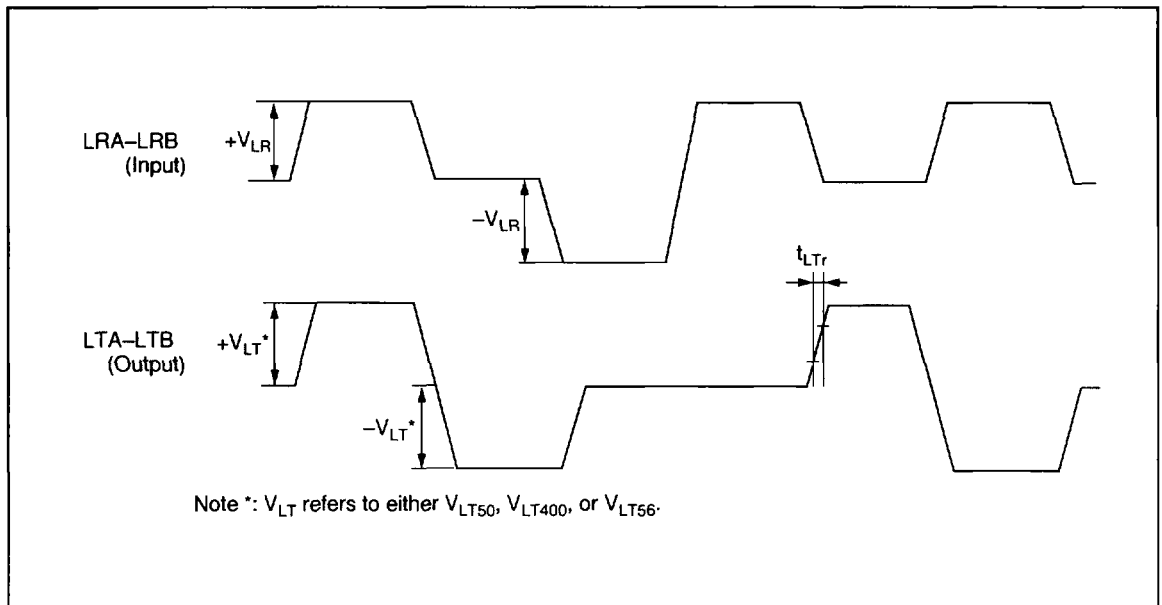


Figure 13. Receiver Input/Driver Output

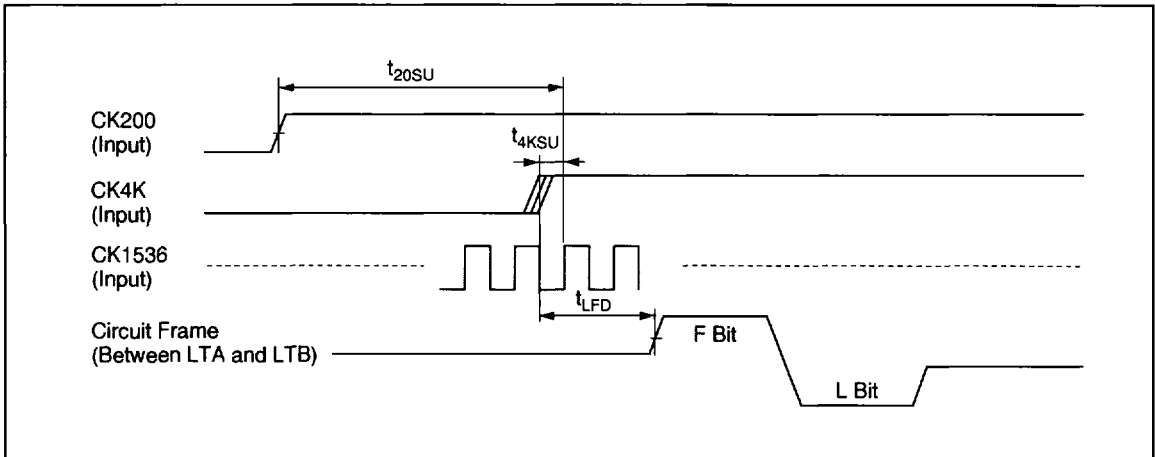


Figure 14. Transmit Frame External Synchronization Timing

Bus Timing Test Loads and Reference Levels

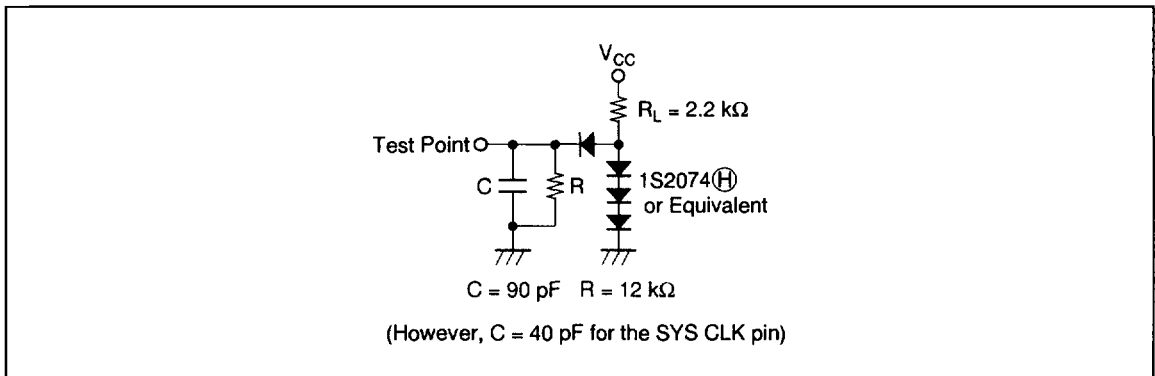


Figure 15. Bus Timing Test Load Circuit (TTL load)

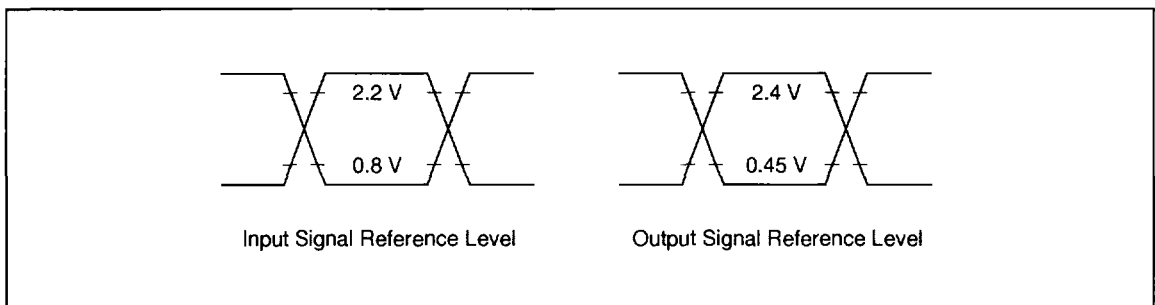


Figure 16. Reference Levels

External Component Connection Example

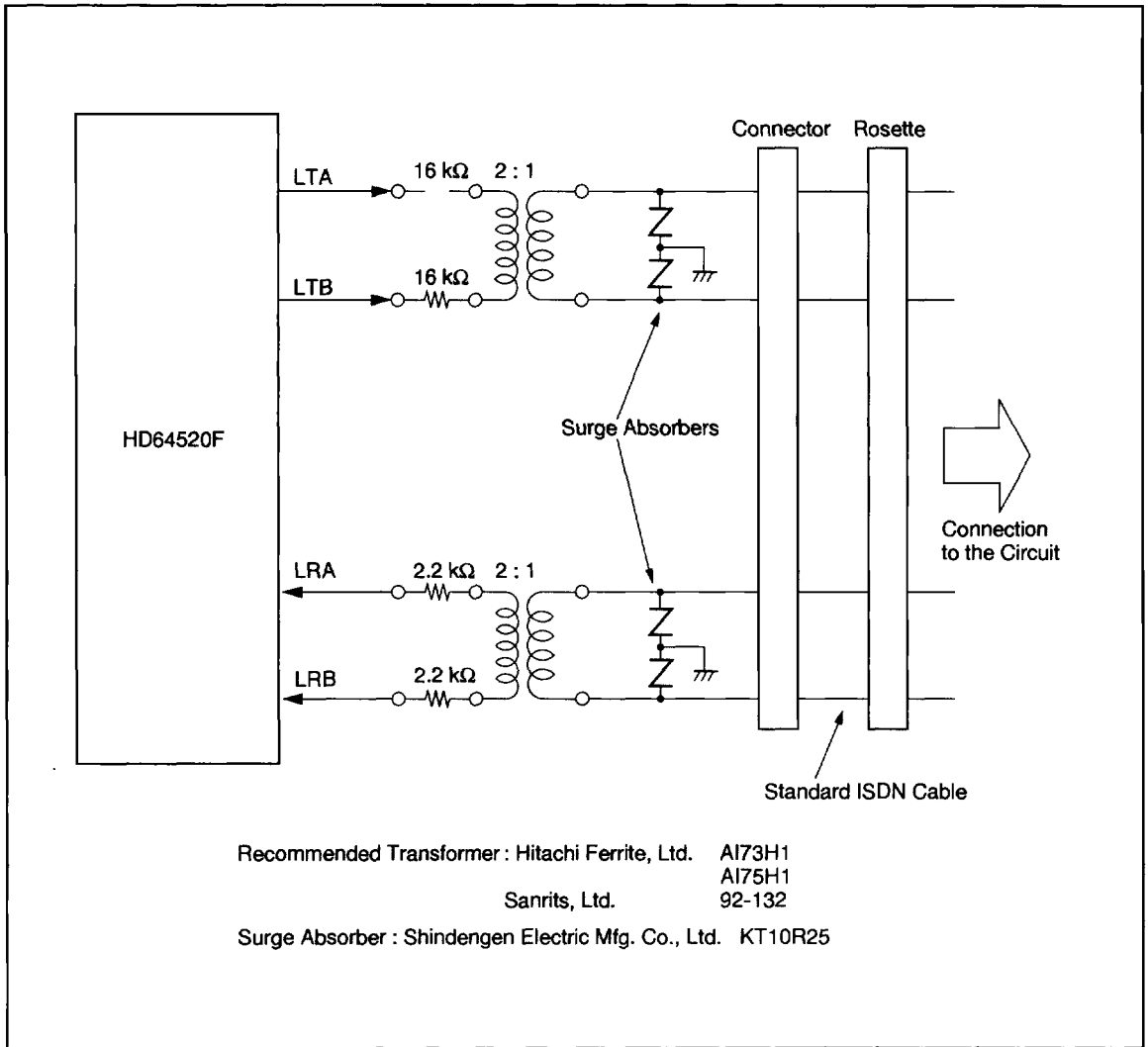


Figure 17. External Component Connection Example