PREVIEW

TS 83512

BIPOLAR HIGH SPEED 12 BITS / 20 MHz A/D CONVERTER

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DESCRIPTION

The TS 83512 is a monolithic bipolar 12 bits Analog-to-Digital converter using a new subranging architecture with on board T/H amplifier and voltage reference.

With an encode rate of 20 MHz, the TS 83512 is specified to operate from commercial to military temperature range with analog input frequency up to 10 MHz, making it ideal for a variety of applications and environments.

Available also in die form.
Evaluation board available.

MAIN FEATURES

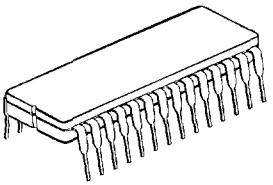
- 12-bits resolution.
- 20 MHz sampling rate.
- Up to 10 MHz input signal frequency.
- Power supply : +5 V ; −5.2 V.
- −55°C / +125°C specified.
- Guaranteed monotonicity.
- Power consumption : 1.25 W.
- Analogic input : ±1 V.
- Clock input / data output : TTL.
- INL typ : ±1.2 LSB.
- DNL typ : ±0.5 LSB.
- Analog input bandwidth : 100 MHz.
- AD 9022, AD 9026 compatibility.
- Similar to AD 872 / AD 872A / AD 871.
- Upgraded version of AD 9005.
- NRZ circuit.

APPLICATIONS

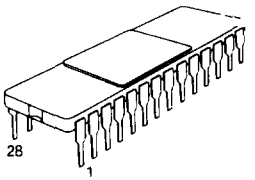
- Digital communications.
- Radar pulse analysis.
- Image processing.
- Medical imaging.
- High energy physics.
- X-Ray and ultrasound imaging.
- Digital instrumentation.
- Telecom wideband transmission.
- Digital filter.

PACKAGING / QUALIFICATION INFORMATION

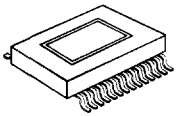
- 3 standard versions : Mil Temp : −55°C, +125°C ; Industrial Temp : −40°C to +85°C ; Civil Temp : 0, +70°C.
- MIL STD 883 class B.
- DESC/SMD planned.
- Packages :
  - Ceramic DIL 28,
  - Dual Ceramic flat pack-28. (under consideration).



J suffix
DIL 28
Cerdip package



C suffix
DIL 28
Side Brazed Ceramic package



Z suffix
DFP 28
Ceramic Dual flat pack

ABSOLUTE MAXIMUM RATINGS (see Note)

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		0 to 6	V
Negative supply voltage	V_{EE}		− 6 to 0	V
Analog input voltage	V_{IN}		V_{EE} to + 3	V
Clock input voltage	CLK		0 to V_{CC}	V
Digital output current	I_D		20	mA
Junction temperature — Plastic package	T_j		+ 150	°C
Junction temperature — Ceramic package			+ 175	°C
Storage temperature	T_{stg}		− 65 to + 150	°C
Operating temperature range	T_{case}	Civil : «C» grade Industrial : «V» grade Military : «M» grade	0 to 70 − 40 to + 85 − 55 to + 125	°C °C °C
Lead temperature (soldering 10 s)	T_{leads}		+ 260	°C

Note : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

RECOMMENDED CONDITIONS OF USES

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	AV_{CC}, DV_{CC}			5		V
Negative supply voltage	V_{EE}			− 5.2		V
Analog input voltage	V_{IN}			± 1		V
Clock input voltage	CLK			TTL levels		
Load		Single LS latch		6	10	pF
Decoupling		All power supplies must be decoupled with an external 100 nF chip capacitors.				
Operating temperature range	T_{case}	Civil : «C» grade Industrial : «V» grade Military : «M» grade		0 to 70 − 40 to + 85 − 55 to + 125		°C °C °C

SPECIFICATIONS

Electrical operating characteristics

$V_{EE} = -5.2\ V$; $V_{CC} = 5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				12		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility				TTL		
Clock inputs						
• Logic «0» voltage	full	IV	0		0.8	V
• Logic «1» voltage	full	IV	2		5	V
Output data						
• Logic «0» voltage (Note 1)	full	II	0		0.5	V
• Logic «1» voltage (Note 1)	full	II	2.4		5	V
MAXIMUM CLOCK FREQUENCY		III		20		MHz
MINIMUM CLOCK FREQUENCY		III		1		MHz
ANALOG INPUT						
Voltage range	full	V		±1		V
Input capacitance		IV		7		pF
Input resistance		V		2		kΩ
Analog bandwidth (Note 2)		V		100		MHz
POWER REQUIREMENTS						
Positive supply voltage		I	4.75	5	5.25	V
	full	II	4.75	5	5.25	V
Positive supply current		I		TBD		mA
	full	II		TBD		mA
Negative supply voltage		I	−5.45	−5.2	−4.95	V
	full	II	−5.45	−5.2	−4.95	V
Negative supply current		I		TBD		mA
	full	II		TBD		mA
Nominal power dissipation		V		1.25	TBD	W
ACCURACY						
Integral nonlinearity (Notes 2 and 3)		I		1.2	2	LSB
	full	II			3	LSB
Differential nonlinearity (Notes 2 and 3)		I		0.5	0.8	LSB
	full	II			1	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

$V_{EE} = -5.2\ V$; $V_{CC} = 5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (Note 4)					
Signal to noise ratio (SNR) (Note 2)					
F_S = 20 MHz F_{in} = 1 MHz	I		68		dB
F_S = 20 MHz F_{in} = 5 MHz	I		66		dB
F_S = 20 MHz F_{in} = 10 MHz	I		65		dB
Signal to noise and distortion ratio (SINAD) (Note 2)					
F_S = 20 MHz F_{in} = 1 MHz	I		67		dB
F_S = 20 MHz F_{in} = 5 MHz	I		65		dB
F_S = 20 MHz F_{in} = 10 MHz	I		63		dB
Total harmonic distorsion (THD) (Note 2)					
F_S = 20 MHz F_{in} = 1 MHz	I		−75		dBc
F_S = 20 MHz F_{in} = 5 MHz	I		−74		dBc
F_S = 20 MHz F_{in} = 10 MHz	I		−70		dBc
Effective number of bits (ENOB)					
F_S = 20 MHz F_{in} = 1 MHz	I		10.8		Bits
F_S = 20 MHz F_{in} = 5 MHz	I		10.5		Bits
F_S = 20 MHz F_{in} = 10 MHz	I		10.2		Bits

Note 1 : TS 83512 load is a single LS latch.
Note 2 : See definition of terms.
Note 3 : Histogram based on sampling of 1 MHz sinusoïdal analog signal with an encode rate of 5 MHz.
Note 4 : For dynamic performance, duty cycle of encode command should be 50 % ±10 %.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested at +25°C.
II	100 % production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample basic).
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	All devices are 100 % production tested at +25°C. 100 % production tested at temperature extremes for military temperature devices, guaranteed by design and and characterization testing for (civil) and industrial devices.
D	100 % probe tested on wafer at T_{amb} = +25°C.

THERMAL CHARACTERISTICS

Package	Parameter	Symbol	Typ.	Unit
Cerdip 28	Thermal resistance - Ceramic junction to ambient	θ_{JA}	32	°C/W
	Thermal resistance - Ceramic junction to case	θ_{JC}	10	°C/W
DFP 28	Thermal resistance - Ceramic junction to ambient	θ_{JA}	45	°C/W
	Thermal resistance - Ceramic junction to case	θ_{JC}	13	°C/W

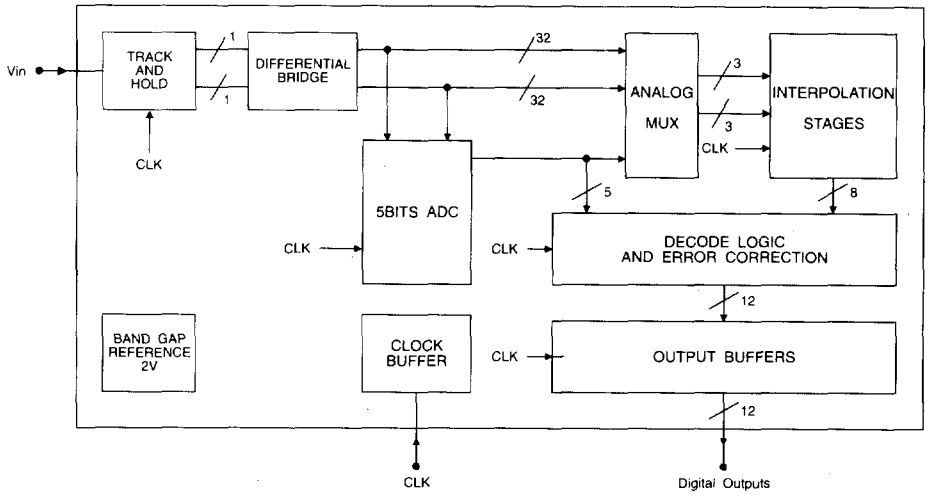


Figure 1 : TS 83512 block diagram.

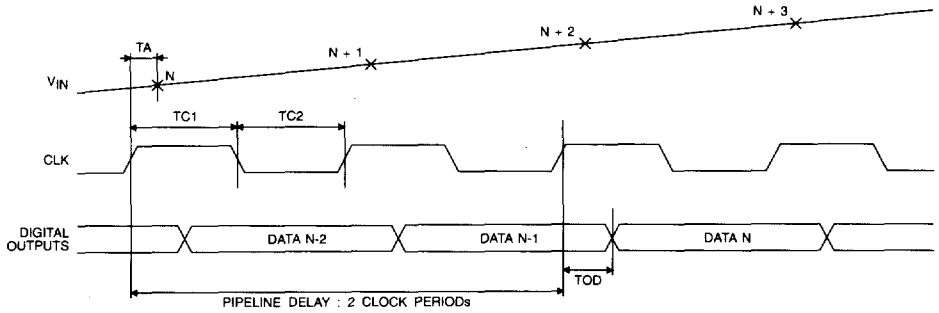


Figure 2 : TS 83512 timing diagram.

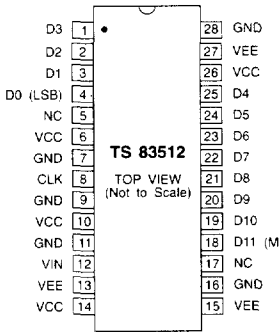
SWITCHING PERFORMANCES (Notes 1, 2 and 3) - see Figure 2

Parameter	Symbol	Typ.	Unit
Minimum Clock pulse width (high)	TC1	25	ns
Minimum Clock pulse width (low)	TC2	25	ns
Aperture delay	TA	TBD	ns
Aperture uncertainty	Jitter	10	ps, rms
Output delay	TOD	20	ns
Output rise time (Note 4)		15	ns
Output fall time (Note 4)		15	ns

Note 1 : See definitions of terms.
Note 2 : $AV_{CC} = DV_{CC} = 5\ V$; $V_{EE} = -5.2\ V$; $T_C = 25°C$.
Note 3 : Typical clock duty cycle is 50 %.
Note 4 : Outputs connected to a single LS latch.

PIN DESCRIPTION

Pin	Name	Function
13, 15, 27	V_{EE}	– 5.2 V power supply.
7, 9, 11, 16, 28	GND	Analog and digital ground.
6, 10, 14, 26	V_{CC}	+ 5 V power supply.
12	V_{IN}	Analog input.
8	CLK	TTL encode clock input to ADC. Internal T/H is placed in hold mode, (ADC is encoding), on the rising edge of encode signal.
1, 2, 3, 4, 18, 19, 20, 21, 22, 23, 24, 25	D0-D11	Digital TTL output bits. D0 is the least significant bit, and D11 is the most significant bit.
5, 17	NC	Not connected.



DEFINITION OF TERMS

Analog bandwidth

The analog input frequency at which the fundamental component in the reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis).

Differential non linearity (DNL)

The differential non linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all |DNL (i)|. DNL error specification of less than 1 LSB guarantees that there are no missing output codes, and that the transfer function is monotonic.

Integral non linearity (INL)

The integral non linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.

Signal to noise ratio (SNR)

The ratio of the RMS signal amplitude to the RMS sum of all other spectral components, without harmonics.

Signal to noise and distortion ratio (SINAD)

The ratio of the RMS signal amplitude to the RMS sum of all other spectral components, including significant harmonics except DC.

Total harmonic distortion (THD)

The ratio of the five most significant harmonic components in the spectrum of the quantized representation, to the fundamental spectral component.

Aperture delay (TA)

The delay between the rising edge of CLK signal and the time at which V_{IN} is sampled.

Output delay (TOD)

The delay from the rising edge of CLK (50 % point) to the V_{OH} = 2 V or V_{OL} = 0.8 V of the digital outputs with 10 pF maximum load.

Non return to zero (NRZ)

If V_{IN} exceeds positive full scale (+ 1 V), output data remain at high level.

Analog input	Voltage level	Digital output
+1.0005 V	Positive full scale +1 LSB	MSB ... LSB 1111111111
+1 V	Positive full scale Full scale −1 LSB	1111111111 1111111110
+1/2 V	Positive 1/2 scale 1/2 scale −1 LSB	1100000000 1011111111
0 V	Bipolar zero (offset zero)	1000000000 01111111111
−1/2 V	1/2 scale +1 LSB Negative 1/2 scale	0100000000 0011111111
−1 V	Full scale +1 LSB Negative full scale	0000000001 0000000000
−1.0005 V	Negative full scale −1 LSB	0000000000

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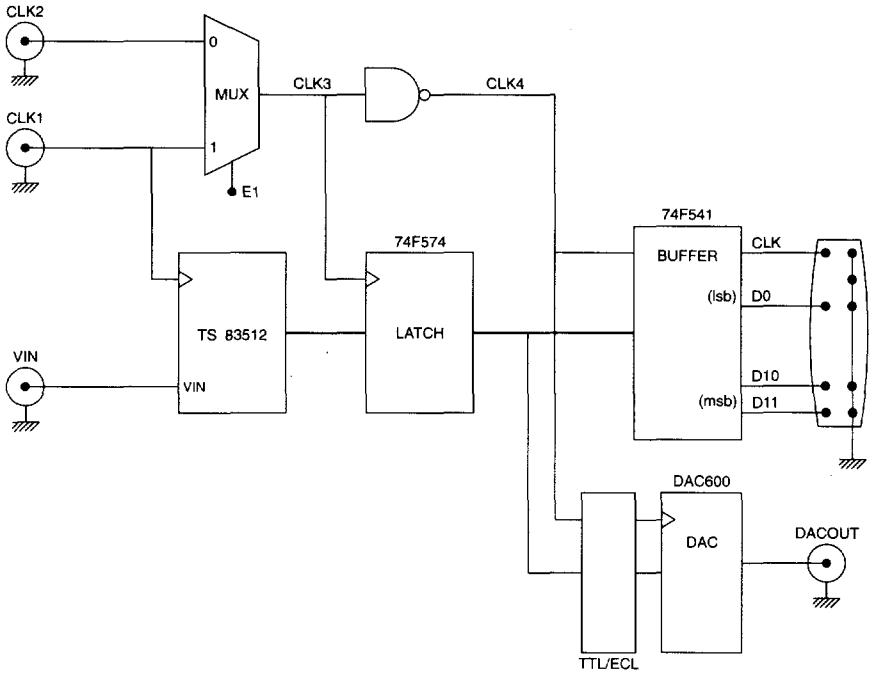
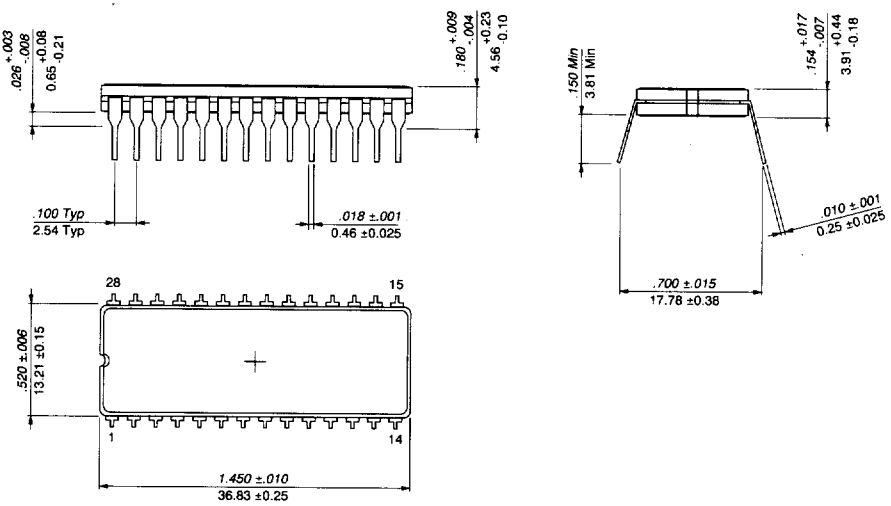
EVALUATION BOARD BLOCK DIAGRAM

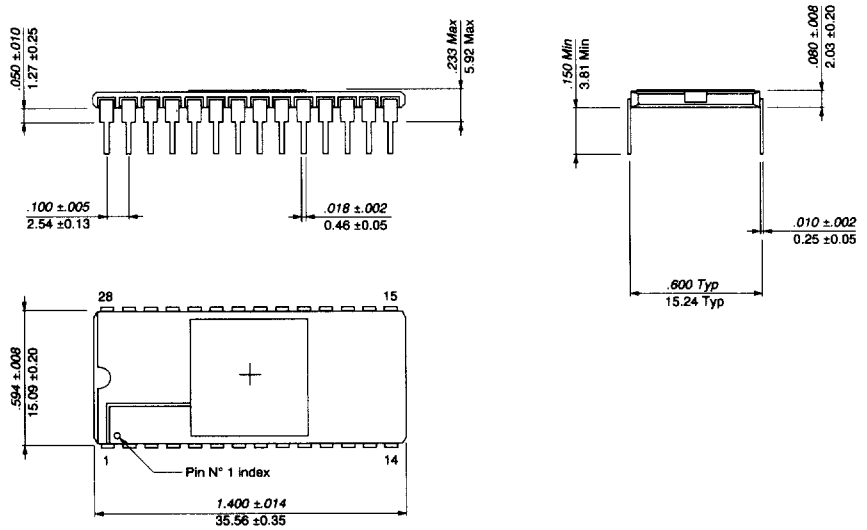


OUTLINE DIMENSIONS

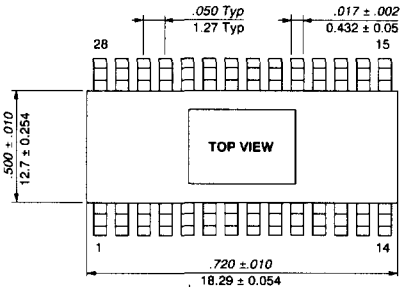
DIL 28 - Cerdip package (J suffix) (Dimensions in inches and mm)

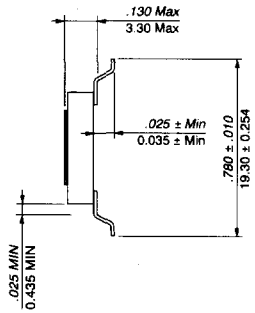


DIL 28 - Ceramic Side Brazed (C suffix) (Dimensions in inches and mm)



DFP 28 - Dual Ceramic Flat Pack (Dimensions in inches and mm)





DIE MECHANICAL INFORMATION : JTS 83512

Pad layout : V974

Die size : 3.9 × 3.65 mm = 14.3 mm²

Die thickness : 380 µm

Metallization : Al-Ni-Au (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

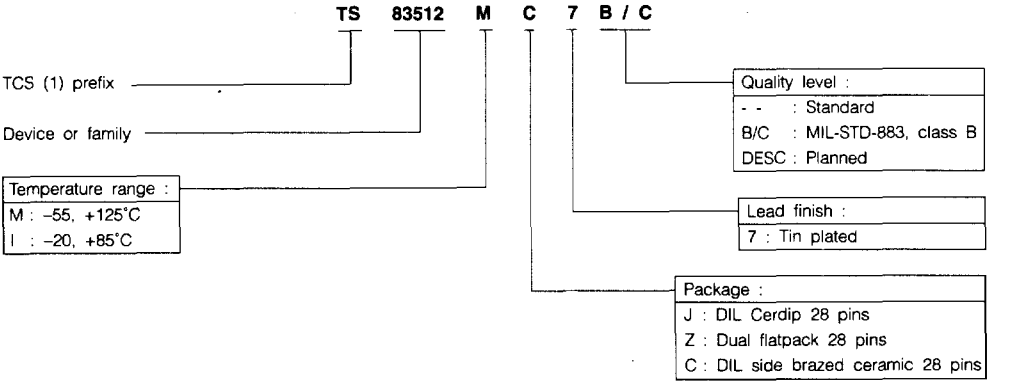
Qualification lot package : DIL 28

Back side potential : V_{EE}

ORDERING INFORMATION

Package device

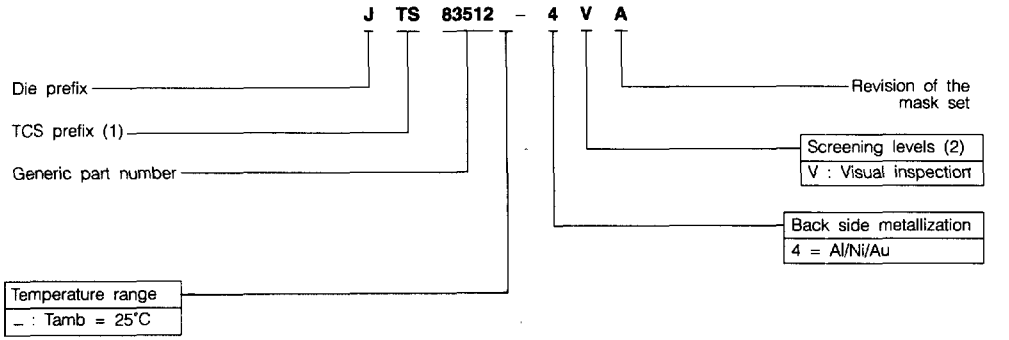
General



Detailled ordering information

Part number	Temperature range (T_C)	Package
TS83512IC7	– 20°C to + 85°C	DIL Ceramic 28
TS83512IZ8	– 20°C to + 85°C	Dual FP 28*
TS83512MC7	– 55°C to + 125°C	DIL Ceramic 28
TS83512MC7B/C	– 55°C to + 125°C	DIL Ceramic 28
* Package under consideration.		

Die form



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of other screening contact your TCS sale office.