

Standard Products

ACT5028B 16-Bit Monolithic Tracking Rad Tolerant Resolver-To-Digital Converter

www.aeroflex.com/RDC

April 16, 2010



FEATURES

- ❑ Radiation performance
 - Total dose: 1 Mrads(Si), Dose rate = 50 - 300 rads(Si)/s
 - SEL: Immune up to 100 MeV-cm²/mg
- ❑ +5VDC power only
- ❑ Programmable: By using a few non critical external resistors and capacitors
 - Resolution: 10, 12, 14 or 16 bit resolution
 - Bandwidth
 - Tracking rate
- ❑ Low power: +5V @ 20 mA typ
- ❑ 45 to 30,000 Hz carrier frequency range
- ❑ Accuracy to 5.3 Arc Minutes
- ❑ Differential instrument amplifiers resolver input
- ❑ -55° to +125°C operating temperature
- ❑ Digital interface logic voltage of 3.3V to 5V
- ❑ Designed for aerospace and high reliability space applications
- ❑ Packaging – Hermetic
 - 52 Pin Ceramic QUAD flat package (CQFP), .956" SQ x .10" Ht max
 - Weight: 5.0g max
- ❑ Evaluation board available for test and evaluation. See Aeroflex Application note AN5028-1
- ❑ Available on DSCC SMD 5962-04235

NOTE: Aeroflex Plainview does not currently have a DSCC Certified Radiation Hardened Assurance Program

APPLICATIONS

This single chip Resolver-to-Digital Converter (RDC) is used in shaft angle control systems, and is suitable for space or other radiation environments that require >1MRad (Si) total dose tolerance. The part is latchup free in heavy ion environments (e.g., geosynchronous orbits) and is estimated to experience SEU induced errors of less than 15 minutes of arc at a rate of 1 per device per 2 years when operating dynamically.

THEORY OF OPERATION

The ACT5028B converter is a single CMOS Type II tracking resolver to digital converter monolithic chip. It is implemented using precision analog circuitry and digital logic. For flexibility, the converter bandwidth, dynamics and velocity scaling are externally set with passive components. Refer to Figure 1, ACT5028B Block Diagram.

The converter is powered from +5VDC. Analog signals are referenced to signal ground, which is nominally VCC/2. The converter consists of three main sections; the Analog Control Transformer (CT), the Analog Error Processor (EP) and the Digital Logic Interface.

The CT has two analog resolver inputs (Sin and Cos) that are buffered by high impedance input instrumentation type amplifiers and the 16 bit digital word which represents the output digital angle. The CT performs the ratiometric trigonometric computation of:

$$\sin(A) \sin(wt) \cos(B) - \cos(A) \sin(wt) \sin(B) = \sin(A-B) \sin(wt)$$

Utilizing amplifiers, switches, logic and resistors in precision ratios. "A" represents the resolver angle, "B" represents the digital angle and sin(wt) represents the resolver reference carrier frequency.

The Error Processor is configured as a critically damped Type II loop. The AC error, $\sin(A-B) \sin(wt)$ is full wave demodulated using the reference squared off as its drive. This DC error is integrated in an analog integrator yielding a velocity voltage which in turn drives a Voltage Controlled Oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II loop. A lead is inserted to stabilize the loop and a lag is inserted at a higher frequency to attenuate the carrier frequency ripple. The error processor drives the 16 bit digital output until it nulls out. Then angle "A" = "B". The digital output equals angle input to the accuracy of the precision control transformer. The various error processor settings are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

The digital logic interface has a separate power line, VLI/O that sets the interface logic 1 level. It can be set anywhere from +3V to the +5V power supply.

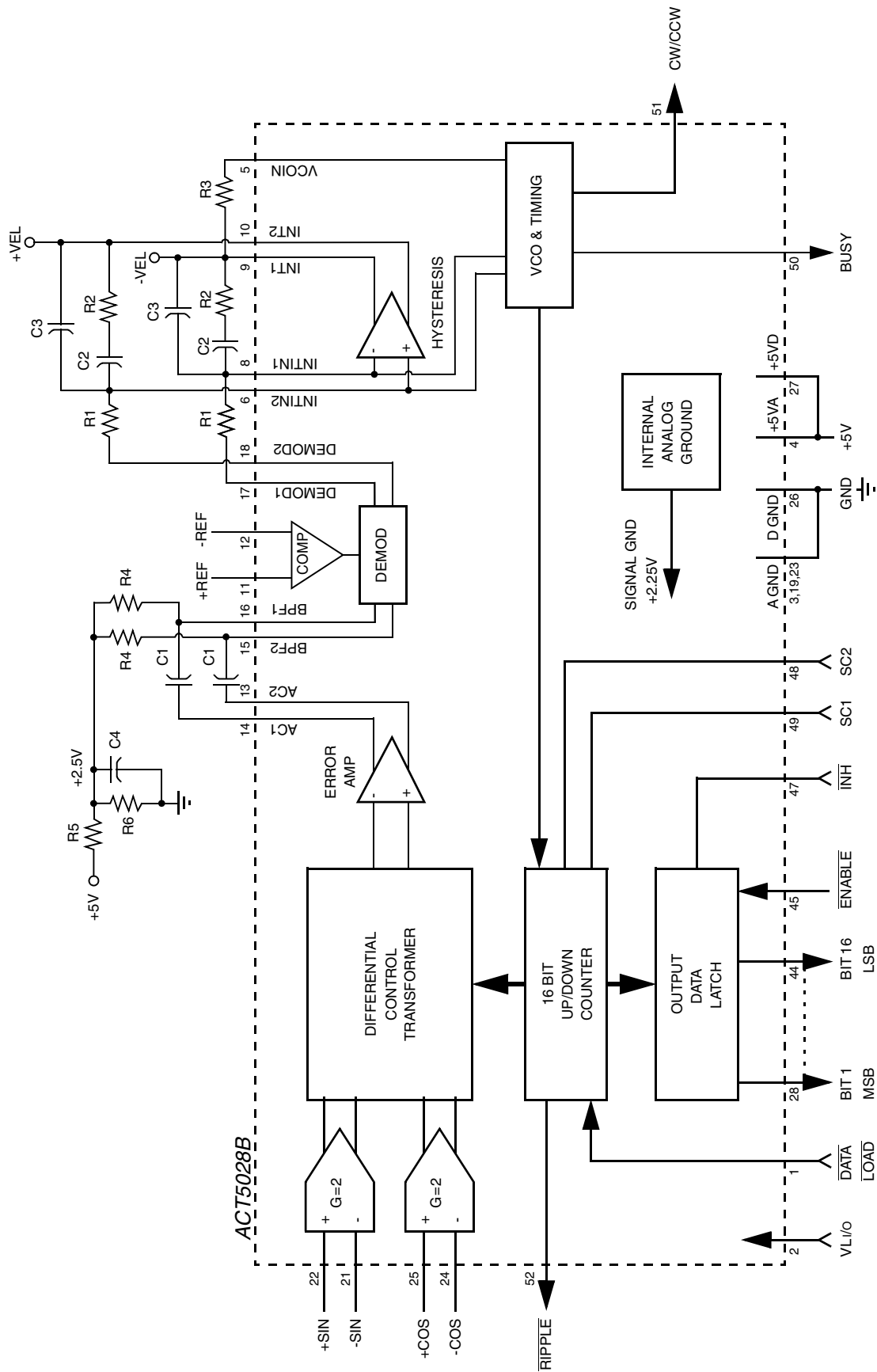


FIGURE 1 – ACT5028B BLOCK DIAGRAM

PIN DESCRIPTIONS

SIGNAL	DIRECTION	PIN	SIGNAL DESCRIPTION															
+SIN -SIN	INPUT	22 21	Analog Sine input from Synchro or Resolver. 1.3Vrms nominal															
+COS -COS	INPUT	25 24	Analog Cosine input from Synchro or Resolver. 1.3Vrms nominal															
+REF -REF	INPUT	11 12	Analog Reference input															
BIT 1 (MSB) BIT 2 BIT 3 BIT 4 BIT 5 BIT 6 BIT 7 BIT 8 BIT 9 BIT 10 BIT 11 BIT 12 BIT 13 BIT 14 BIT 15 BIT 16 (LSB)	BIDIR	28 29 30 31 32 34 35 36 37 38 39 40 41 42 43 44	Digital angle data. Parallel format. Natural binary positive logic. Bit 1, most significant bit = 180°, Bit 2 = 90°, Bit 3 = 45° and so on. In the 10 bit mode, Bit 10 is the LSB. Bits 11-16 are 0s. In the 12 bit mode, Bit 12 is the LSB. Bits 13-16 are 0s. In the 14 bit mode, Bit 14 is the LSB. Bits 15-16 are 0s. In the 16 bit mode, Bit 16 is the LSB.															
SC1 SC2	INPUT	49 48	Digital input. Sets the resolution. <table><tr><th>SC1</th><th>SC2</th><th>Resolution</th></tr><tr><td>0</td><td>0</td><td>10 bit</td></tr><tr><td>0</td><td>1</td><td>12 bit</td></tr><tr><td>1</td><td>0</td><td>14 bit</td></tr><tr><td>1</td><td>1</td><td>16 bit</td></tr></table>	SC1	SC2	Resolution	0	0	10 bit	0	1	12 bit	1	0	14 bit	1	1	16 bit
SC1	SC2	Resolution																
0	0	10 bit																
0	1	12 bit																
1	0	14 bit																
1	1	16 bit																
ENABLE*	INPUT	45	Logic 0 enables digital angle output. Otherwise it is high impedance.															
INH*	INPUT	47	Logic 0 freezes the digital angle output so that it can be safely read.															
DATALOAD*	INPUT	1	Logic 0 enables the digital angle lines to be inputs to preset the angle. Logic 1 is for normal digital angle output.															
BUSY	OUTPUT	50	A logic 1 pulse when the digital angle changes by 1 LSB.															
CW/CCW	OUTPUT	51	For turns counting. Logic 1 = counting up (CW), logic 0 = counting down (CCW).															
RIPPLE*	OUTPUT	52	Ripple clock for turns counting. A logic 0 pulse = a 0° transition in either direction.															
AC1 AC2	OUTPUT	14 13	Differential AC error output															
BPF1 BPF2	INPUT	16 15	Differential AC error input to demodulator															
DEM0D1 DEM0D2	OUTPUT	17 18	Differential DC error output															
INTIN1 INTIN2	INPUT	8 6	Differential DC input to differential velocity integrator															
INT1 INT 2	OUTPUT	9 10	Differential velocity output															
VCOIN	INPUT	5	Input to Voltage Controlled Oscillator															
VCC VDD	POWER	4 27	Analog Power In Digital Power In															
A GND D GND	POWER	3, 19, 23 26	Analog Power ground Digital Power ground															
VLi/o	POWER	2	Digital input/output DC power supply. Sets logic 1 level. +3V to +5V															

* Indicates Active Low Signal

ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUE
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Positive Power Supply Voltage (VCC = VDD)	-0.5 V to +7.0 V
Analog Output Current (Output Shorted to GND)	32 mA Max
Digital Output Current (Output Shorted to GND)	18.6 mA Max
Analog Input Voltage Range	-0.3 V to + (VCC +.3 V)
Digital Input Voltage Range	-0.3 V to + (VDD +.3 V)
Thermal Resistance θ_{JC} Specification	1.25°C/W
Maximum Junction Temperature	135°C

* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only; functional operation beyond these operating conditions is not recommended and extended exposure beyond these operating conditions may effect device reliability.

OPERATING CONDITIONS

(TA = -55°C to +125°C)

POWER SUPPLY	PARAMETER	MIN	TYP	MAX	UNIT
VDD = VCC	Operating Voltage	4.5	5	5.5	VDC
IDD + ICC	Operating Current	-	20	35	mA
VL/I/O	Interface Voltage	3	3.3, 5	5.5	VDC

ELECTRICAL CHARACTERISTICS ^{2,5,6}

(TA = -55°C to +125°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy ⁴	Add 1 LSB for total Error	-	±2	± 5	Minutes
Repeatability		-	-	1	LSB
Resolution per LSB	10 Bit Mode	0.35	-	-	Degrees
		21.1	-	-	Minutes
	12 Bit Mode	0.09	-	-	Degrees
		5.27	-	-	Minutes
	14 Bit Mode	0.022	-	-	Degrees
		1.32	-	-	Minutes
	16 Bit Mode	0.0055	-	-	Degrees
		0.33	-	-	Minutes
Max Tracking Rate	<u>SC1</u> <u>SC2</u> <u>Bits Used</u>				
10 Bit Mode	0 0 B1 - B10	1024	-	-	RPS
12 Bit Mode	0 1 B1 - B12	256	-	-	RPS
14 Bit Mode	1 0 B1 - B14	64	-	-	RPS
16 Bit Mode	1 1 B1 - B16	16	-	-	RPS
VCO Frequency		1.05	-	-	MHz

ELECTRICAL SPECIFICATIONS^{2,5,6}
(TA = -55°C to +125°C)

ANALOG SIGNAL INPUTS	SYM	PARAMETER	MIN	TYP	MAX	UNITS
SIN, COS, REF, VCOIN, INTIN1, INTIN2, BPF1, BPF2	VSIN, VCOS, VREF	Voltage measurement made between ± inputs	1.0	1.3	1.5	VRMS
	FREF	Frequency ¹	45	-	30K	Hz
		Impedance	2.5	-	-	MΩ
		Capacitance ³	-	5	15	pF
		DC Bias on -Sin, -Cos	-	VCC/2	-	VDC
		Bias Current				
		+25°C	-100	-	+100	nA
+125°C	-1000	-	+1000	nA		
DIGITAL INPUTS						
ENABLE, DATALOAD SC2, SC1, INH See Note 3	VIL	Logic Low ³	-	-	0.8	VDC
	VIH	Logic High ³	2	-	-	VDC
	IIN	Leakage Current				
		+25°C	-200	-	+200	nA
		+125°C	-2000	-	+2000	nA
		Impedance	2.5	-	-	MΩ
Capacitance ³		-	5	15	pF	
DIGITAL OUTPUTS						
BUSY, RIPPLE CW/CCW	VOL	Logic Low @ 1.6mA	-	-	0.3	VDC
	VOH	Logic High @ -1.6mA	VLi/O - .8	-	-	VDC
DIGITAL I/O						
B1 - B16 ⁷	VIL	Logic Low ³	-	-	0.8	VDC
	VIH	Logic High ³	2	-	-	VDC
	VOL	Logic Low @ 1.6mA	-	-	0.3	VDC
	VOH	Logic High @ -1.6mA	VLi/O - .8	-	-	VDC
	IIN	Leakage Current				
		+25°C	-200	-	+200	nA
		+125°C	-2000	-	+2000	nA
	IZ	High-Z Leakage Current ³				
+25°C		-200	-	+200	nA	
+125°C		-2000	-	+2000	nA	

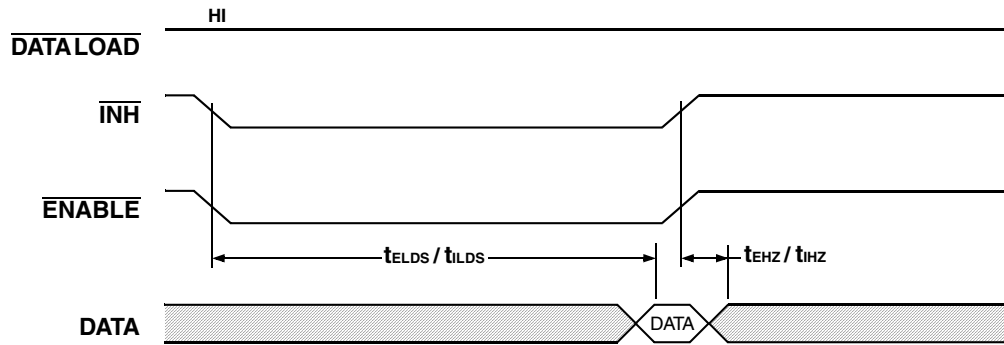
TIMING SPECIFICATIONS ⁶

DIGITAL OUTPUT	SYM	COMMENTS	MIN	TYP ²	MAX	UNITS
Busy	t _{LH}	Rise Time	-	20	85	ns
	t _{HL}	Fall Time	-	20	85	ns
CW/CCW, Ripple, B1- B16	t _{LH}	Rise Time	-	45	100	ns
	t _{HL}	Fall Time	-	45	100	ns
Busy Pulse Width	t _{BPW}		300	400	600	ns
Busy to Data Stable ³	t _{BDS}	Enable = Low	-	-	350	ns
Ripple Pulse Width	t _{RPW}		160	200	300	ns
Busy to Ripple ³	t _{BR}		-	100	150	ns
READ DATA ³ ($\overline{\text{Enable}}$ & $\overline{\text{INH}}$ would normally be tied together, $\overline{\text{Data Load}}$ = Logic Hi)						
$\overline{\text{Enable}}$ Low to Data Stable	t _{ELDS}		-	-	70	ns
$\overline{\text{Enable}}$ High to Data Hi-Z	t _{EHZ}		-	-	70	ns
$\overline{\text{INH}}$ Low to Data Stable	t _{ILDS}		-	-	400	ns
$\overline{\text{INH}}$ High to Data Change	t _{IHZ}		-	-	150	ns
WRITING DATA ³ ($\overline{\text{Enable}}$ & $\overline{\text{INH}}$ = Logic Hi)						
Data Load Pulse Width	t _{DLPW}	Transparent Trailing Edge Latch	200	-	-	ns
Data Setup to Data Load	t _{WDS}		60	-	-	ns
Data Hold	t _{WDH}		10	-	-	ns

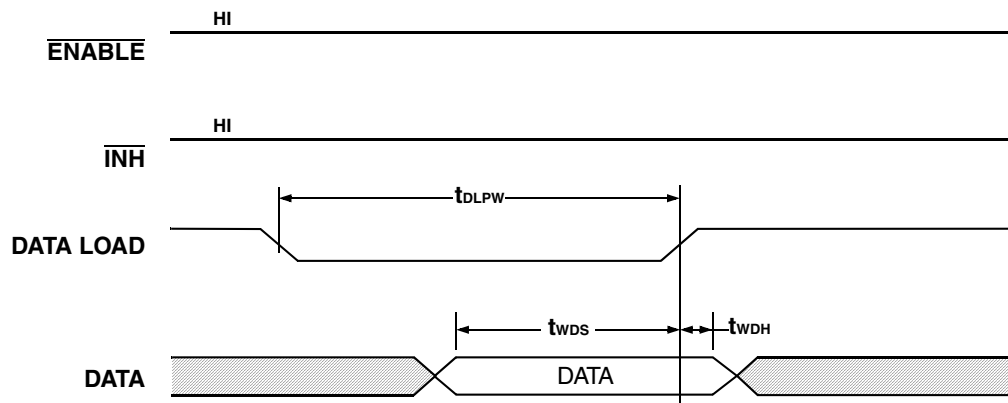
Notes

- @ 10 Bits, FREF > 4 x BWCL
@ 12 Bits, FREF > 8 x BWCL
@ 14 Bits, FREF > 12 x BWCL
@ 16 Bits, FREF > 16 x BWCL
- All typical values are measured at +25°C.
- Characteristics are guaranteed by design, not production tested.
- Accuracy apply over the full operating Power Supply voltage range, Full operating Temperature range, Reference Frequency range, 10% Signal Amplitude variation and 10% Reference Harmonic distortion.
- For ESD protection the ACT5028B features limiting resistors in series with diodes. Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation.
- All testing at nominal voltage.
- All unused inputs shall be tied to Ground. Bit 1 is always the MSB.

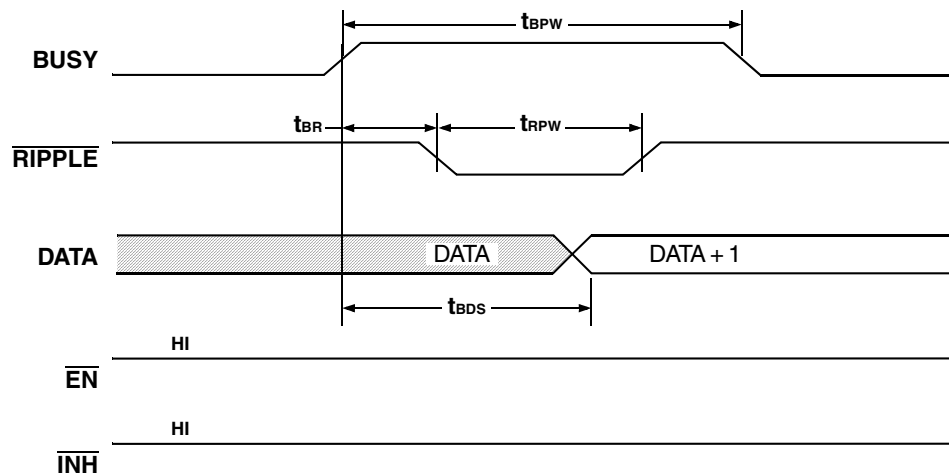
READ CYCLE



WRITE CYCLE



BUSY TIMING



ACT5028B TIMING DIAGRAMS

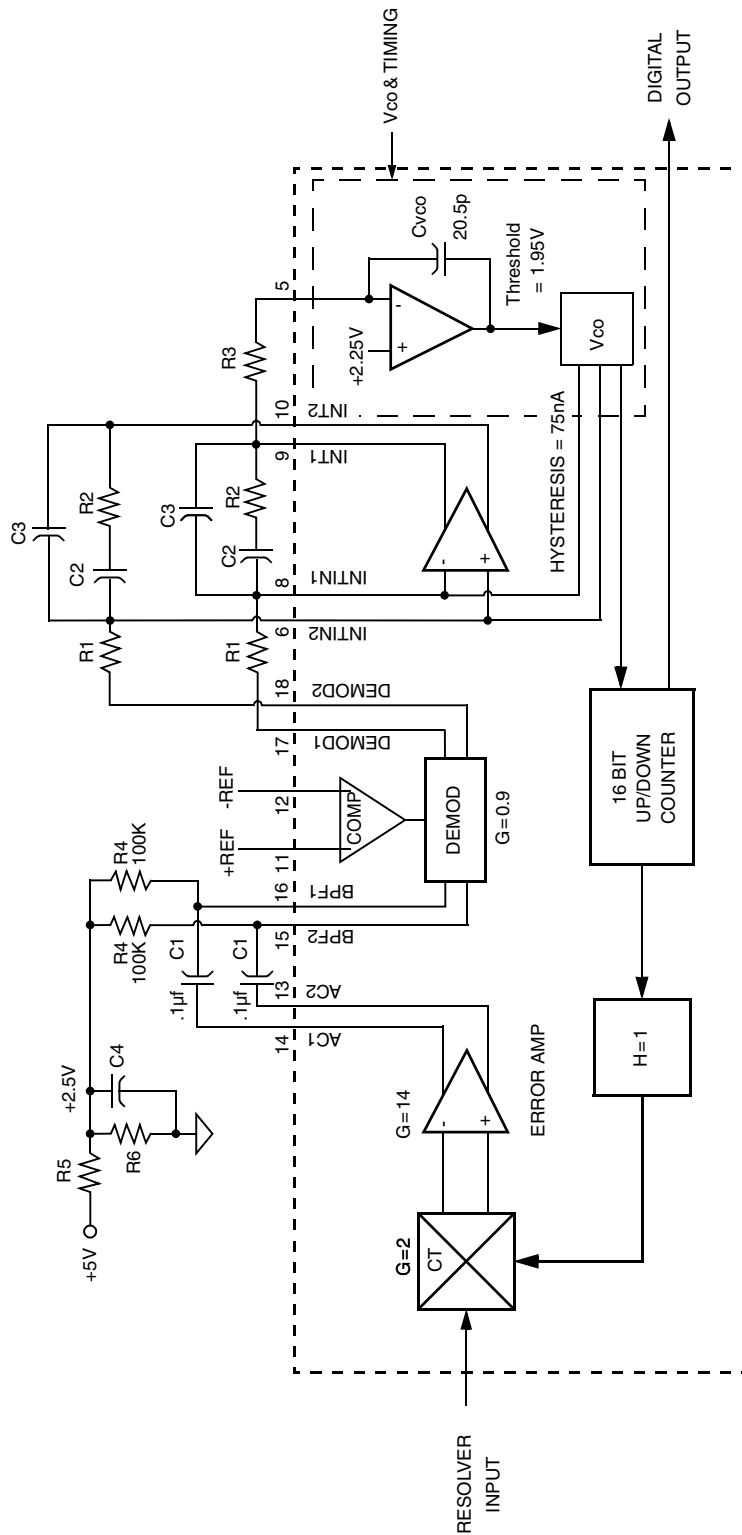


FIGURE 2 – ACT5028B FUNCTIONAL BLOCK DIAGRAM

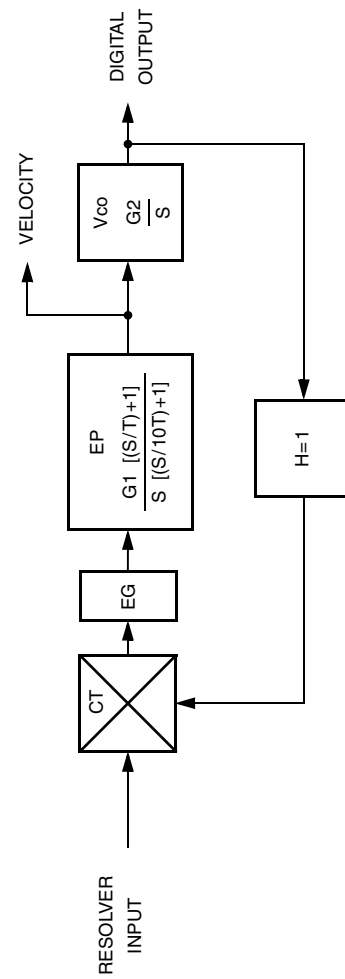


FIGURE 3 – ACT5028B TRANSFER FUNCTION DIAGRAM

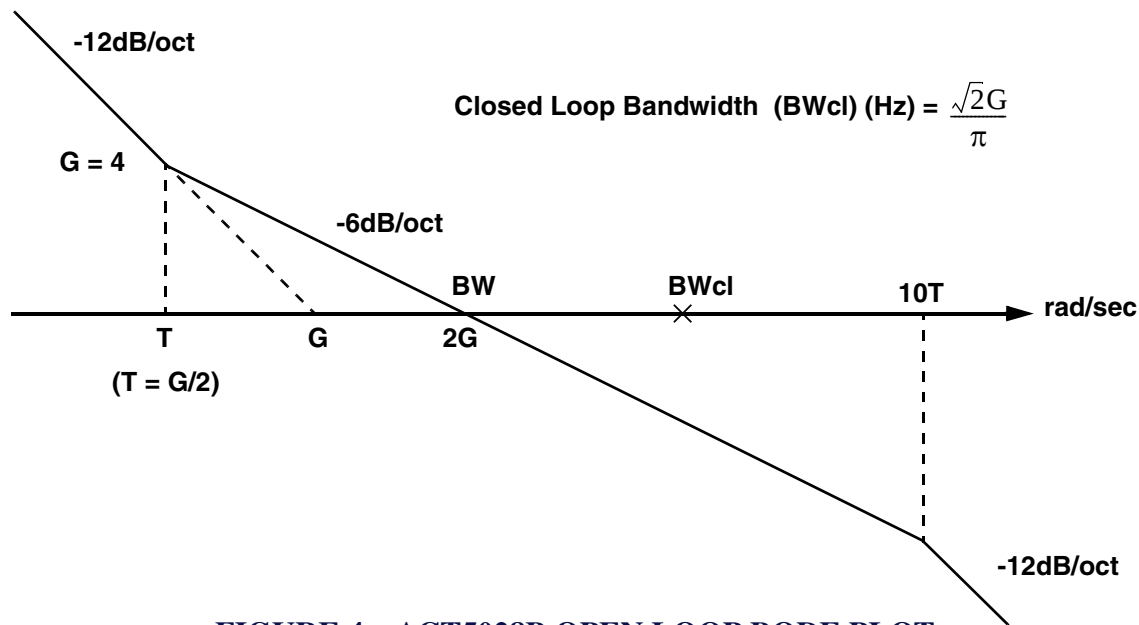


FIGURE 4 – ACT5028B OPEN LOOP BODE PLOT

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram, Transfer Function Diagram and Bode plots, as shown in Figures 2, 3 and 4.

PROCEDURE FOR SELECTING RDC BANDWIDTH COMPONENTS *

Input: Carrier Frequency (Fc) in Hz [47 to 30,000 Hz]

Input: Nominal Resolver Input Level in Vrms [1Vrms min. to 1.5Vrms max.]

Input: Resolution in bits; 10, 12, 14 or 16 bits

Input: Closed Loop Bandwidth (BWcl) in Hz

[10 bit; BWcl = Fc/4 max.]

[12 bit; BWcl = Fc/8 max.]

[14 bit; BWcl = Fc/12 max.]

[16 bit; BWcl = Fc/16 max.]

Input: Maximum Tracking Rate in RPS
(RPS = rotations per second)

[16 bit; 16 RPS max.]

[14 bit; 64 RPS max.]

[12 bit; 256 RPS max.]

[10 bit; 1024 RPS max.]

Input: Hysteresis in LSBs. Recommended is 1 LSB for 16 & 14 bits and 0.7 LSBs for 12 & 10 bits.

EG = Nominal Resolver Input Level • .0027 [16 bit] or

EG = Nominal Resolver Input Level • .011 [14 bit] or

EG = Nominal Resolver Input Level • .043 [12 bit] or

EG = Nominal Resolver Input Level • .17 [10 bit]

$G = 2.22 \cdot BW_{cl}$

$G^2 = EG \cdot 0.45 \cdot G1 \cdot G2$

Hysteresis recommended values

HYS = 0.7 [10 & 12 bit] or

HYS = 1 [14 & 16 bit] or

$R1_{(ohms)} = 6 \cdot 10^6 \cdot EG \cdot HYS$

$G2 = \text{Maximum Tracking Rate} \cdot 2^{15}$ [16 bit] or

$G2 = \text{Maximum Tracking Rate} \cdot 2^{13}$ [14 bit] or

$G2 = \text{Maximum Tracking Rate} \cdot 2^{11}$ [12 bit] or

$G2 = \text{Maximum Tracking Rate} \cdot 2^9$ [10 bit]

$R3_{(ohms)} = (25 \cdot 10^9) / G2$

$G1 = G^2 / (EG \cdot .45 \cdot G2)$

$$C2_{(\text{farads})} = 1/(G1 \cdot R1)$$

$$C3_{(\text{farads})} = C2/10$$

$$R2_{(\text{ohms})} = 2/(G \cdot C2)$$

ACT5028B EXAMPLE CALCULATIONS

Carrier Frequency = 800 Hz

Nominal Resolver Input Level = 1.3Vrms

Resolution = 14 bits

Closed Loop Bandwidth (BWcl) = 20 Hz

Maximum Tracking Rate in RPS = 1

Hysteresis = 1 LSB

$$EG = \text{Nominal Resolver Input Level} \cdot .011 \quad [14 \text{ bit}] = 1.3 \cdot .011 = .014$$

$$G = 2.22 \cdot BWcl = 2.22 \cdot 20 = 44.4$$

$$HYS = 1 \quad [14 \text{ bit}]$$

$$R1_{(\text{ohms})} = 6 \cdot 10^6 \cdot EG \cdot HYS = 6 \cdot 10^6 \cdot .014 \cdot 1 = 84K. \text{ Use closest standard resistor} = 84.5K \quad 1\%$$

$$G2 = \text{Maximum Tracking Rate} \cdot 2^{13} = 8192 \quad [2^{13} \text{ for 14 bits}]$$

$$R3_{(\text{ohms})} = (25 \cdot 10^9)/G2 = (25 \cdot 10^9)/8192 = 3,050K. \text{ Use closest standard resistor} = 3.01M \quad 1\% \text{ or } 3M \quad 5\%$$

$$G^2 = EG \cdot 0.45 \cdot G1 \cdot G2$$

$$G1 = G^2/(EG \cdot .45 \cdot G2) = 44.4^2/((.014 \cdot .45 \cdot 8192)) = 38.2$$

$$C2_{(\text{farads})} = 1/(G1 \cdot R1) = 1/(38.2 \cdot 84.5K) = .31\mu F. \text{ Use closest standard capacitor} = .33\mu F \quad 10\%$$

$$C3 = C2/10_{(\text{farads})} = C2/10 = .33\mu/10 = .033\mu F$$

$$R2_{(\text{ohms})} = 2/(G \cdot C2) = 2/(44.4 \cdot .33\mu) = 136.5K. \text{ Use closest standard resistor} = 137K \quad 1\%$$

SIGNAL AND REFERENCE INPUT CONDITIONING

Inputs to the converter should be 1.3 Vrms nominal, resolver format referenced to Vcc/2 nominal Figure 5 shows various input configurations.

REFERENCE CONDITIONING

Most resolvers have a LEADING input to output phase shift. A simple C-R leading phase shift network (Figure 5 – Reference Conditioning) from the resolver reference to the RDC's reference input will provide the compensating phase shift required to bring the signals in phase. If the resolver has a LAGGING input to output phase shift an R-C lagging phase shift network (low pass network) would be required.

Note the C-R phase lead circuit on the input to the Demodulator (BPF1 and BPF2) in Figure 2 should be considered when calculating the total system phase compensation.

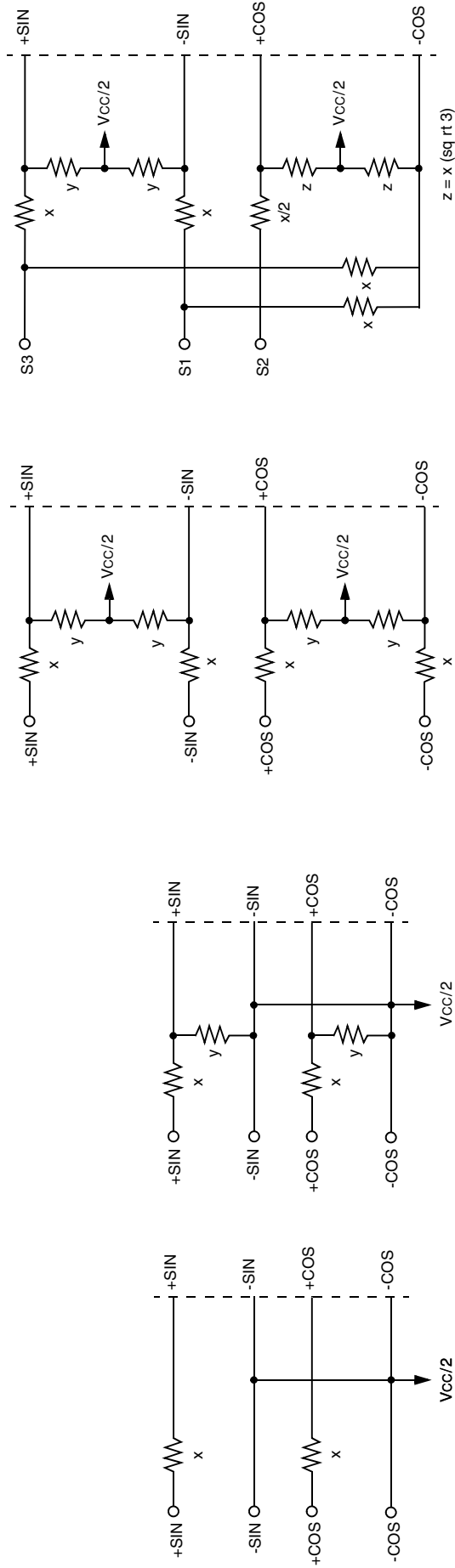
The formula for calculating the phase shift network is as follows:

$$\text{Phase angle} = \text{ArcTan} \frac{1}{\frac{6.28 \times (R7 + R8) \times C}{F_{REF}}}$$

Select a convenient capacitor value and perform the following calculation to determine the proper resistor value.

$$R = \frac{1}{(\text{Tan (Phase Angle)}) \times F_{REF} \times 6.28 \times C}$$

*** Software Program SW5028-2 available at Aeroflex WEB site.**

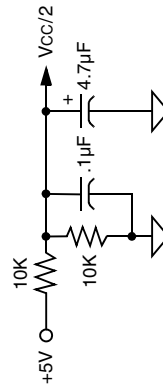


DIRECT RESOLVER

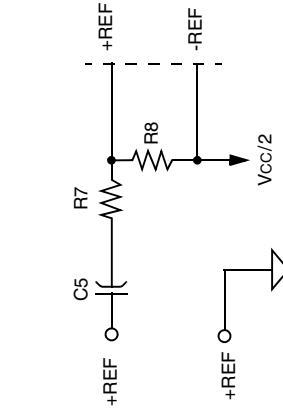
SINGLE ENDED RESOLVER CONDITIONING

DIFFERENTIAL RESOLVER CONDITIONING

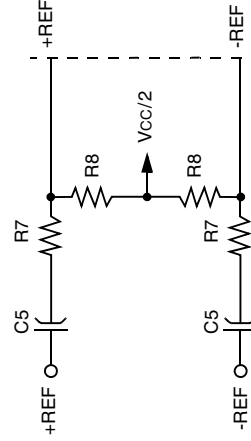
SYNCHRO CONDITIONING



2.5VDC



SINGLE ENDED REFERENCE CONDITIONING



DIFFERENTIAL REFERENCE CONDITIONING (FLOATING REFERENCE)

FIGURE 5 – ACT5028B RESOLVER, SYNCHRO AND REFERENCE INPUT CONFIGURATIONS

Reading the ACT 5028B

The Busy signal is asynchronous to the Read signal created by the interface circuit that reads it. Because of the asynchronous nature of the system (inherent with other Resolver to Digital Converters) the designer must be careful when reading the digital interface.

The implementation of reading the RDC is accomplished in one of two ways, using a CPU/MPU or using an FPGA. The best method for reading the counter may also depend on the rep rate of the counter clock that can vary from 0 to 1 μ S.

The Busy pulse is instrumental in reading stable data from the ACT5028. The Busy pulse will be present for the following two situations:

- 1) When ever data is incremented or decremented in the RDC counter.
- 2) Directly after the trailing positive going edge of /INH (see A within example 5 timing diagram).

Based on 1 above there are many methods that can be implemented to synchronize the reading of data from the ACT5028, below are a few examples:

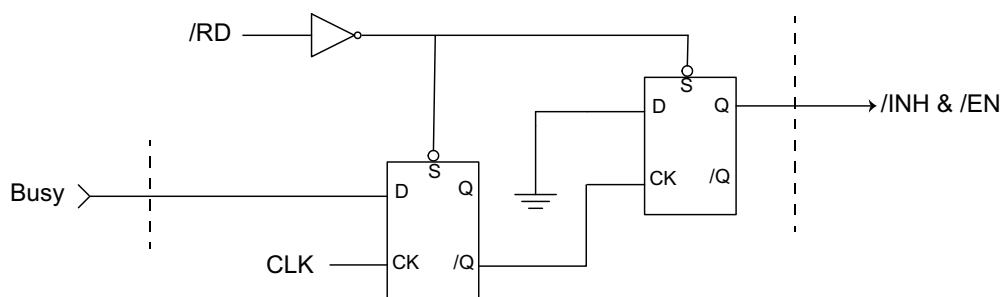
Example 1: If the only time a read will occur is after the RDC has stopped (0 rps) there will be no Busy signal to contend with.

Example 2: Knowing the Busy rep rate an Interrupt to a CPU or Logic can be developed from the Busy pulse for the system to Read the RDC chip as long as the read is guaranteed to occur prior to the next Busy pulse.

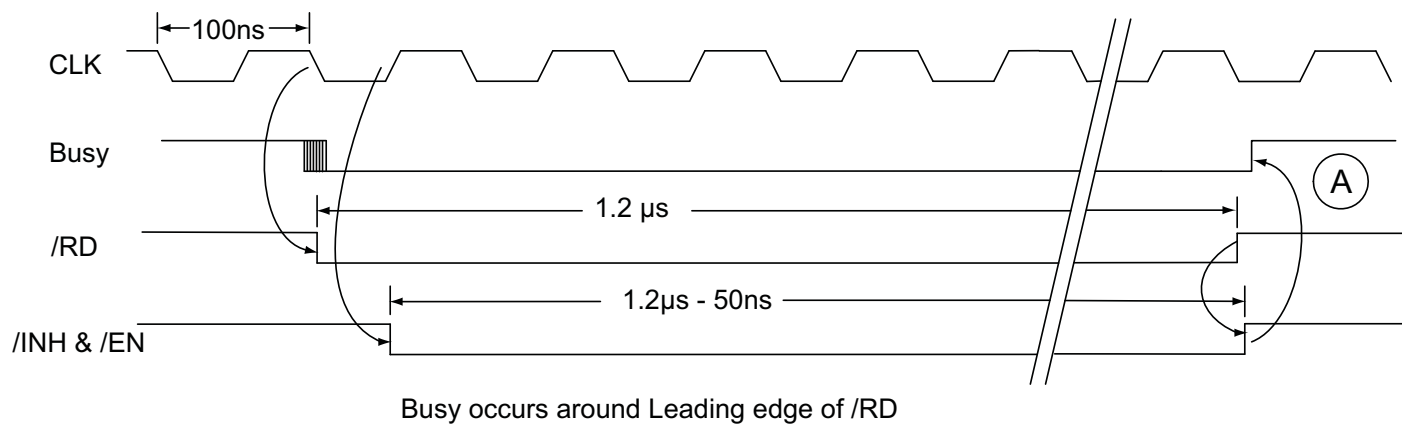
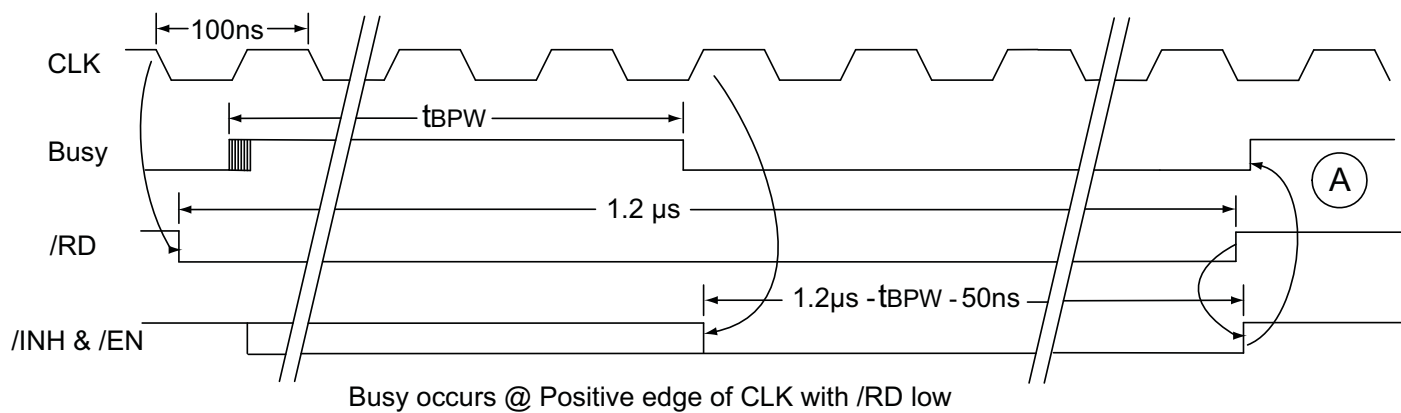
Example 3: As long as the resolver is rotating the Busy Pulse can be used to indicate stable data to be sampled on leading or trailing edge.

Example 4: Ignore Busy and perform two reads back to back and compare, if they are equal you have good data. The designer should be aware of the rep rate of Busy which is equal to the clock rate of the counter. In most cases the angular velocity is < 3 rps in which case with a 16 bit counter rep rate would be $(1 / 2^{16} * 3) 5\mu$ S. In this situation the reads would like to be within 5 μ s of each other and the LSB would be ignored. Although this method would be easier to implement with a CPU it could also be done in an FPGA.

Example 5: The circuit below ignores the Busy signal but insures sampling of stable data. The clock should be a least 10MHz, the /RD pulse should be a minimum of 1.2 μ s (to insure minimum /INH pulse width of 400ns), the sampling of data should be taken on the rising edge of the signal /RD. The /RD signal is synced up with the CLK such that the sampling on the D latch occurs on the opposite edge of the /RD transition.



EXAMPLE 5 CIRCUIT



EXAMPLE 5 CIRCUIT TIMING WAVEFORMS

TABLE I – ACT5028B PIN OUT DESCRIPTIONS (CQFP PACKAGE)

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	$\overline{\text{DATA LOAD}}$	19	AGND	37	BIT 9
2	VL I/O	20	N/C	38	BIT 10
3	AGND	21	-SIN	39	BIT 11
4	A +5V	22	+SIN	40	BIT 12
5	VCOIN	23	AGND	41	BIT 13
6	INTIN2	24	-COS	42	BIT 14
7	N/C	25	+COS	43	BIT 15
8	INTIN1	26	D GND	44	BIT 16 (LSB)
9	INT1	27	D +5V	45	$\overline{\text{ENABLE}}$
10	INT2	28	BIT 1 (MSB)	46	N/C
11	+REF	29	BIT 2	47	$\overline{\text{INH}}$
12	-REF	30	BIT 3	48	SC2
13	AC2	31	BIT 4	49	SC1
14	AC1	32	BIT 5	50	BUSY
15	BPF2	33	N/C	51	CW/CCW
16	BPF1	34	BIT 6	52	$\overline{\text{RIPPLE}}$
17	DEM0D1	35	BIT 7		
18	DEM0D2	36	BIT 8		

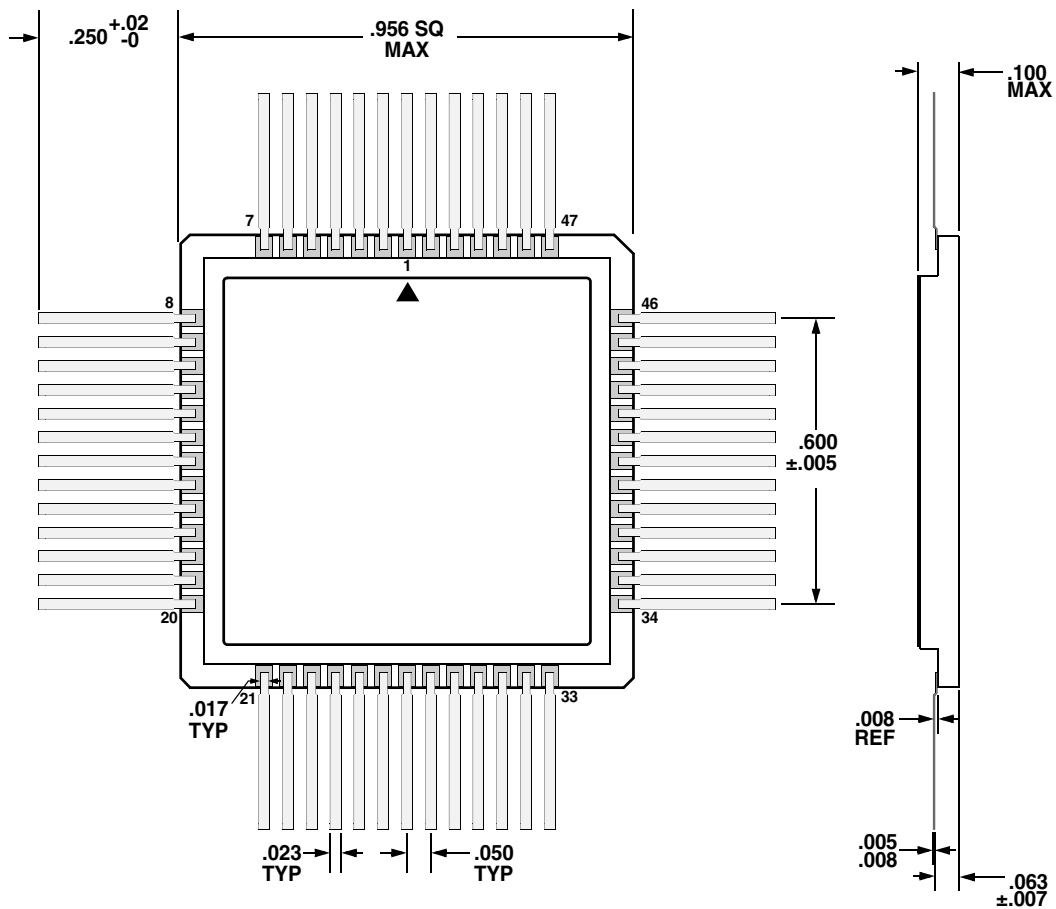


FIGURE 6 – 52 PIN CERAMIC QUAD FLAT PACKAGE (CQFP) OUTLINE

This Errata information represents the known bugs, anomalies, and work-arounds for the ACT5028 Resolver to Digital Converter

DESCRIPTION OF ANOMALIES:

Anomaly #1: Instability at 360° and 180° Input Angles

Anomaly #2: Correcting for the Integral Nonlinearity Error found in Revision B Silicon

Anomaly #3: Precautionary note when power is first applied.

EFFECTED PARTS:

Model	Anomaly	Anomaly	Anomaly
ACT5028-2-1-X	1	2a	3
ACT5028-2-2-X	1	2b	3

ANOMALY #1

PROBLEM DESCRIPTION:

This problem occurs in the 16 Bit mode when rotating in the clockwise (CW) direction and has been observed on 100% of the parts tested at 25°C. It occurs 100% of the time at 360° and approximately 76% at 180°. At 360° the problem occurs when the counter passes from FFFF to 0000 then reverse rotation (CCW) back to FFFF. At 180° the problem occurs when the counter passes from 7FFF to 8000 then reverse rotation (CCW) back to 7FFF.

Two different failure modes have been observed:

- 1) The output latch locks to a value with the MSB inverted giving the indication that the RDC chip is 180° out of phase, the RDC chip exhibits zero error. This condition remains indefinitely until the resolver rotates in either direction by one count. At which time the RDC chip responds to the 180° error which takes less than 150ms to correct.
- 2) The RDC chip sees an immediate error of 180° and begins to correct for this error which takes less than 150ms.

In some cases it has been observed that the MSB is OK but the next bit gets inverted which provides a 90° error. In this case the time required for the RDC chip to correct its self is less than 75 ms.

RECOMMENDED ACTIONS:

- 1) Use the 10 or 12 Bit mode where this problem doesn't exist. Note: The 14 bit mode will also work using the Aeroflex part numbers over the temperature ranges shown below:

ACT5028-2-1-S	-55°C to +125°C
ACT5028-2-2-S	-40°C to +125°C
- 2) Insure a hysteresis of at least one bit to prevent this anomaly when rotating very slowly.
- 3) Avoid reversing direction at 360° and 180° when rotating in the CW direction.
- 4) If the resolver stops within two counts of 360° or 180° wait 150ms after motion resumes before reading the RDC output.

ANOMALY #2

PROBLEM DESCRIPTION AND RECOMMENDED ACTION:

This Errata information is to address the constant Integral Nonlinearity (INL) that exists at each angle of the ACT5028B Resolver to Digital Converter (RDC). This error is repeatable from chip to chip and provides a look up Table of offsets that must be added to the output of the Resolver to Digital Converter to get the correct angle.

Figure 7 shows the error in Minutes that exists at 2° increments for the full 360°. Note that the INL error from 0° to 180° is basically the same as the error between 180° and 360°. Table II has the angle and correction factor (in Minutes) that must be added to zero out the INL error.

A simple calculation can be performed to derive a correction factor for angles that fall between the angles listed in Table II herein.

AL = Larger Angle

AS = Smaller Angle

CL = Correction Factor associated with larger Angle

CS = Correction Factor associated with smaller Angle

NA = New Angle

NCF = New Correction Factor

Formula:

$$\text{NCF} = \text{CS} + (((\text{NA} - \text{AS}) / (\text{AL} - \text{AS})) * (\text{CL} - \text{CS}))$$

Example:

Require the correction factor @ 15°

$$\text{NCF} = 10.17114258 + (((15 - 14) / (16 - 14)) * (11.11376953 - 10.17114258))$$

$$\text{NCF} = 10.17114258 + (((1) / (2)) * .94262695)$$

$$\text{NCF} = 10.17114258 + (.5 * .94262695)$$

$$\text{NCF} = 10.17114258 + .471313475$$

$$\text{NCF} = 10.64245606 \text{ minutes}$$

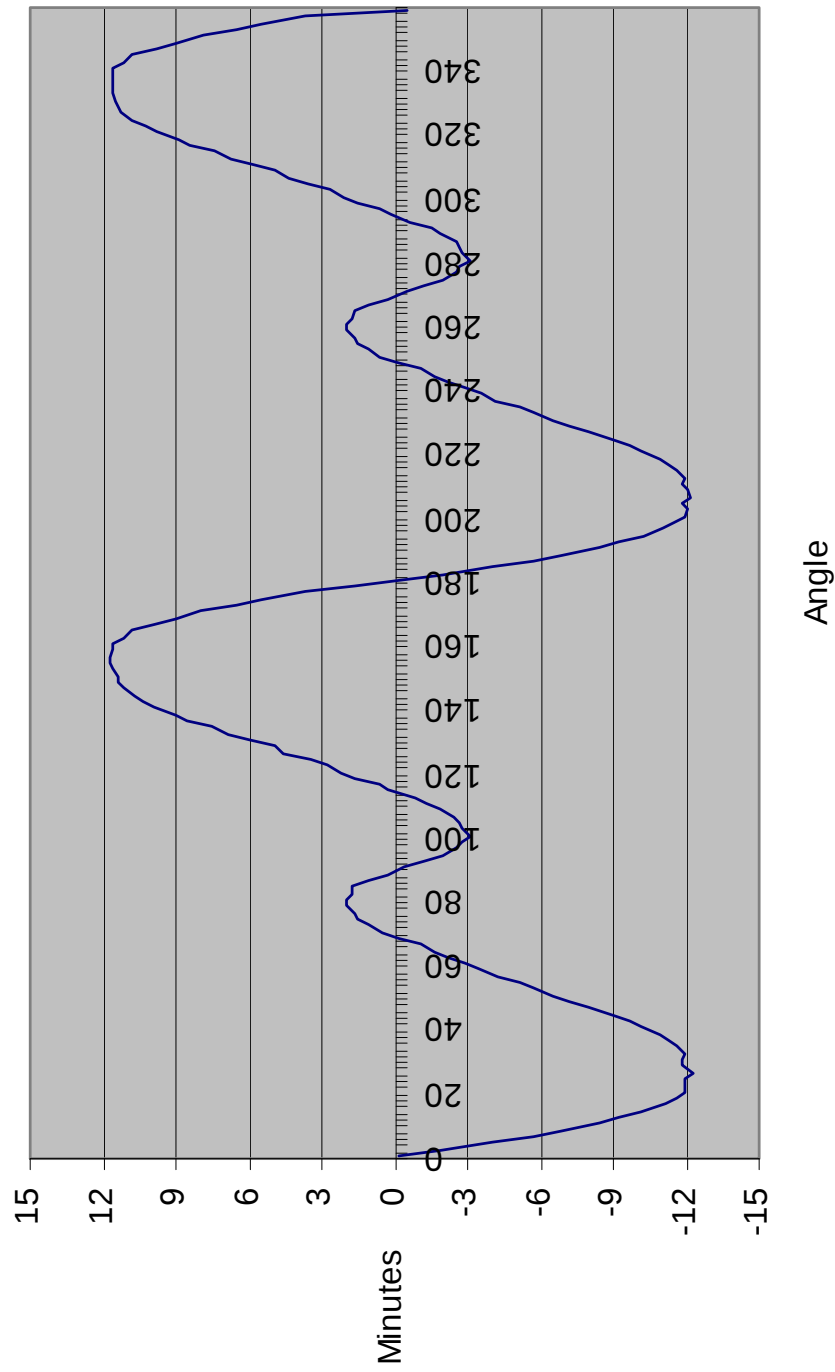


Figure 7 – Anomaly #2a Angle Error Chart

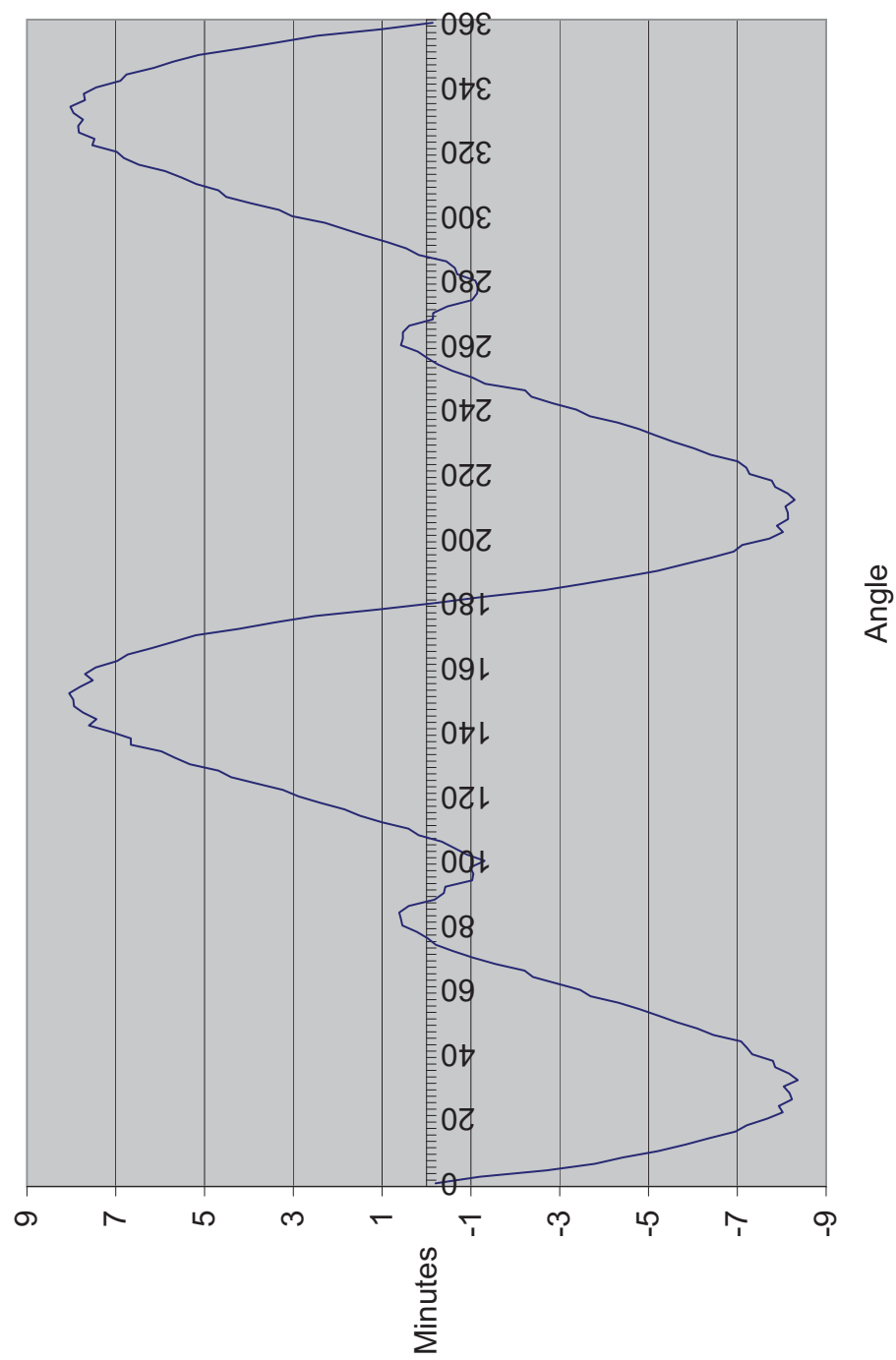


Figure 7 – Anomaly #2b Angle Error Chart

Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor
0	0.125244141	90	0.415283203	180	0.145019531	270	0.474609375
2	1.911621094	92	1.153564453	182	1.997314453	272	1.206298828
4	4.073730469	94	1.977539062	184	3.981445312	274	1.970947266
6	5.715087891	96	2.537841797	186	5.754638672	276	2.577392578
8	6.868652344	98	2.814697266	188	6.822509766	278	2.649902344
10	8.411132812	100	3.071777344	190	8.411132813	280	3.150878906
12	9.241699219	102	2.735595703	192	9.221923828	282	2.794921875
14	10.17114258	104	2.656494141	194	10.19750977	284	2.682861328
16	11.11376953	106	2.478515625	196	11.09399414	286	2.564208984
18	11.54882812	108	1.885253906	198	11.44995117	288	1.858886719
20	11.94433594	110	1.285400391	200	11.97729492	290	1.562255859
22	11.99707031	112	0.837158203	202	12.01025391	292	0.626220703
24	11.91137695	114	-0.243896484	204	11.88500977	294	-0.171386719
26	12.26733398	116	-0.626220703	206	12.19482422	296	-0.652587891
28	11.85205078	118	-1.621582031	208	12.10913086	298	-1.496337891
30	11.77954102	120	-2.168701172	210	11.82568359	300	-2.083007812
32	11.97070312	122	-2.814697266	212	11.92456055	302	-2.649902344
34	11.64770508	124	-3.460693359	214	11.64111328	304	-3.618896484
36	11.26538086	126	-4.548339844	216	11.22583008	306	-4.403320313
38	10.90942383	128	-4.871337891	218	10.89624023	308	-4.95703125
40	10.16455078	130	-5.945800781	220	10.13818359	310	-5.879882812
42	9.683349609	132	-6.842285156	222	9.650390625	312	-6.723632813
44	9.030761719	134	-7.48828125	224	8.984619141	314	-7.461914063
46	8.002441406	136	-8.582519531	226	7.969482422	316	-8.450683594
48	7.237792969	138	-9.043945313	228	7.218017578	318	-8.918701172
50	6.545654297	140	-9.887695313	230	6.492919922	320	-9.755859375
52	5.6953125	142	-10.31616211	232	5.682128906	322	-10.29638672
54	5.174560547	144	-10.73144531	234	5.174560547	324	-10.81054687
56	4.198974609	146	-11.15332031	236	4.185791016	326	-11.29174805
58	3.487060547	148	-11.43017578	238	3.520019531	328	-11.3972168
60	2.939941406	150	-11.32470703	240	2.887207031	330	-11.44995117
62	2.241210938	152	-11.64770508	242	2.181884766	332	-11.57519531
64	1.614990234	154	-11.70043945	244	1.588623047	334	-11.65429688
66	1.087646484	156	-11.71362305	246	1.114013672	336	-11.62792969
68	0.131835938	158	-11.5949707	248	0.171386719	338	-11.62792969
70	-0.547119141	160	-11.58837891	250	-0.573486328	340	-11.56201172
72	-1.0546875	162	-11.1862793	252	-1.074462891	342	-11.12036133
74	-1.549072266	164	-10.79077148	254	-1.502929687	344	-10.81713867
76	-1.641357422	166	-9.861328125	256	-1.628173828	346	-9.834960938
78	-1.977539063	168	-8.971435547	258	-1.984130859	348	-8.978027344
80	-1.944580078	170	-7.929931641	260	-1.957763672	350	-7.883789063
82	-1.766601563	172	-6.512695313	262	-1.713867188	352	-6.473144531
84	-1.753417969	174	-5.510742187	264	-1.694091797	354	-5.444824219
86	-1.0546875	176	-3.697998047	266	-1.034912109	356	-3.684814453
88	-0.250488281	178	-1.680908203	268	-0.283447266	358	-1.654541016

Table II – Anomaly #2a Correction Factor (Minutes)

Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor
0	0.203780402	90	0.388943965	180	0.192649156	270	0.149467633
2	1.201123493	92	0.425014547	182	1.302393729	272	0.466394333
4	2.70465535	94	1.029048142	184	2.654324654	274	1.024646311
6	3.789635076	96	1.054983614	186	3.541737941	276	1.138295364
8	4.421013418	98	0.985566018	188	4.412445369	278	1.15876717
10	5.215566619	100	1.304993369	190	5.203491983	280	1.099923444
12	5.834478943	102	0.905201887	192	5.803723899	282	0.694276061
14	6.365571511	104	0.618766526	194	6.389561265	284	0.634835761
16	6.955572794	106	0.339237225	196	6.917655625	286	0.445449797
18	7.215013746	108	-0.175559243	198	7.108442088	288	-0.177214754
20	7.668033013	110	-0.406551233	200	7.718946308	290	-0.454718209
22	8.020721684	112	-0.99953425	202	8.027522848	292	-0.889492647
24	7.933794161	114	-1.499164395	204	7.888002744	294	-1.403421394
26	8.232306488	116	-1.844624191	206	8.144939892	296	-1.843684976
28	8.178317924	118	-2.397679189	208	8.138785463	298	-2.293495361
30	8.045994542	120	-2.881543541	210	8.080969999	300	-3.028744943
32	8.36259965	122	-3.236345202	212	8.292840379	302	-3.324410371
34	8.165615526	124	-3.826772691	214	8.137597002	304	-3.95622932
36	7.853648573	126	-4.402200107	216	7.853112414	306	-4.509103327
38	7.801531535	128	-4.684869835	218	7.773708404	308	-4.688703638
40	7.335965753	130	-5.328598278	220	7.275534799	310	-5.187045539
42	7.221900549	132	-5.670542709	222	7.201587126	312	-5.509262725
44	7.082034482	134	-5.97411451	224	7.004955442	314	-5.888379652
46	6.460299345	136	-6.658819257	226	6.398031462	316	-6.48066597
48	6.09360404	138	-6.661897423	228	6.026752907	318	-6.814284697
50	5.627097169	140	-7.094021917	230	5.558449327	320	-6.980523747
52	5.225444131	142	-7.603145351	232	5.165559731	322	-7.525344389
54	4.799049593	144	-7.4361178	234	4.774337917	324	-7.475305746
56	4.331451914	146	-7.735451293	236	4.300501478	326	-7.830463169
58	3.692843475	148	-7.941762029	238	3.67712898	328	-7.845085267
60	3.461690092	150	-7.955998624	240	3.376174401	330	-7.737209372
62	2.917592224	152	-8.046982441	242	2.842718999	332	-7.950106111
64	2.396542424	154	-7.80890584	244	2.361198081	334	-8.023122068
66	2.206561334	156	-7.518632897	246	2.219187977	336	-7.690545974
68	1.553478755	158	-7.694354839	248	1.317468789	338	-7.71908654
70	1.049330378	160	-7.452276395	250	1.026060671	340	-7.438013668
72	0.597675735	162	-6.973083459	252	0.584687534	342	-6.895998369
74	0.206092961	164	-6.72826432	254	0.257365342	344	-6.759761311
76	0.019981548	166	-6.191360248	256	0.024375455	346	-6.141721479
78	-0.219060483	168	-5.698378367	258	-0.199283218	348	-5.697087991
80	-0.546519868	170	-5.196077543	260	-0.576187854	350	-5.132956339
82	-0.576407731	172	-4.228528382	262	-0.534840477	352	-4.20309308
84	-0.614729518	174	-3.402853297	264	-0.531974122	354	-3.335120298
86	-0.399630686	176	-2.508137965	266	-0.387924935	356	-2.453570836
88	0.180584177	178	-1.065912708	268	0.143590373	358	-1.041202907

Table II – Anomaly #2b Correction Factor (Minutes)

ANOMALY #3

PRECAUTIONARY NOTE:

The ACT5028 RDC converter can provide incorrect data output if a unit step of 180° (starting at any angle) is introduced to the Sin / Cos input.

This anomaly is difficult to reproduce since a Resolver will never provide a unit step function to the RDC chip.

The only time this would be a concern is during power up, if the Resolver is set to 180° . The RDC will initialize its internal counter to 0000h which simulates the unit step function mentioned above. In practice this error condition during power up is difficult to produce because of the dynamics associated with all the variables when power is first applied.

If the system designer does nothing to accommodate this potential problem the system could see an error at power on, however, this error will be self corrected once the Resolver begins to rotate.

ORDERING INFORMATION ³

AEROFLEX PART #	DSCC SMD #	SCREENING	PACKAGE
ACT5028-201-1S ACT5028-201-2S	5962-0423501KXC 5962-0423501KXA	In accordance with DSCC SMD Rev. B Silicon ²	CQFP -
ACT5028-202-1S ACT5028-202-2S	5962-0423502KXC 5962-0423502KXA		
ACT5028-2-1-S ¹	-	Class K, Rev. B Silicon ²	
ACT5028-2-1-7 ¹		Class C, Rev. B Silicon ²	
ACT5028-2-2-S ¹	-	Class K, Rev. B Silicon ²	
ACT5028-2-2-7 ¹		Class C, Rev. B Silicon ²	
ACT5028, Evaluation board ^{3 4}		-	

Notes

1. Dash #'s:

The first dash number indicates the revision of silicon:

-1 = Rev. A

-2 = Rev. B

The second dash number indicates the wafer lot run.

The last dash number indicates the testing level of the part:

7 = Class C = Commercial Flow, Commercial Temp. Range, 0°C to +70°C testing

S = MIL-PRF-38534 Class K Flow, -55°C to +125°C testing (Rev. B Silicon)

2. See Errata information Anomaly #1, 2 & 3 within this data sheet.

3. Contact factory for availability and pricing.

4. See Application note AN5028-1

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

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