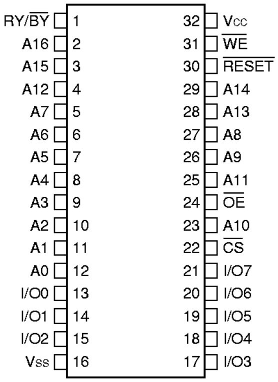
128Kx8 CMOS MONOLITHIC EEPROM

*ADVANCED**

FIG. 1

PIN CONFIGURATION

32 DIP
32 CSOJ
TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground
$\overline{RESET}$	Reset
RY/$\overline{BY}$	Ready/Busy

FEATURES

- Access Times of 150, 200, 250, 300ns
- JEDEC Approved Packages
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ce.ramic, 0.400" SOJ (Package 101)
- Organized as 128Kx8.
- CMOS:
  - Radiation Tolerant with Epitaxial Layer Die
- Commercial, Industrial and Military Temperature Ranges
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Page Write Cycle Time 10ms Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.6 to +6.25	V
Voltage on $\overline{\text{OE}}$ and A9		-0.6 to +13.5	V

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{RESET}}$	RY/$\overline{\text{BY}}$	Mode	Data I/O
L	L	H	H*	High Z	Read	Data Out
H	X	X	X	High Z	Standby	High Z
L	H	L	H	High Z to V_{OL}	Write	Data In
L	H	H	H	High Z	Out Disable	High Z
X	X	H	X		Write Inhibit	
X	L	X	X			
L	L	H	H	V_{OL}	Data Polling	Data Out (I/O_7)
X	X	X	L	High Z	ProgramReset	High Z

NOTE:
* Refer to the recommended DC operating conditions.
X = Don't care

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

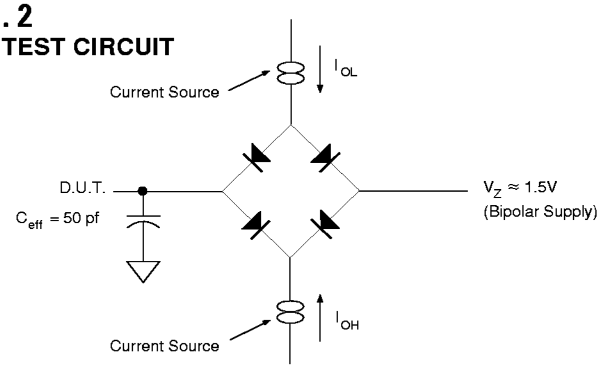
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{\text{CS}}$ = V_{IH}, $\overline{\text{OE}}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	I_{CC}	$\overline{\text{CS}}$ = V_{IL}, $\overline{\text{OE}}$ = V_{IH}, f = 5MHz		60	mA
Standby Current	I_{SB}	$\overline{\text{CS}}$ = V_{IH}, $\overline{\text{OE}}$ = V_{IH}, f = 5MHz		1	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5V		0.40	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.5V	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIG. 2

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

WRITE

A write cycle is initiated when OE is high and a low pulse is on WE or CS with CS or WE low. The address is latched on the falling edge of CS or WE whichever occurs last. The data is latched by the rising edge of CS or WE, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 3 and 4 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the CS line low. Write enable consists of setting the WE line low. The write cycle begins when the last of either CS or WE goes low.

The WE line transition from high to low also initiates an internal 150 µsec delay timer to permit page mode operation. Each subsequent WE transition from high to low that occurs before the completion of the 150 µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Write Cycle Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Write Pulse Width (WE or CS)	t_{WP}	250		ns
Chip Select Set-up Time	t_{CS}	0		ns
Address Hold Time	t_{AH}	150		ns
Data Hold Time	t_{DH}	10		ns
Chip Select Hold Time	t_{CH}	0		ns
Data Set-up Time	t_{DS}	100		ns
Output Enable Set-up Time	t_{OES}	0		ns
Output Enable Hold Time	t_{OEH}	0		ns
Byte Load Cycle	t_{BL}	1		µs
Reset High Time	t_{RES}	1		µs
Reset Protect Time	t_{RP}	100		µs

FIG. 3

WRITE WAVEFORMS WE CONTROLLED

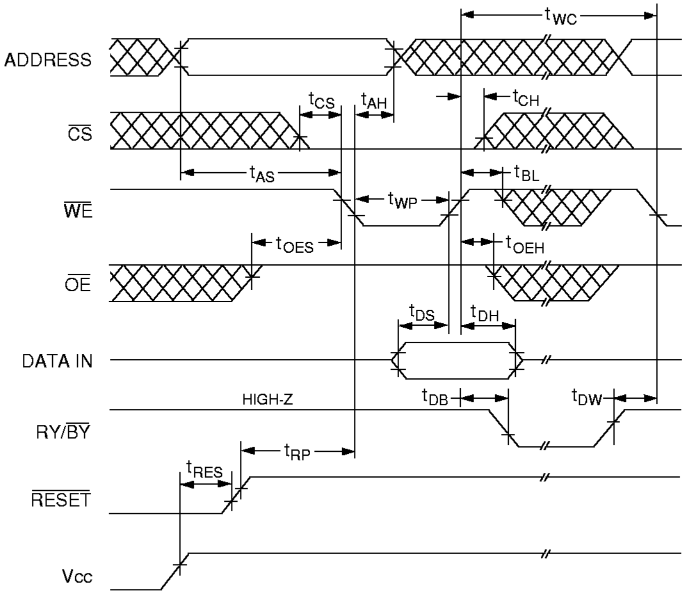
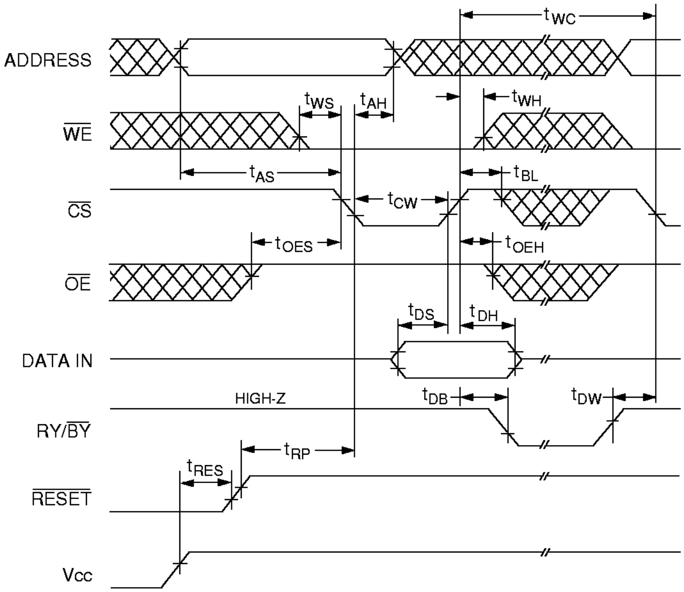


FIG. 4

WRITE WAVEFORMS CS CONTROLLED



READ

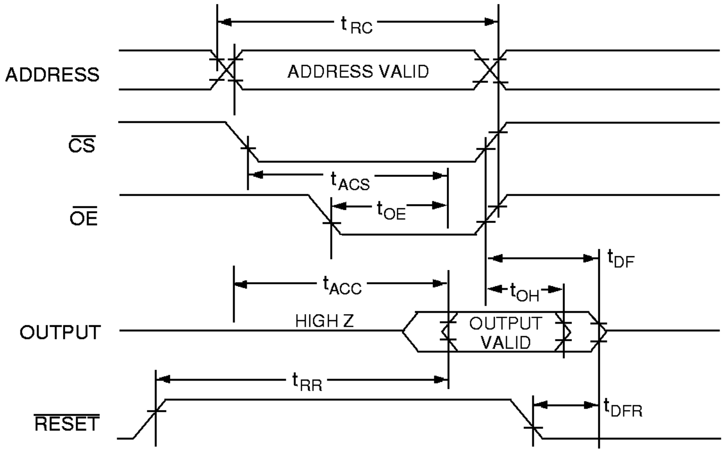
The WME128K8-XXXE stores data at the memory location determined by the address pins. When $\overline{CS}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, this data is present on the outputs. When $\overline{CS}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This two line control prevents bus contention.

AC READ CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Read Cycle Parameter	Symbol	-150		-200		-250		-300		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		300		ns
Address Access Time	t_{ACC}		150		200		250		300	ns
Chip Select Access Time	t_{ACS}		150		200		250		300	ns
Output Hold from Add. Change, $\overline{OE}$ or $\overline{CS}$	t_{OH}	0		0		0		0		ns
Output Enable to Output Valid	t_{OE}	10	75	10	75	10	85	10	85	ns
Chip Select or $\overline{OE}$ to High Z Output	t_{DF}		55		55		70		70	ns
$\overline{RESET}$ Low to Output Float	t_{DFR}		350		350		350		350	ns
$\overline{RESET}$ to Output Delay	t_{RR}		450		450		450		450	ns

FIG. 5
READ WAVEFORMS



NOTES:
$\overline{OE}$ may be delayed up to t_{ACS} - t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{OE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

DATA POLLING

The WME128K8-XXXE offers a data polling feature which allows a faster method of writing to the device. Figure 6 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D_7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

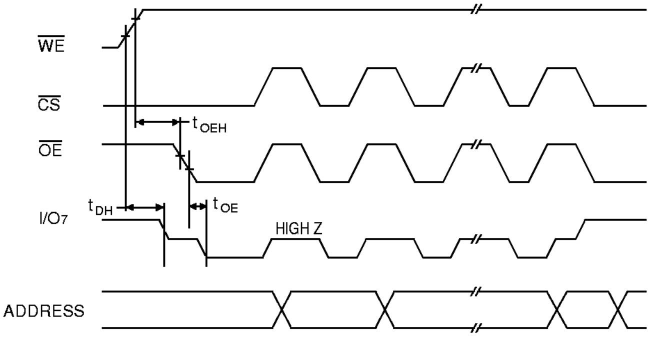
DATA POLLING CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t_{DH}	10		ns
$\overline{OE}$ Hold Time	t_{OEH}	0		ns
$\overline{OE}$ To Output Valid	t_{OE}		55	ns

FIG. 6

DATA POLLING WAVEFORMS



PAGE WRITE OPERATION

The WME128K8-XXXE has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 30µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 30µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

PAGE WRITE CHARACTERISTICS

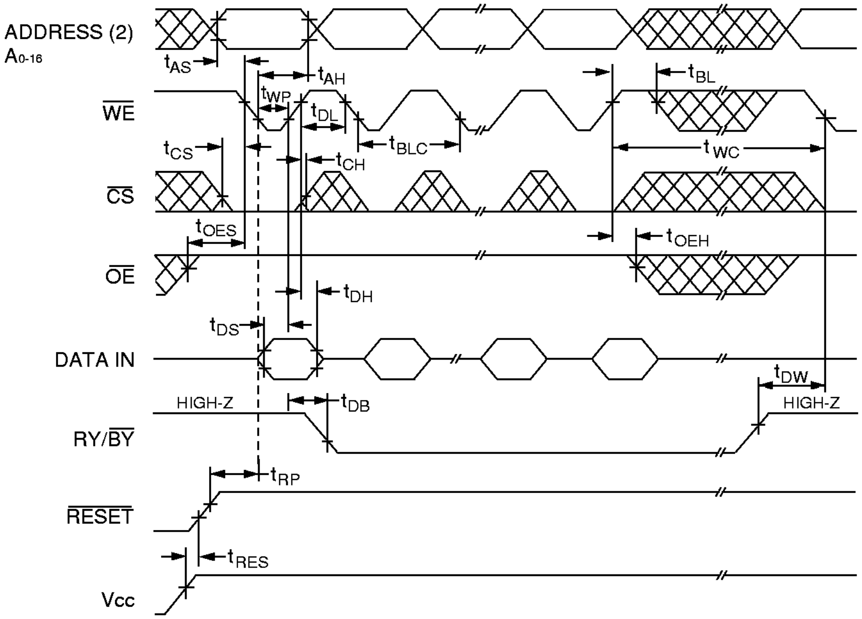
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Page Mode Write Characteristics				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Address Hold Time (1)	t_{AH}	150		ns
Data Set-up Time	t_{DS}	100		ns
Data Hold Time	t_{DH}	10		ns
Write Pulse Width	t_{WP}	250		ns
Byte Load Cycle Time	t_{BLC}		30	µs
Byte Load Window	t_{BL}	100		µs
Data Latch Time	t_{DL}	300		ns
$\overline{\text{RESET}}$ Protect Time	t_{RP}	100		µs
$\overline{\text{RESET}}$ High Time	t_{RES}	1		µs
Time to Device Busy	t_{DB}	120		ns
Write Start Time	t_{DW}	150		ns

1. Page address must remain valid for duration of write cycle.

FIG. 7

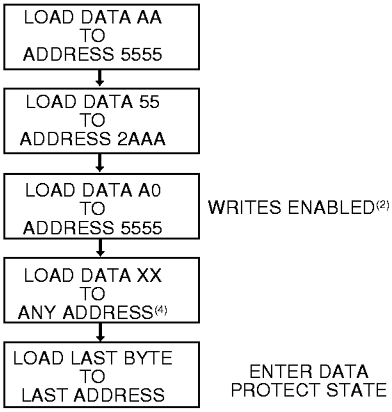
PAGE WRITE WAVEFORMS
$\overline{\text{CS}}$ CONTROLLED(1)



NOTES:
1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. A_7 - A_{16} are page addresses and must be same within the page write operation.

FIG. 8

SOFTWARE DATA PROTECTION ENABLE ALGORITHM(1)

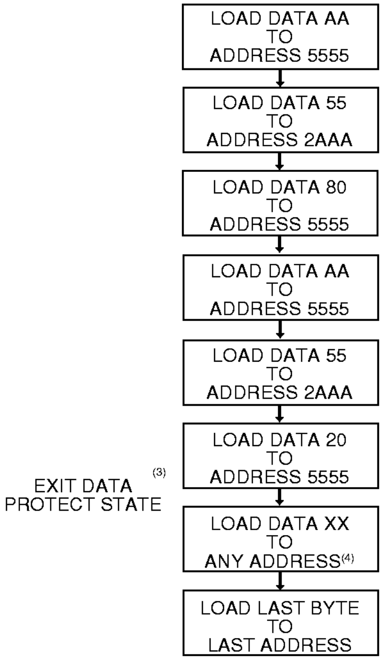


NOTES:

1. Data Format: D_7 - D_0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

FIG. 9

SOFTWARE DATA PROTECTION DISABLE ALGORITHM(1)



NOTES:

1. Data Format: D_7 - D_0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WE-128K32-XXXE has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of t_{WC}. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K byte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

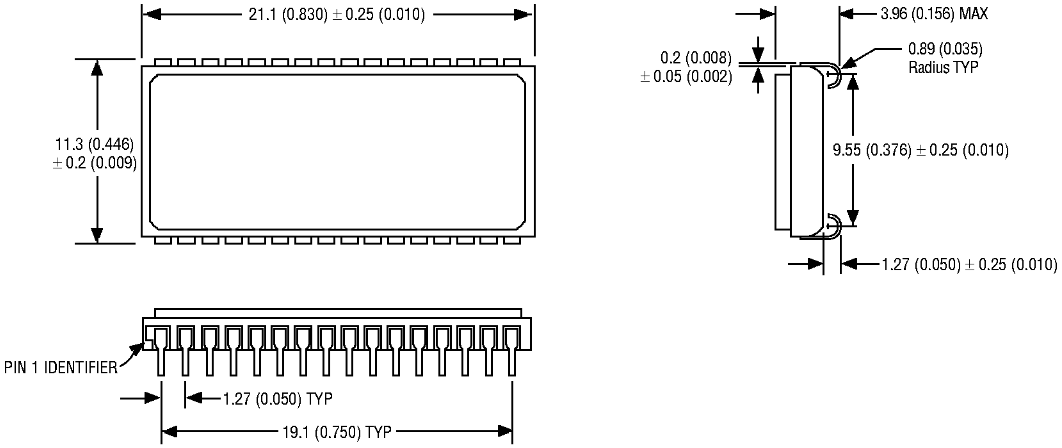
These features protect against inadvertent writes to the WME128K8-XXXE. These are included to improve reliability during normal operation:

a) Write inhibiting
Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

b) Noise filter
Pulses of <20ns (typ) on $\overline{WE}$ or $\overline{CS}$ will not initiate a write cycle.

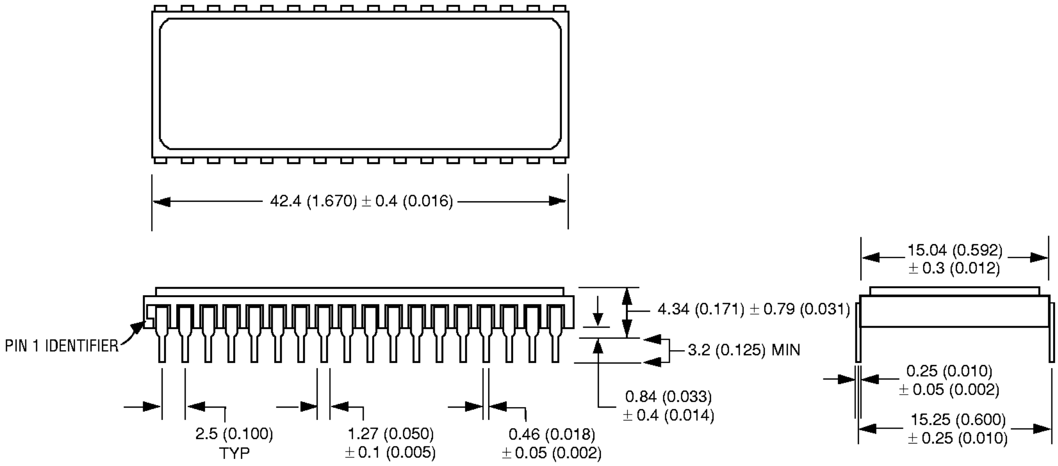
c) Protection by $\overline{\text{RESET}}$

PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M E 128K 8 - XXX X X E X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

E = Epitaxial Layer

DEVICE GRADE:

Q = MIL-STD-883 Compliant		
M = Military Screened	-55°C to +125°C	
I = Industrial	-40°C to +85°C	
C = Commercial	0 to +70°C	

PACKAGE TYPE:

C = 32 Pin Ceramic DIP (Package 300)

DE = 32 Lead CSOJ (Package 101)

ACCESS TIME (ns)

ORGANIZATION 128K x **8**

EEPROM

MONOLITHIC

WHITE MICROELECTRONICS