Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

ADVANCE INFORMATION
IDT 7384

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar, or image processing applications
- Includes flexible funnel shifter
- Pipeline or flow-through modes
- Multi-level pipeline register on one input port
- Three accumulators with an internal feedback path
- Scaling shifter on output stage for dynamic range control
- Rounding on output stage
- Bit reversal on output stage for FFT address generation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS ™ technology
- Available in 84-lead PGA and 84-pin surface mount PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7384 is a high-speed cascadable Arithmetic Logic Unit (ALU). This three-bus device has a 4-level pipeline register on one input port (A port) and a single input register on the other input port (B port). An ultra-fast 16-bit ALU, a funnel shifter with merge capabilities, and three accumulators make up the heart of the IDT7384. With IDT's high-performance CEMOS ™ technology, the IDT7384 can do arithmetic or logic operations in 20ns. Results of ALU operations can be scaled, rounded, or bit reversed for FFT address generation using the IDT7384 output stage.

The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F accumulators can also be set into clocked or flow-through mode. The A port has a 4-level pipeline register that can be configured as 1 four-level, 2 two-level, or 4 single-level pipelines. The three LDA0-LDA2 control pins set the configuration and the register loaded.

The IDT7384 has five function pins to select 1 of 32 arithmetic or logic operations and the R, S input selections to the ALU. The R and S ALU inputs can be A, B, F, or all 1's. This ALU has a carry out pin for cascading. Three accumulators are provided on the IDT7384 for intermediate result storage.

The IDT7384 funnel shifter will do logical shifts, rotates, and rotates with merges. The 16-bit R-multiplexer and S-multiplexer inputs can be concatenated in either order for 32-bit logical shifts. A 16-bit result is extracted at the funnel shifter output. The R-multiplexer input can be rotated or rotated and merged with the F feedback bus using the S-multiplexer input as a mask.

The output stage of this ALU can round the F result up or down by one bit. The F result can also be arithmetically or logically shifted by one bit under the IDT7384 output control (FS0-FS5). Bit reversal can be performed on the F result to generate fast Fourier transform (FFT) addresses.

An output enable is provided for three-state control of the output port on a bus.

The IDT7384 is available in 84-pin PLCC or PGA packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B for high reliability systems.

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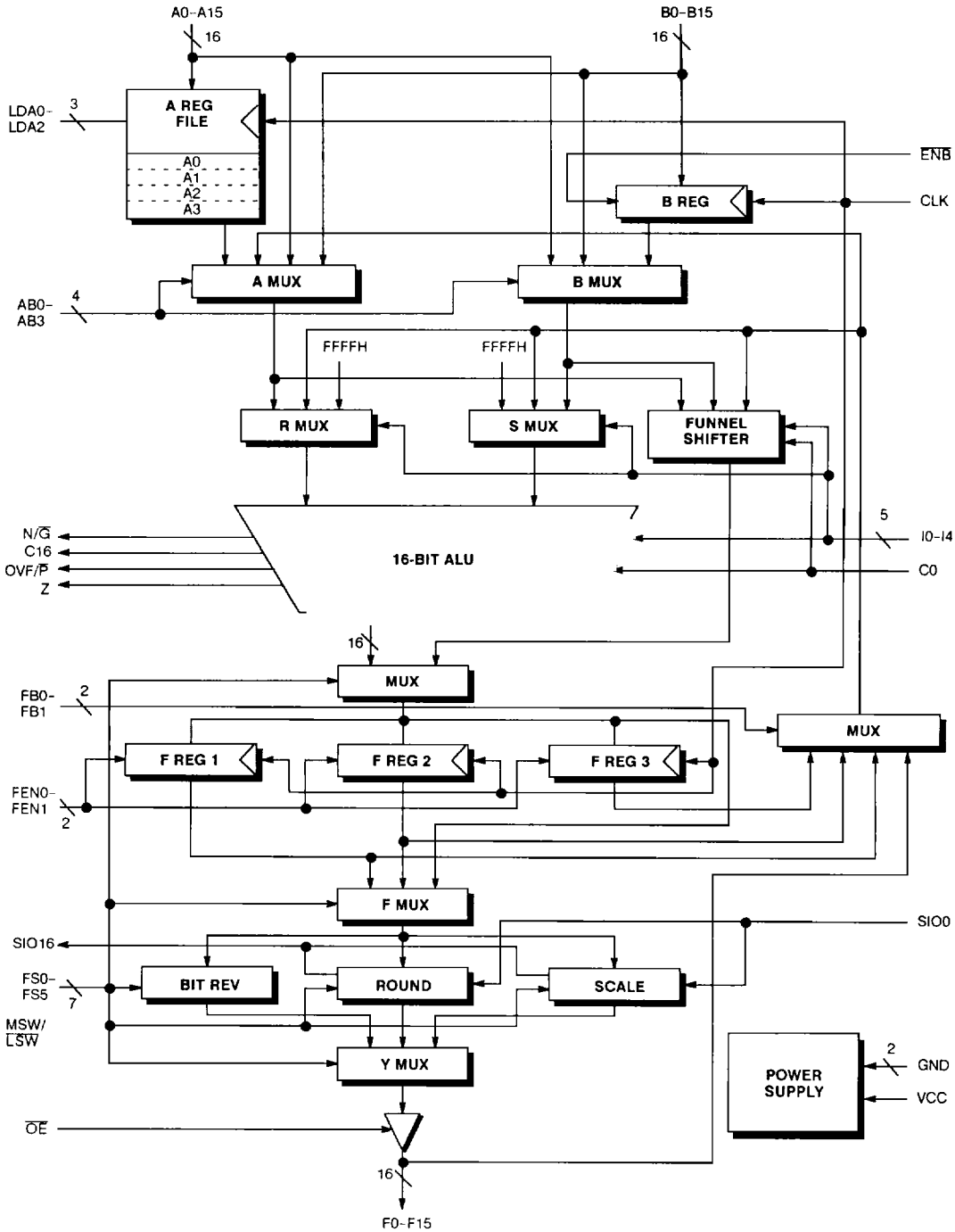
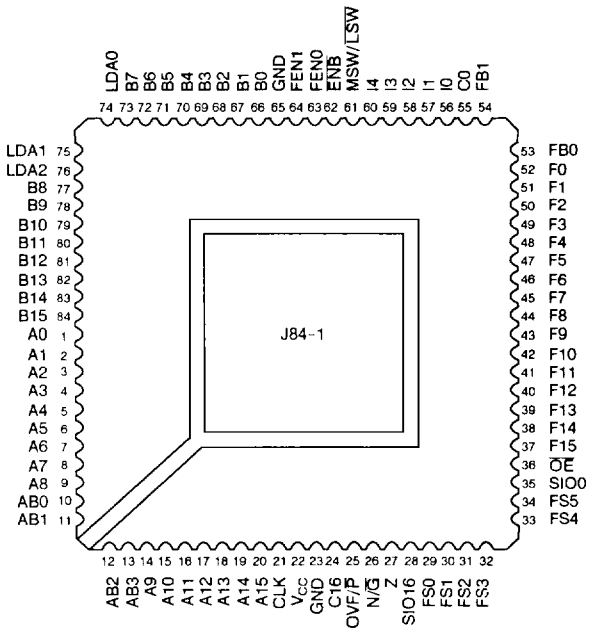
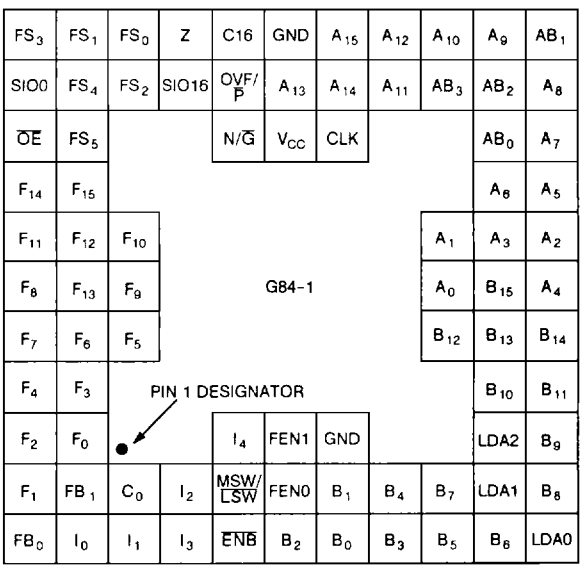
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PLCC
TOP VIEW



PGA
TOP VIEW

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