TMC2249

CMOS Digital Mixer

12 x 12 Bit, 30MHz

The TMC2249 is a high-speed digital arithmetic circuit consisting of two 12-bit multipliers, an adder and a cascadeable accumulator. All four multiplier inputs are accessible to the user, and each includes a user-programmable pipeline delay of up to 16 clocks in length. The 24-bit adder/subtractor is followed by an accumulator and 16-bit input port which allows the user to cascade multiple TMC2249s. A new 16-bit accumulated output is available every clock, up to the maximum rate of 30MHz. All inputs and outputs are registered except the three-state output enable, and all are TTL compatible.

The TMC2249 utilizes a pipelined, bus-oriented structure offering significant flexibility. Input register clock enables and programmable input data pipeline delays on each port offer an adaptable input structure for high-speed digital systems. Following the multipliers, the user may perform addition or subtraction of either product, arithmetic rounding to 16 bits, and accumulation and summation of products with a cascading input. The output port allows access to all 24 bits of the internal accumulator by switching between overlapping least and most-significant 16-bit words, and a three-state output enable simplifies a connection to an external system bus.

All programmable features are utilized on a clock-by-clock basis, with internal data and control pipeline registers provided to maintain synchronous operation between incoming data and all available functions within the device.

The TMC2249 has numerous applications in digital processing algorithms, from executing simple image mixing and switching, to performing complex arithmetic functions and complex waveform synthesis. FIR filters, digital quadrature mixers and modulators, and vector arithmetic functions may also be implemented with this device.

Fabricated using TRWs proprietary OMICRON-C™ one-micron CMOS process, the TMC2249 operates at a guaranteed clock rate of 30MHz over the standard commercial temperature and supply voltage ranges, and is available in a low-cost 120 pin plastic pin grid array.

Features

- 30MHz Input And Computation Rate
- Two 12-Bit Multipliers With Separate Data And Coefficient Inputs
- Independent, User-Selectable Pipeline Delays Of 1 to 16 Clocks On All Input Ports
- Separate 16-Bit Input Port Allows Cascading Or Addition Of A Constant
- User-Selectable Rounding Of Products
- Fully Registered, Pipelined Architecture
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 120 Pin Plastic Pin Grid Array

Applications

- Video Switching
- Image Mixing
- Digital Signal Modulation
- Complex Frequency Synthesis
- Digital Filtering
- Complex Arithmetic Functions

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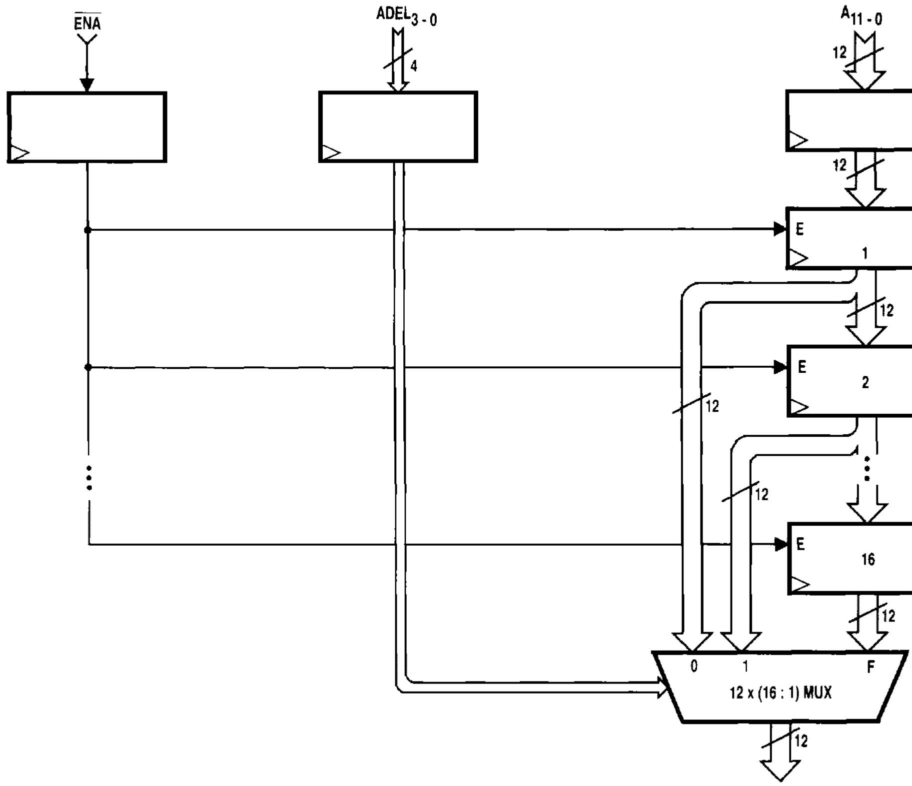
Functional Block Diagram



Functional Description

General Information

The TMC2249 performs the summation of products described by the formula:

$$S(N+6) = A(N-ADEL) \bullet B(N-BDEL) \bullet (-1^{NEG1(N)}) + C(N-CDEL) \bullet D(N-DDEL) \bullet (-1^{NEG2(N)}) + CAS(N+3 \bullet FT)$$

where ADEL through DDEL range from 1 to 16 pipe delays. All inputs and controls utilize pipeline delay registers to maintain synchronicity with the data input during that clock, except when the Cascade data input is routed directly to the accumulator by use of the Feedthrough control. One-half LSB rounding to 16 bits may be performed on the sum of products while summing with the cascade input data. The user may access either the upper or lower 16 bits of the 24-bit accumulator by swapping overlapping registers. The output bus has an asynchronous high-impedance enable, to simplify interfacing to complex systems.

Signal Definitions

Power

V_{DD}, GND	The TMC2249 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK	The TMC2249 operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

A_{11-0} – D_{11-0}	A through D are the four 12-bit registered data input ports. A_0-D_0 are the LSBs. See *Table 1*. Data presented to the input ports is clocked in to the top of the 16-stage delay pipeline on the next clock when enabled, "pushing" data down the register stack.
CAS_{15-0}	CAS is the 16-bit Cascade data input port. CAS_0 is the LSB. See *Table 1*.

Outputs

S_{15-0}	The current 16-bit result is available at the Sum output. The LSB is S_0. The output may be the most or least significant 16 bits of the current accumulator output, as determined by $\overline{SWAP}$. S_0 is the LSB. See *Table 1*.

Controls

$\overline{ENA}$ – $\overline{END}$	Input data presented to port i11-0 (i=A, B, C, or D) are latched into delay pipeline i, and data already in pipeline i advance by one register position, on each rising edge of CLK for which ENi is LOW. When ENi is HIGH, the data in pipeline i do not move and the value at the input port i will be lost before it reaches the multiplier.
$ADEL_{3-0}$ – $DDEL_{3-0}$	ADEL through DDEL are the four-bit registered input data pipe delay select word inputs. Data to be presented to the multipliers is selected from one of sixteen stages in the input data delay pipe registers, as indicated by the delay select word presented to the respective input port during that clock. The minimum delay is one clock (select word=0000), and the maximum delay is 16 clocks (select word=1111). Following powerup these values are indeterminate and must be initialized by the user.
NEG1, NEG2	The products of the multipliers are negated, causing a subtraction to be performed during the internal summation of products, when the Negate controls are HIGH. NEG1 negates the product A x B, while NEG2 acts on the output of the multiplier which generates the product C x D. These controls indicate the operation to be performed on data input during the current clock, when the length controls ADEL–DDEL are set to zero.
RND	When the rounding control is HIGH, the sum of products resulting from data input during that clock is rounded to 16 bits. Rounding is performed only during the first cycle of each accumulation sequence, to avoid the accumulation of roundoff errors.
FT	When the Feedthrough control is HIGH, the pipeline delay through the cascade data path is minimized to simplify the cascading of multiple devices. When FT is LOW and ADEL through DDEL are all set to 0, the data inputs are aligned, such that $S(n+6) = CAS(n) + A(n)B(n) + C(n)D(n)$. See *Table 2*.
$\overline{CASEN}$	Data presented at the cascade data input port are latched and accumulated internally when the input enable $\overline{CASEN}$ during that clock is LOW. When $\overline{CASEN}$ is HIGH, the cascade input port is ignored.
ACC	When the registered Accumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of previous products.
$\overline{SWAP}$	The user may access both the most and least-significant 16 bits of the 24-bit accumulator by utilizing $\overline{SWAP}$. Normal operation of the device, with $\overline{SWAP}$=HIGH, outputs the most significant word. Setting $\overline{SWAP}$=LOW puts a double-register structure into "toggle" mode, allowing the user to examine the LSW on alternate clocks. New output data will not be clocked into the output registers until $\overline{SWAP}$ returns HIGH.
$\overline{OE}$	Data currently in the output registers is available at the output bus S_{15-0} when the asynchronous Output Enable is LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.

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Table 1. Data Formats and Bit Weighting

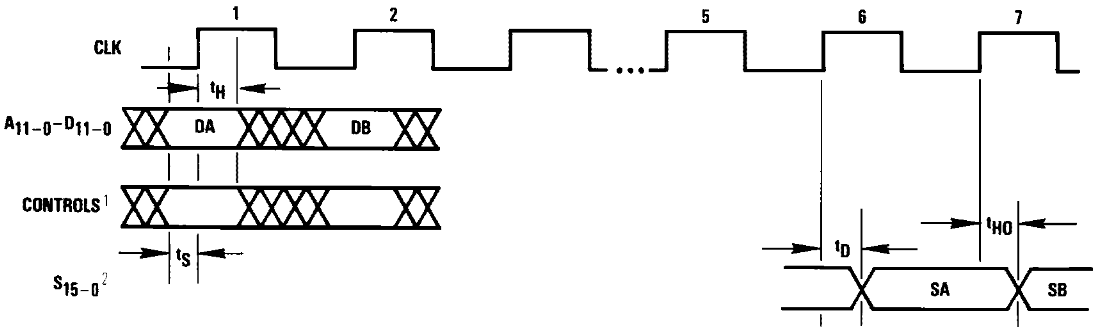
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
				-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DATA INPUT ($A_{11-0} - D_{11-0}$)
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	CASCADE INPUT (CAS_{15-0})
																SUM (S_{15-0})
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSW
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	MSW

Note: 1. A minus sign indicates the sign bit.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8	13, 21, 50, 112
	GND	Ground	E3, G3, J3, L6, H11, C7	9, 17, 25, 46, 79, 116
Clock	CLK	System Clock	C3	2
Inputs	A_{11-0}	A Input	N8, M8, L8, N9, M9, N10, L9, M10, N11, N12, L10, M11	52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63
	B_{11-0}	B Input	N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, L4	51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 39, 38
	C_{11-0}	C Input	A9, B9, A10, C9, B10, A11, B11, C10, A12, B12, C11, A13	111, 110, 109, 108, 107, 106, 105, 104, 103, 102, 101, 100
	D_{11-0}	D Input	B8, A8, B7, A7, A6, B6, C6, A5, B5, A4, C5, B4	113, 114, 115, 117, 118, 119, 120, 121, 122, 123, 124, 125
	$ADEL_{3-0}$	A Delay	L11, M12, M13, K11	68, 69, 70, 71
	$BDEL_{3-0}$	B Delay	M2, L3, N1, L2	36, 35, 31, 30
	$CDEL_{3-0}$	C Delay	D11, B13, C13, D12	95, 94, 93, 92
	$DDEL_{3-0}$	D Delay	A2, C4, B3, A1	127, 128, 129, 130
	CAS_{15-0}	Cascade Input	L13, K12, J11, K13, J12, J13, H12, H13, G12, G11, G13, F13, F12, F11, E13, E12	73, 74, 75, 76, 77, 78, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89
Outputs	S_{15-0}	Sum Output	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27
Controls	$\overline{ENA} - \overline{END}$	Input Enables	N13, N2, C12, A3	64, 37, 96, 126
	NEG1, NEG2	Negate	B1, D3	4, 5
	RND	Round	C2	6
	FT	Feedthrough	E11	91
	$\overline{CASEN}$	Cascade Enable	D13	90
	ACC	Accumulate	B2	3
	$\overline{SWAP}$	Swap Output Words	K3	29
	$\overline{OE}$	Output Enable	M1	28
No Connect	NC	None	L12	1, 32, 33, 34, 65, 66, 67, 72, 98, 99, 100, 131, 132
		Index Pin	D4	

Figure 1. Timing Diagram



Notes: 1. Except $\overline{OE}$.
2. Assumes $\overline{OE}$ = LOW, and ADEL – DDEL set to 0

Figure 2. Equivalent Input Circuit

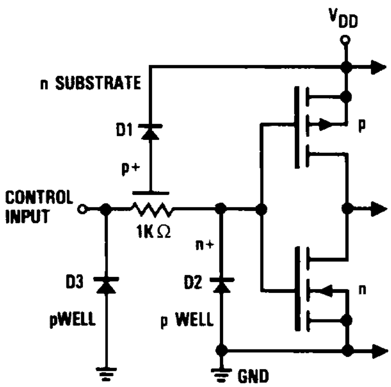


Figure 3. Equivalent Output Circuit

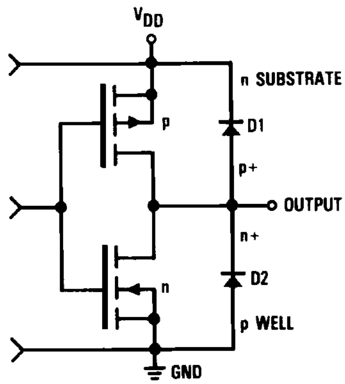
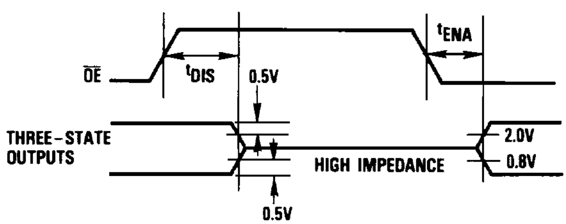


Figure 4. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD}+0.5)V
Output	
Applied voltage[2]	−0.5 to (V_{DD}+0.5)V
Forced current[3,4]	−6.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended[1]			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0			−2.0	mA
t_{CY}	Cycle Time	V_{DD}=Min TMC2249	40						ns
		TMC2249-1	33						ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	15						ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	10						ns
t_S	Input Setup Time		8						ns
t_H	Input Hold Time		4						ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					−55		125	°C

Note: 1. Consult factory for extended temperature specifications

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		6			mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OEN}$ = 5V, f = 25MHz		100			mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		60		60	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but operation is guaranteed as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF TMC2249		17			ns
		TMC2249-1		15			ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	5				ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		15			ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		20			ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

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Applications Discussion

Basic Operation

The TMC2249 is a flexible signal and image processing building block with numerous user-selectable functions which expand it's usefulness. *Table 2* clarifies the operation of the device, demonstrating the various features available to the user and the timing delays incurred.

Table 2. TMC2249 Operation Sequence

CLK	ADEL	A_{11-0}	BDEL	B_{11-0}	CDEL	C_{11-0}	DDEL	D_{11-0}	NEG1	NEG2	CAS_{15-0}	FT	ACC	RND	$\overline{SWAP}$	S_{15-0}
1	0	A(1)	0	B(1)	0	C(1)	0	D(1)	L	L	–	L	L	L	H	–
2	0	A(2)	0	B(2)	0	C(2)	0	D(2)	L	H	–	L	L	L	H	–
3	0	A(3)	0	B(3)	0	C(3)	0	D(3)	H	L	–	L	L	L	H	–
4	0	A(4)	0	B(4)	0	C(4)	0	D(4)	L	L	CAS(4)	L	L	L	H	–
5	0	A(5)	0	B(5)	0	C(5)	0	D(5)	L	L	–	L	L	L	H	–
6	0	A(6)	0	B(6)	0	C(6)	0	D(6)	L	L	–	L	L	H	H	$(A(1) \cdot B(1) + C(1) \cdot D(1))_{ms}$
7	0	A(7)	0	B(7)	0	C(7)	0	D(7)	L	L	–	L	H	H	H	$(A(2) \cdot B(2) - C(2) \cdot D(2))_{ms}$
8	0	A(8)	0	B(8)	0	C(8)	0	D(8)	L	L	CAS(8)	H	L	L	L	$(-A(3) \cdot B(3) + C(3) \cdot D(3))_{ms}$
9	0	A(9)	0	B(9)	0	C(9)	0	D(9)	L	L	–	L	L	L	H	$(A(4) \cdot B(4) + C(4) \cdot D(4) + CAS(4))_{ms}$
10																$(A(5) \cdot B(5) + C(5) \cdot D(5) + CAS(8))_{ms}$
11																$(A(6) \cdot B(6) + C(6) \cdot D(6) + 2^7)_{ms}$
12																$(A(7) \cdot B(7) + C(7) \cdot D(7) + S(11))_{ms}$
13																$(S(12))_{ls}$
14																$(A(9) \cdot B(8) + C(7) \cdot D(6))_{ms}$

Where H = HIGH, L = LOW. "ms" indicates most significant output word (bits 23 – 8), "ls" indicates least significant word (bits 15 – 0). The appropriates enables for the indicated data are assumed, otherwise '–' indicates that port not enabled. Note that the output data summation including A(8) – D(8) is lost, since the output on cycle 13 is swapped to the LSW of S(12) on cycle 8.

Digital Filtering

The input structure of the TMC2249 demonstrates great versatility when all four multiplier inputs and the programmable delay registers are utilized. ***Tables 3*** and ***4*** demonstrate how a direct-form symmetric FIR filter of up to 32 taps can be implemented. By utilizing the four input delay registers as pipelined storage banks, the user can store up to 32 coefficient-data word pairs, split into alternate "even" and "odd" halves. Two taps of the filter are calculated on each clock, and the user then increments/decrements the delay words (ADEL – DDEL). The sums of products are successively added to the global sum in the internal accumulator. Once all of the products of the desired taps have been summed, the resultant is available at the output. The user then "pushes" a new time-data sample on to the appropriate even or odd data register "stack" and reiterates the summation. Note that the coefficient bank "pointers", the BDEL and DDEL delay words, are alternately incremented and decremented on successive filter passes to maintain alignment between the incoming data samples and their respective coefficients. The effective filter speed is calculated by dividing the clock rate by one-half the number of taps implemented.

Table 3. Using the TMC2249 to Perform FIR Filtering — Initial Data Loading

	Even Data	Odd Data	Coefficient	Storage
Register Position (Hex)	A	C	B	D
0	x(31)	x(30)	h(0)	h(1)
1	x(29)	x(28)	h(2)	h(3)
2	x(27)	x(26)	h(4)	h(5)
3	x(25)	x(24)	h(6)	h(7)
4	x(23)	x(22)	h(8)	h(9)
5	x(21)	x(20)	h(10)	h(11)
6	x(19)	x(18)	h(12)	h(13)
7	x(17)	x(16)	h(14)	h(15)
8	x(15)	x(14)	h(15)	h(14)
9	x(13)	x(12)	h(13)	h(12)
A	x(11)	x(10)	h(11)	h(10)
B	x(9)	x(8)	h(9)	h(8)
C	x(7)	x(6)	h(7)	h(6)
D	x(5)	x(4)	h(5)	h(4)
E	x(3)	x(2)	h(3)	h(2)
F	x(1)	x(0)	h(1)	h(0)

Table 4. FIR Filtering – Operation Sequence

Cycle	Push A	B	Push C	D	ADEL	CDEL	BDEL	DDEL	ACC	ENA	ENC	ENB	END	Convolution Sum	Resultant Output
1	–	–	–	–	0	0	0	0	H	H	H	H	H	x(31)•h(0)+x(30)•h(1)	
2	–	–	–	–	1	1	1	1	H	H	H	H	H	+x(29)•h(2)+x(28)•h(3)	
3	–	–	–	–	2	2	2	2	H	H	H	H	H	+x(27)•h(4)+x(26)•h(5)	
4	–	–	–	–	3	3	3	3	H	H	H	H	H	+x(25)•h(6)+x(24)•h(7)	
5	–	–	–	–	4	4	4	4	H	H	H	H	H	+x(23)•h(8)+(22)•h(9)	
6	–	–	–	–	5	5	5	5	H	H	H	H	H	+x(21)•h(10)+x(20)•h(11)	
7	–	–	–	–	6	6	6	6	H	H	H	H	H	+x(19)•h(12)+x(18)•(13)	
8	–	–	–	–	7	7	7	7	H	H	H	H	H	+x(17)•h(14)+x(16)•h(15)	
9	–	–	–	–	8	8	8	8	H	H	H	H	H	+x(15)•h(15)+(14)•h(14)	
10	–	–	–	–	9	9	9	9	H	H	H	H	H	+x(13)•h(13)+x(12)•h(12)	
11	–	–	–	–	A	A	A	A	H	H	H	H	H	+x(11)•h(11)+x(10)•h(10)	
12	–	–	–	–	B	B	B	B	H	H	H	H	H	+X(9)•h(9)+x(8)•h(8)	
13	–	–	–	–	C	C	C	C	H	H	H	H	H	+x(7)•h(7)+x(6)•h(6)	
14	–	–	–	–	D	D	D	D	H	H	H	H	H	+x(5)•h(5)+x(4)•h(4)	
15	–	–	–	–	E	E	E	E	H	H	H	H	H	+x(3)•h(3)+x(2)•h(2)	
16	–	–	x(32)	–	F	F	F	F	H	H	L	H	H	+x(1)•h(1)+x(0)•h(0)	
17	–	–	–	–	0	0	F	F	H	H	H	H	H	x(31)•h(1)+x(32)•h(0)	
18	–	–	–	–	1	1	E	E	H	H	H	H	H	+x(29)•h(3)+x(30)•h(2)	
19	–	–	–	–	2	2	D	D	H	H	H	H	H	+x(27)•h(5)+x(28)•h(4)	
20	–	–	–	–	3	3	C	C	H	H	H	H	H	+x(25)•h(7)+x(26)•h(6)	
21	–	–	–	–	4	4	B	B	H	H	H	H	H	+x(23)•h(9)+x(24)•h(8)	$S=\sum_{k=0}^{31} h(k)x(n-k)$
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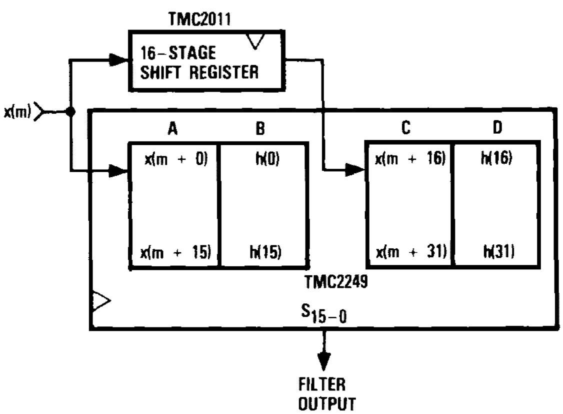
Digital Filtering (cont.)

Alternatively, non-symmetric FIR Filters can be implemented using the TMC2249 in a similar fashion. Here, a shift register is used to delay the incoming data fed to the A input by an amount equal to one-half the length of the filter (the length of the A delay register). As shown in *Figure 5*, the data is then sent to the C input, thus "stacking" the A and C delay registers to create a single N-tap FIR filter. The incremented delay words (ADEL – DDEL) for all four inputs are identical. Again, the filter throughput is equal to the clock speed divided by one-half the number of taps implemented.

Figure 5. Non-Symmetric 32-Tap FIR Filtering Using the TMC2249



Complex Arithmetic Functions

The TMC2249 can also be used to perform complex arithmetic functions. The basic function performed by the device, ignoring the delay controls,

$$SUM = (\pm A \bullet B) + (\pm C \bullet D),$$

can realize in two steps the familiar summation:

$$(P+jR)(S+jT) = \underset{(1)}{(PS-RT)} + j\underset{(2)}{(PT+SR)}$$

by loading the TMC2249 as follows:

Step	TMC2249 Inputs A	B	C	D	NEG1	NEG2	Resultant Output
1	P	S	R	T	L	H	(PS – RT)
2	P	T	R	S	L	L	(PT + SR)

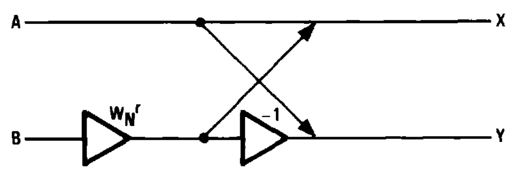
where H and L indicate a logic HIGH and LOW.

Thus we can perform a complex multiplication in two clock cycles. Notice that the user must switch the two components of the second input vector between the B and D inputs to obtain the second complex summation.

Calculating a Butterfly

Taking advantage of the complex multiply which we implemented above using the TMC2249, we can expand slightly to calculate a Radix-2 Butterfly, the core of the Fast Fourier Transform algorithm. To review, the Butterfly is calculated as shown in *Figure 6*.

Figure 6. Signal Flow Diagram of Radix-2 Butterfly



Where $X = A + B(W_N^r)$
$Y = A - B(W_N^r)$,

and W_N^r is the complex phase coefficient, or "twiddle factor" for the N-point transform, which is:

$$W_N^r = e^{-j(2\pi/N)}$$
$$= \cos(2\pi/N) + j(\sin(2\pi/N))$$
$$= Re(W) + jIm(W),$$

with Re and Im indicating the real and imaginary parts of the vector.

Expanding the complex vectors A and B to calculate X and Y, we get:

$$X = (Re(A) + jIm(A)) + (Re(B)Re(W) - Im(B)Im(W) + j(Re(B)Im(W) + Im(B)Re(W))$$
$$= (Re(A) + Re(B)Re(W) - Im(B)Im(W)) + j(Im(A) + Re(B)Im(W) + Im(B)Re(W))$$
$$= Re(X) + jIm(X)$$

and,

$$Y = (Re(A) + jIm(A)) - (Re(B)Re(W) - Im(B)Im(W) + j(Re(B)Im(W) + Im(B)Re(W))$$
$$= (Re(A) - Re(B)Re(W) + Im(B)Im(W)) + j(Im(A) - Re(B)Im(W) - Im(B)Re(W))$$
$$= Re(Y) + jIm(Y)$$

Calculating a Butterfly (cont.)

The butterfly is then neatly implemented in four clocks, as follows:

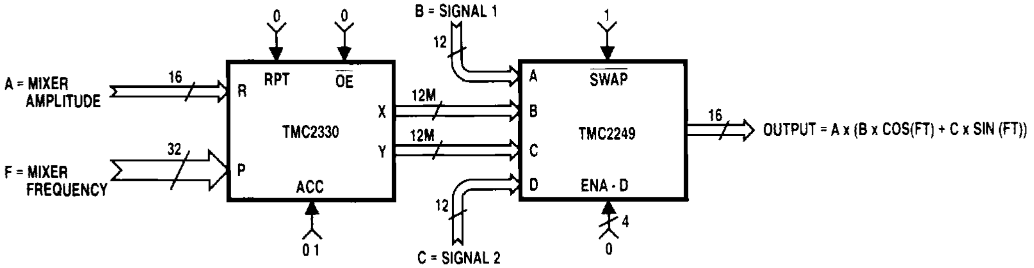
Step	TMC2249 Inputs							Resultant Output
	A	B	C	D	CAS Input	NEG1	NEG2	
1	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	L	H	Re(X)
2	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	H	L	Re(Y)
3	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	L	L	Im(X)
4	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	H	H	Im(Y)

Notice again that the components of the second vector must be switched by the user on the second half of the computation, as well as the parts of the vector presented to the cascade input.

Quadrature Modulation

The TMC2249 can also be used to advantage as a digital-domain complex frequency synthesizer, as demonstrated in *Figure 7*. Here, orthogonal sinusoidal waveforms are generated digitally by sequentially addressing Sine and Cosine ROMS. These quadrature phase coefficients can then be multiplied with two input signals, such as digitized analog data. The TMC2249 then adds these products, which could be output directly to a high-speed digital-to-analog converter such as the TRW TDC1012 for direct waveform synthesis. This 12-bit, 20MHz DAC is ideally suited to waveform generation, featuring extremely low glitch energy for low spurious harmonics.

Figure 7. Direct Quadrature Waveform Synthesizer Using the TMC2249



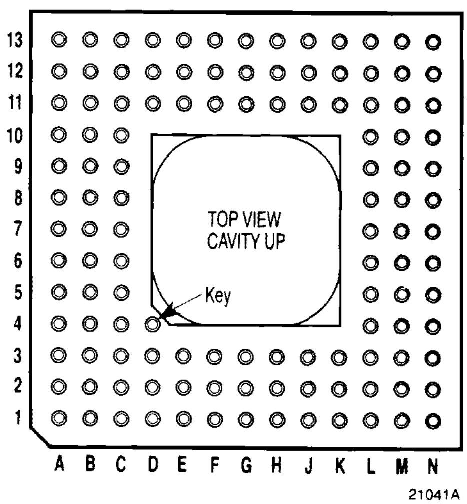
Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	CLK	G3	GND	L3	$BDEL_2$	L7	V_{DD}	L11	$ADEL_3$	G11	CAS_6	C11	C_1	C7	GND
B2	ACC	G1	S_7	M2	$BDEL_3$	N7	B_{11}	M12	$ADEL_2$	G13	CAS_5	B12	C_2	A7	D_8
B1	NEG1	H1	S_6	N2	$\overline{ENB}$	N8	A_{11}	M13	$ADEL_1$	F13	CAS_4	A12	C_3	A6	D_7
D3	NEG2	H2	S_5	L4	B_0	M8	A_{10}	K11	$ADEL_0$	F12	CAS_3	C10	C_4	B6	D_6
C2	RND	H3	V_{DD}	M3	B_1	L8	A_9	L12	NC	F11	CAS_2	B11	C_5	C6	D_5
C1	S_{15}	J1	S_4	N3	B_2	N9	A_8	L13	CAS_{15}	E13	CAS_1	A11	C_6	A5	D_4
D2	S_{14}	J2	S_3	M4	B_3	M9	A_7	K12	CAS_{14}	E12	CAS_0	B10	C_7	B5	D_3
E3	GND	K1	S_2	L5	B_4	N10	A_6	J11	CAS_{13}	D13	$\overline{CASEN}$	C9	C_8	A4	D_2
D1	S_{13}	J3	GND	N4	B_5	L9	A_5	K13	CAS_{12}	E11	FT	A10	C_9	C5	D_1
E2	S_{12}	K2	S_1	M5	B_6	M10	A_4	J12	CAS_{11}	D12	$CDEL_0$	B9	C_{10}	B4	D_0
E1	S_{11}	L1	S_0	N5	B_7	N11	A_3	J13	CAS_{10}	C13	$CDEL_1$	A9	C_{11}	A3	$\overline{END}$
F3	V_{DD}	M1	$\overline{OE}$	L6	GND	N12	A_2	H11	GND	B13	$CDEL_2$	C8	V_{DD}	A2	$DDEL_3$
F2	S_{10}	K3	$\overline{SWAP}$	M6	B_8	L10	A_1	H12	CAS_9	D11	$CDEL_3$	B8	D_{11}	C4	$DDEL_2$
F1	S_9	L2	$BDEL_0$	N6	B_9	M11	A_0	H13	CAS_8	C12	$\overline{ENC}$	A8	D_{10}	B3	$DDEL_1$
G2	S_8	N1	$BDEL_1$	M7	B_{10}	N13	$\overline{ENA}$	G12	CAS_7	A13	C_0	B7	D_9	A1	$DDEL_0$

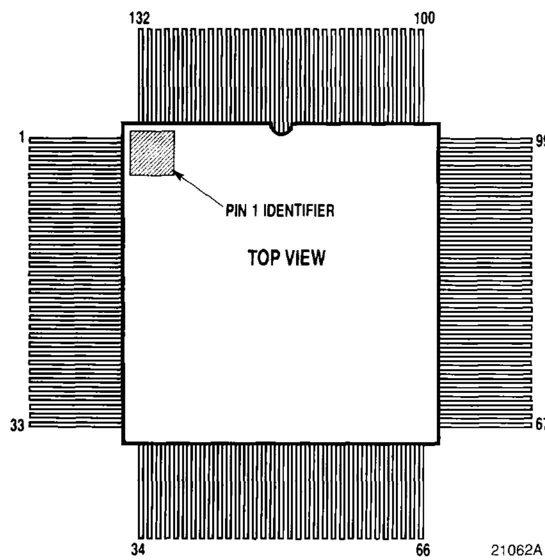
H

Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	23	S_3	45	B_7	67	NC	89	CAS_0	111	C_{11}
2	CLK	24	S_2	46	GND	68	$ADEL_3$	90	CASEN	112	V_{DD}
3	ACC	25	GND	47	B_8	69	$ADEL_2$	91	FT	113	D_{11}
4	NEG1	26	S_1	48	B_9	70	$ADEL_1$	92	$CDEL_0$	114	D_{10}
5	NEG2	27	S_0	49	B_{10}	71	$ADEL_0$	93	$CDEL_1$	115	D_9
6	RND	28	OE	50	V_{DD}	72	NC	94	$CDEL_2$	116	GND
7	S_{15}	29	SWAP	51	B_{11}	73	CAS_{15}	95	$CDEL_3$	117	D_8
8	S_{14}	30	$BDEL_0$	52	A_{11}	74	CAS_{14}	96	ENC	118	D_7
9	GND	31	$BDEL_1$	53	A_{10}	75	CAS_{13}	97	C_0	119	D_6
10	S_{13}	32	NC	54	A_9	76	CAS_{12}	98	NC	120	D_5
11	S_{12}	33	NC	55	A_8	77	CAS_{11}	99	NC	121	D_4
12	S_{11}	34	NC	56	A_7	78	CAS_{10}	100	NC	122	D_3
13	V_{DD}	35	$BDEL_2$	57	A_6	79	GND	101	C_1	123	D_2
14	S_{10}	36	$BDEL_3$	58	A_5	80	CAS_9	102	C_2	124	D_1
15	S_9	37	ENB	59	A_4	81	CAS_8	103	C_3	125	D_0
16	S_8	38	B_0	60	A_3	82	CAS_7	104	C_4	126	END
17	GND	39	B_1	61	A_2	83	CAS_6	105	C_5	127	$DDEL_3$
18	S_7	40	B_2	62	A_1	84	CAS_5	106	C_6	128	$DDEL_2$
19	S_6	41	B_3	63	A_0	85	CAS_4	107	C_7	129	$DDEL_1$
20	S_5	42	B_4	64	ENA	86	CAS_3	108	C_8	130	$DDEL_0$
21	V_{DD}	43	B_5	65	NC	87	CAS_2	109	C_9	131	NC
22	S_4	44	B_6	66	NC	88	CAS_1	110	C_{10}	132	NC



120 Pin Plastic Pin Grid Array – H5 Package



132 Leaded CERQUAD – L5 Package

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2249H5C	STD $-T_A=0°C$ to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2249H5C
TMC2249H5C1	STD $-T_A=0°C$ to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2249H5C1
TMC2249L5V	EXT $-T_C=-55°C$ to 125°C	MIL-STD-883	132 Leaded CERQUAD	2249L5V
TMC2249L5V1	EXT $-T_C=-55°C$ to 125°C	MIL-STD-883	132 Leaded CERQUAD	2249L5V1

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