

Description

The RoHS 6/6 compliant STC5423 is a single chip clock synchronization solution for applications in SDH/SETS, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813 option 1 and 2, G.8262 EEC option1 and 2, Telcordia GR1244 and GR253.

The STC5423 accepts 2 clock reference inputs and generates 9 synchronized clock outputs including two frame pulse outputs at 8kHz and 2kHz. Synchronized clock outputs may be programmed for a wide variety frequencies from 1MHz up to 156.25MHz, in 1kHz steps. Reference inputs are individually monitored for activity and quality. Reference selection may be automatic, manual, hard-wired manual.

Two independent timing generators, T0 and T4, may operate in the **Freerun**, **Synchronized**, **Pseudo Holdover** and **Holdover** mode. Each timing generator includes a DSP-based PLL. Synchronized mode is in external timing while freerun, pseudo holdover and holdover mode are in self-timing. DSP-based PLL technology removes any external part except the oscillator. It provides excellent performance and reliability to STC5423.

The STC5423 is clocked by an external oscillator (TCXO or OCXO). Using a well-chosen external oscillator ensures the STC5423 meet the required specifications and standards.

Features

- Complies with ITU-T G.813 opt1 and opt2, G.8262 EEC opt1 and opt2, Telcordia GR1244 and GR253 (Stratum3/4E/4/SMC)
- Two timing generators, T0 and T4; T4 may locks to T0's synchronized output
- Supports multiple master redundant application (T0 only)
- Supports 4 different frequencies of external oscillator: 10MHz, 12.8MHz, 19.2MHz, 20MHz
- Accepts 2 clock reference inputs
- Reference inputs are automatically frequency detected; each is monitored for activity and quality
- Supports automatic, manual, and hard-wired manual reference selection
- Outputs 9 synchronized clock outputs, including 2 frame pulse clocks
- 9 independent clock synthesizers
- Phase-align or hit-less reference locking/switching
- Programmable loop bandwidth, from 0.1Hz to 100Hz
- Programmable phase skew in synthesizer level
- Supports bus interface: Intel, Motorola, Multiplex, SPI
- Single 3.3V operation
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package

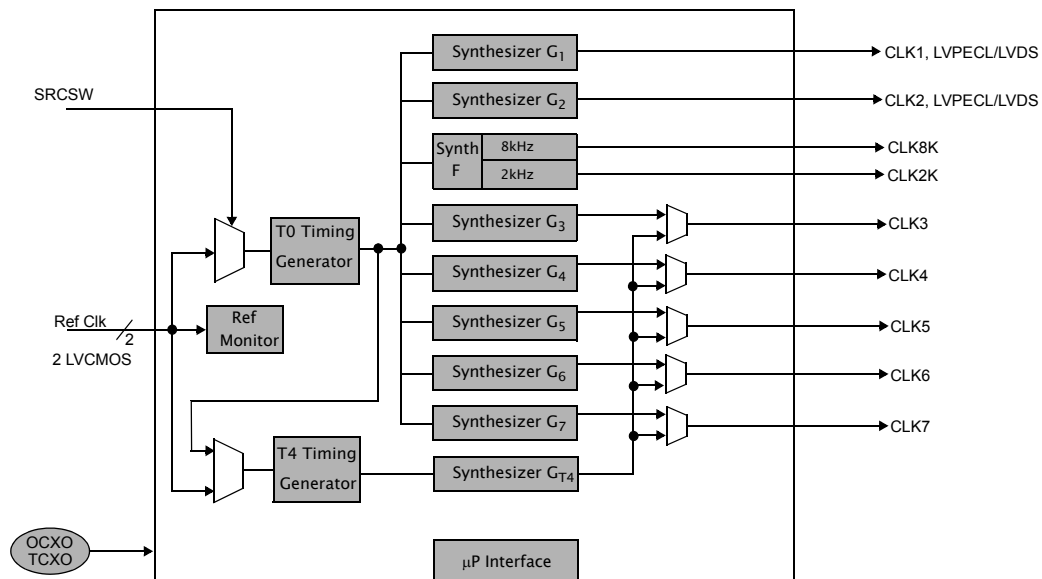


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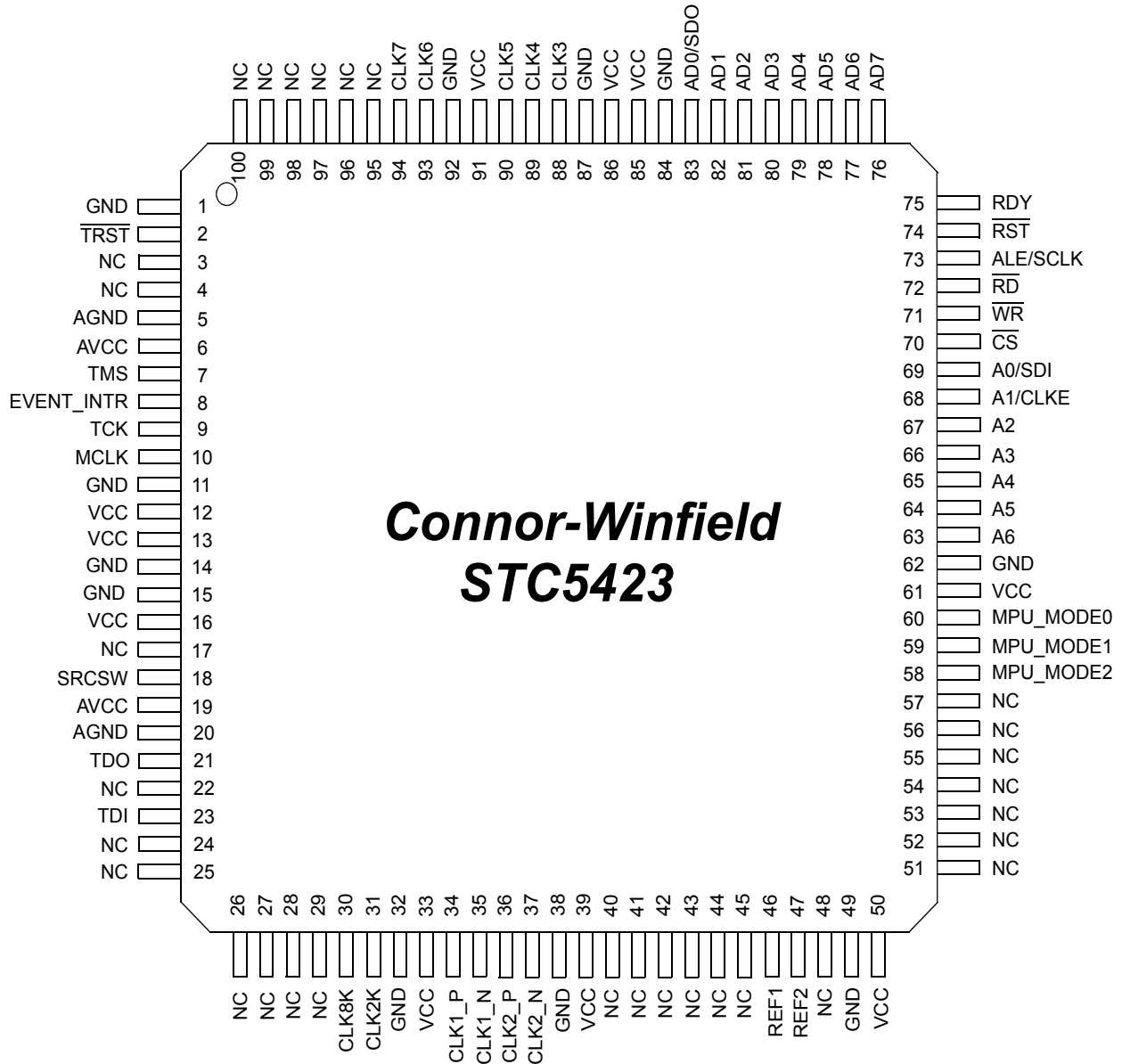
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STC5423 Pin Diagram (Top View)



STC5423 Pin Description

All I/O is LVCMOS, except for CLK1 and CLK2, which are LVPECL/LVDS.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
AVCC	6,19,		3.3V analog power input
AGND	5, 20,		Analog ground
VCC	12, 13, 16, 33, 39, 50, 61, 85, 86, 91		3.3V power input
GND	1, 11, 14, 15, 32, 38, 49, 62, 84, 87, 92		Digital ground
$\overline{\text{TRST}}$	2	I	JTAG boundary scan reset, active low
TCK	9	I	JTAG boundary scan clock
TMS	7	I	JTAG boundary scan mode selection
TDI	23	I	JTAG boundary scan data input
TDO	21	O	JTAG boundary scan data output
$\overline{\text{RST}}$	74	I	Active low to reset the chip
MCLK	10	I	Master clock input (TCXO or OCXO)
EVENT_INTR	8	O	Event interrupt
REF1	46	I	Reference input 1
REF2	47	I	Reference input 2
CLK1_P	34	O	Clock output CLK1 positive. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₁ . LVPECL or LVDS
CLK1_N	35	O	Clock output CLK1 negative. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₁ . LVPECL or LVDS
CLK2_P	36	O	Clock output CLK2 positive. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₂ . LVPECL or LVDS
CLK2_N	37	O	Clock output CLK2 negative. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₂ . LVPECL or LVDS
CLK3	88	O	Clock output CLK3. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₃ or Synthesizer G _{T4} (T4). LVCMOS.
CLK4	89	O	Clock output CLK4. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₄ or Synthesizer G _{T4} (T4). LVCMOS.
CLK5	90	O	Clock output CLK5. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₅ or Synthesizer G _{T4} (T4). LVCMOS.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
CLK6	93	O	Clock output CLK6. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₆ or Synthesizer G _{T4} (T4). LVCMOS.
CLK7	94	O	Clock output CLK7. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G ₇ or Synthesizer G _{T4} (T4). LVCMOS.
CLK8K	30	O	8kHz frame pulse signal, 50% duty cycle or programmable pulse width (T0)
CLK2K	31	O	2kHz frame pulse signal, 50% duty cycle or programmable pulse width (T0)
SRCSW	18	I	Hard-wired manual reference input pre-selection
MPU_MODE0	60	I	Bus interface: Intel, Motorola, Multiplexed, SPI
MPU_MODE1	59	I	
MPU_MODE2	58	I	
\overline{CS}	70	I	SPI bus chip select
\overline{WR}	71	I	Write access for Intel, Motorola and Multiplex bus interface
\overline{RD}	72	I	Read access for Intel and Multiplex bus interface
ALE/SCLK	73	I	ALE: Address latch enable for Multiplex bus interface SCLK: Clock edge selection for SPI
RDY	75	O	Ready/Data Acknowledge for Intel, Motorola and Multiplex bus interface
A0/SDI	69	I	A0~A6: Address pins for bus interface Intel and Motorola SDI: SPI bus data input CLKE: Clock edge selection for SPI
A1/CLKE	68	I	
A2	67	I	
A3	66	I	
A4	65	I	
A5	64	I	
A6	63	I	
AD0/SDO	83	I/O	
AD1	82	I/O	
AD2	81	I/O	
AD3	80	I/O	
AD4	79	I/O	
AD5	78	I/O	
AD6	77	I/O	
AD7	76	I/O	

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
NC	3, 4, 17, 22, 24, 25, 26, 27, 28, 29, 40, 41, 42, 43, 44, 45, 48, 51, 52, 53, 54, 55, 56, 57, 95, 96, 97, 98, 99, 100		No connection. Pins are recommended to be tied to ground

Register Map

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID = 0x5423
0x01				
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision number
0x07	Fill_Obs_Window	3-0	R/W	Activity monitor: Leaky bucket fill observation window
0x08	Leak_Obs_Window	3-0	R/W	Activity monitor: Leaky bucket leak observation window
0x09	Bucket_Size	5-0	R/W	Activity monitor: Leaky bucket size
0x0A	Assert_Threshold	5-0	R/W	Activity monitor: Leaky bucket alarm assert threshold
0x0B	De_Assert_Threshold	5-0	R/W	Activity monitor: Leaky bucket alarm de-assert threshold
0x0C	Freerun_Cali	10-0	R/W	Freerun calibration, 2's complement, -102.4 to +102.3 ppm, step in 0.1ppm
0x0D				
0x0E	Disqualification_Range	9-0	R/W	Reference disqualification range, 0 ~ 102.3 ppm. The value is also specified as pull-in range
0x0F				
0x10	Qualification_Range	9-0	R/W	Reference qualification range, 0 ~102.3 ppm.
0x11				
0x12	Qualification_Soaking_Time	5-0	R/W	Reference qualification soaking time, 0 ~ 63s
0x13	Ref_Index_Selector	3-0	R/W	Determines which reference data is shown in register Ref_Info.
0x14	Ref_Info	15-0	R	Frequency offset and frequency of the reference with index selected by register Ref_Infor_Selector
0x15				
0x16	Ref_Activity	1-0	R	Reference activity for reference 1 and 2
0x18	Ref_Qual	1-0	R	Reference 1 and 2 qualification
0x1A	Interrupt_Event_Status	7-0	R/W	Interrupt events
0x1B	Interrupt_Event_Enable	7-0	R/W	Selects which of interrupt events will assert pin EVENT_INTR
0x1C	Interrupt_Config	1-0	R/W	Pin EVENT_INTR configuration and idle mode
0x1D	Hard_Wired_Switch_Pre_Selection	7-0	R/W	Pre-selects reference number 1 and reference number 2 for hard-wired manual switch mode
0x1E	SRCSW_Status	0	R	Indicates the status of pin SRCSW
0x1F ¹	T0/T4_Tag_Select	0	R/W	Selects registers between T0 and T4 for register 0x20 - 0x3F
0x20	Control_Mode	7, 5-2, 0	R/W	Frame phase align, Mode of Holdover, Revertive, Manual/Auto, OOP, SRCSW
0x21	Loop_Bandwidth	7-0	R/W	Loop bandwidth selection
0x22	Auto_Elect_Ref	3-0	R	Indicates the reference input elected by auto reference elector
0x23	Manual_Select_Ref	3-0	R/W	The reference specified by users for manual selection mode
0x24	Selected_Ref	3-0	R	Indicates the PLL current selected reference
0x25	Device_Holdover_History	31-0	R	Device Holdover History
0x26				
0x27				
0x28				
0x29	Long_Term_Accu_History	31-0	R	Long term Accumulated History
0x2A				
0x2B				
0x2C				

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x2D	Short_Term_Accu_History	31-0	R	Short term Accumulated History
0x2E				
0x2F				
0x30				
0x31	User_Specified_History	31-0	R/W	User programmed holdover history
0x32				
0x33				
0x34				
0x35	History_Ramp	7-0	R/W	Controls long term history and short term history accumulation bandwidth and the locking stage's frequency ramp control
0x36	Ref_Priority_Table	7-0	R/W	REF1-2 selection priority
0x3C	PLL_Status	7-6, 4-0	R	PLL status. SYNC, LOS, LOL, OOP, SAP, DHT, HHA
0x3D	Holdover_Accu_Flush	0-0	W	Flush/reset the long-term history and the device holdover history
0x3E	PLL_Event_Out	7-0	R/W	PLL event out (TBD)
0x3F	PLL_Event_In	7-0	R/W	PLL event in: Relock
0x4A	Synth_Index_Select	3-0	R/W	Determines which synthesizer is selected for setting frequency value and adjusting phase skew
0x4B	Synth_Freq_Value	17-0	R/W	Selects synthesizer frequency value from 1MHz to 156.25MHz, in 1kHz steps, based on which synthesizer index is selected at the register Synth_Index_Select
0x4C				
0x4D				
0x4E	Synth_Skew_Adj	11-0	R/W	Adjusts phase skew for the synthesizer, based on which synthesizer index is selected at the register Synth_Index_Select
0x4F				
0x50	CLK1/2_Signal_Level	1-0	R/W	Selects the signal level (LVPECL or LVDS) for clock outputs CLK1 and CLK2
0x51	CLK1_Sel	1-0	R/W	Selects synthesizer G ₁ or enable tri-state for CLK1
0x52	CLK2_Sel	1-0	R/W	Selects synthesizer G ₂ or enable tri-state for CLK2
0x53	CLK3_Sel	1-0	R/W	Selects synthesizer (G ₃ or G _{T4}) or enable tri-state for CLK3
0x54	CLK4_Sel	1-0	R/W	Selects synthesizer (G ₄ or G _{T4}) or enable tri-state for CLK4
0x55	CLK5_Sel	1-0	R/W	Selects synthesizer (G ₅ or G _{T4}) or enable tri-state for CLK5
0x56	CLK6_Sel	1-0	R/W	Selects synthesizer (G ₆ or G _{T4}) or enable tri-state for CLK6
0x57	CLK7_Sel	1-0	R/W	Selects synthesizer (G ₇ or G _{T4}) or enable tri-state for CLK7
0x59	CLK8K_Sel	6-0	R/W	8kHz frame pulse clock output duty cycle and frame edge selection
0x5A	CLK2K_Sel	6-0	R/W	2kHz frame pulse clock output duty cycle and frame edge selection
0x70	Field_Upgrade_Status	2-0	R	Indicates the status of field upgrade process
0x71	Field_Upgrade_Data	7-0	R/W	Loads 7600 bytes of firmware configuration data
0x72	Field_Upgrade_Count	12-0	R	Counts byte numbers that have been loaded
0x73				
0x74	Field_Upgrade_Start	7-0	W	Writes three values consecutively to start the field upgrade process
0x7F	MCLK_Freq_Reset	7-0	R	Select the frequency of the external oscillator

Note 1: Timing generator T0 and T4 share register 0x20 ~ 0x3F. Register 0x1F selects between T0 and T4 for the sharing registers 0x20~0x3F.

Master Clock Frequency

The STC5423 supports four different frequencies of master clock. Initial default accepted frequency of MCLK is 12.8MHz. Besides, the STC5423 provides three additional options: 10MHz, 19.2MHz, and 20MHz. See Chip Master Clock for details.

Table 3: Master Clock Frequency

12.8MHz	Initial default frequency
10MHz	Optional accepted frequency
19.2MHz	
20MHz	

Input and Output Frequencies

Table 4: Acceptable Ref Input frequencies (REF1 and REF2)

Frequency
8 kHz
64 kHz
19.44 MHz
38.88 MHz
77.76 MHz
1.544 MHz
2.048 MHz
6.48 MHz
8.192 MHz
16.384 MHz
25 MHz
50 MHz
125 MHz

Table 5: Available Clock Output Frequencies

CLK	CLK Level	Synthesizer	Clock Output Frequency Range
CLK1	LVPECL/LVDS	G ₁	1MHz ~ 156.25MHz, in 1kHz steps
CLK2	LVPECL/LVDS	G ₂	1MHz ~ 156.25MHz, in 1kHz steps
CLK8K	LVCMOS	F	8kHz
CLK2K		F	2kHz
CLK3	LVC MOS	G ₃ (T0) or G _{T4} (T4)	1MHz ~ 156.25MHz, in 1kHz steps
CLK4	LVC MOS	G ₄ (T0) or G _{T4} (T4)	1MHz ~ 156.25MHz, in 1kHz steps
CLK5	LVC MOS	G ₅ (T0) or G _{T4} (T4)	1MHz ~ 156.25MHz, in 1kHz steps
CLK6	LVC MOS	G ₆ (T0) or G _{T4} (T4)	1MHz ~ 156.25MHz, in 1kHz steps
CLK7	LVC MOS	G ₇ (T0) or G _{T4} (T4)	1MHz ~ 156.25MHz, in 1kHz steps

Clock Output Jitter

Table 6: Clock Output Jitter

Clock Output	Frequency	RMS jitter ² (Typical)	pk-pk jitter ² (10 ⁻¹²) (Typical)	
	(MHz)	(ps)	(ps)	(UI)
CLK1/CLK2 (LVPECL)	156.25	13	210	0.03
	155.52	13	210	0.03
	125	13	210	0.03
	77.76	13	210	0.02
CLK3~CLK7 (LVCMOS)	77.76	19	330	0.03
	38.88	16.5	280	0.01
	19.44	15	230	0.005
	25	13	180	0.005
	2.048	11	180	0.0004
	1.544	11	160	0.0003

Note 2: Filter bandwidth is from 12kHz to Frequency/2

General Description

Application

The STC5423 is a single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813 (option1 and option 2), G.8262 EEC (option1 and option2), Telcordia GR1244, and GR253 (Stratum3/4E/4/SMC). Its highly integrated design implements all necessary reference selection, monitoring, filtering, synthesis, and control functions. An external oscillator (e.g., high precision OCXO or TCXO) completes a system level solution (see Functional Block Diagram, Figure 1). The STC5423 has four different frequencies options of external oscillator. The STC5423 supports multiple-master operation for redundant application.

Overview

The STC5423 accepts 2 reference inputs and generates 9 synchronized clock outputs, including 2 frame pulse clock outputs at 8kHz and 2kHz. Two independent PLL-based timing generators, T0 and T4, provide the essential functions for Synchronous Equipment Timing Sources (SETS). T0 controls synthesizer G₁~G₇, and synthesizer F. T4 controls synthesizer G_{T4}. Clock outputs CLK₁~CLK₇ can be derived from synthesizer G₁~G₇, respectively. CLK₃~CLK₇ can also be derived from synthesizer G_{T4} from T4 path. Frame pulse clock outputs are derived from synthesizer F. The STC5423 incorporates a microprocessor interface, which can be configured for all common microprocessor interface types.

Chip Master Clock

The STC5423 operates with an external oscillator (e.g., OCXO or TCXO) as its master clock. The device supports four different frequencies of master clock: Initial default accepted frequency 12.8MHz and three additional options at 10MHz, 19.2MHz, and 20MHz.

Reference Inputs

The STC5423 accepts 2 reference inputs which support frequencies range from 8kHz to 125MHz. The two reference inputs are continuously frequency auto-detected, activity and quality monitored. The activity

monitoring is implemented with a programmable leaky bucket algorithm. A reference is designated as “qualified” if it is selected and its fractional frequency offset is within the programmed range for a programmed soaking time. An auto reference elector elects the most appropriate one from the reference inputs according to the revertivity status, and each reference’s priority and qualification. If none of the reference inputs is qualified, holdover or freerun mode will be elected depending on the availability of the holdover history.

Reference selection may be automatic, manual, or hard-wired manual. In automatic reference selection mode, the most appropriate one elected from the auto reference elector will be the selected reference input. In manual reference selection mode, user may specify any of the reference inputs as the selected reference input for external timing or holdover/freerun for self-timing. In hard-wired manual mode, user can fast switch using control pin SRCSW between two pre-programmed reference inputs. The reference input elected from the auto reference elector will not affect the selected reference input in manual or hard-wired manual mode.

In manual reference selection mode, the timing generator T4 may accept T0’s synchronized output as its input.

Timing Generator and Operation Mode

The STC5423 includes two independent timing generators, T0 and T4, to provide the essential functions for SETS. Each timing generator can individually operate in **Freerun**, **Synchronized**, **Pseudo-Holdover** and **Holdover** mode. A timing generator is in either external-timing or self-timing. In external timing, PLL of the timing generator phase-locks to the selected external reference input. In self-timing, the PLL simply tunes the clock synthesizers to a given fractional frequency offset. Synchronized mode is in external timing. PLL’s loop bandwidth may be programmed individually to vary the timing generator’s filtering function. Conversely, freerun, pseudo-holdover and holdover modes are all in self-timing. When selected reference and previous holdover history are unavailable, such as in system’s initialization stage, freerun mode may be entered or used. When selected reference input is unavailable but a long-

term holdover history accumulated in previous synchronized mode is available, holdover mode may be entered or used. STC5423 may enter pseudo-holdover using short-term frequency history. In STC5423, the freerun clock is derived from the MCLK (external oscillator) and digitally calibrated to compensate the external oscillator's accuracy offset. STC5423 also allow users to program and manipulate the holdover history accumulators.

Phase Synchronization

In synchronized mode, the phase relationship between the selected reference input and the clock output maybe phase arbitrary or frame phase align for T0 timing generator. Frame phase align is enabled when bit Phase Align of the register **Control Mode** is set to "Align" and the reference input is at 8kHz. For timing generator T4, the phase relationship is only phase arbitrary. It allows an arbitrary phase relation to be rebuilt during reference switch to minimize the downstream clock's phase transient. In this condition, the STC5423 can provide **hit-less** switching if both references are traced to the same clock source (e.g., PRC).

A maximum frequency ramp may be programmed to minimize the ramp changing of fractional frequency offset in case the new selected reference is not traced to the same source. This feature restrains the frequency transient which may cause the pull-out-of-lock of the downstream network elements.

Clock Outputs

The STC5423 generates 9 synchronized clock outputs: 2 differential clock outputs (LVPECL or LVDS) CLK1 and CLK2, 5 clock outputs CLK3 to CLK7 (LVCMOS), one 8kHz and one 2kHz frame pulse clock outputs (LVCMOS). CLK1~CLK7 can be derived from synthesizer G1~G7 through T0 path, respectively, in which CLK3~CLK7 can also be derived from synthesizer G_{T4} through T4 path. Frame pulse clock outputs are derived from synthesizer F. See Figure 1 for functional details. Frequency of clock outputs CLK1~CLK7 is programmable by programming frequency of synthesizers from 1MHz up to 156.25MHz, in 1kHz step. Each of the synthesizers has different default frequency value. The STC5423 allows the user to program the phase skew of each clock synthesizer, up and down 50ns in roughly 0.024ns step to adjust the phase of clock outputs.

Frame pulse clock synthesizer generates frame pulse clock outputs CLK8K and CLK2K at frequency of 8kHz and 2kHz. The duty-cycle of CLK8K and CLK2K is programmable.

Redundant Design

Timing generator T0 supports **multiple-master** operation for redundant applications to allow system protection against the failure of the single part.

In multiple-master configuration, all units work as masters. If the bit Phase Align of the register **Control Mode** is set to "Align" and frequency of the selected reference input is 8kHz, frame phase alignment is enabled for T0 timing generator only. Clock outputs of all the units will keep in frame phase alignment. In order to meet same synchronization requirement, each unit should use same parameter setup including loop bandwidth.

Control Interfaces

The STC5423's control interfaces are composed of hardwire control pins and the bus interface. They provide application access to the STC5423's internal control and status registers. This bus interface may be configured among four type of micro-controller interfaces, 3 of them are in parallel (Intel, Motorola, Multiplexed) and one in serial (SPI). The selection of the bus interface is pin-controlled.

Field Upgradability

The STC5423 supports Field Upgradability which allows the user to load size of 7600 byte firmware configuration data (provided as per request) via bus interface. It provides the user a flexible field solution for different applications.

Advantage and Performance

The kernel of each timing generator is a DSP-based PLL. In STC5423, all internal modules are either digital or numerical, including the phase detectors, filters, and clock synthesizers. The revolutionary pure-digital design makes the timing generator become an accurate and reliable **deterministic** system. This modern technology removes any external part except the external oscillator. It provides excellent performance and reliability to STC5423. A well-chosen oscillator will make STC5423 meet all the synchronization requirements. Short-term stability associated with the

desired loop bandwidth is a more important factor than aging projection and thermal response that should be considered when select an appropriate oscillator.

Detailed Description

The STC5423 is a single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. The revolutionary pure-digital internal modules, DSP-based PLL and clock synthesizer are used in the device so that the overall characteristics are more stable compared to traditional method.

Chip Master Clock

The device operates with an external oscillator (e.g., OCXO or TCXO) as its master clock, connected to the **MCLK** input, pin 10. Generally, user should select an oscillator has great stability and low phase noise as the master clock (MCLK).

The STC5423 supports four different accepted frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency of MCLK for STC5423 is 12.8MHz. When 10MHz, 19.2MHz, or 20MHz is selected as the frequency of MCLK, the user must write register **MCLK Freq Reset** three times consecutively, with no intervening read/writes from/to other register. An internal soft-reset will occur after writes completed. The accepted frequency of MCLK input returns to 12.8MHz following any regular reset. See register **MCLK Freq Reset** for details.

In the meantime, the STC5423 allows user to read three values at the register **MCLK Freq Reset**: FRQID, COUNT, and ID Written Value.

FRQID

Indicates the ID of the frequency of MCLK that the STC5423 currently accept.

COUNT

Indicates how many times the register **MCLK Freq Reset** has been written to.

ID Written Value

Indicates the ID of associated value that is being written to the register **MCLK Freq Reset**.

See the register **MCLK Freq Reset** for more details.

Freerun Clock

The STC5423 has an internal freerun clock synthesized from the MCLK. The frequency offset of the internal freerun clock can be calibrated by writing to the register **Freerun Cali**. It has the stability of the external TCXO/OCXO. The calibration offset may be programmed from -102.4 to +102.3ppm, in 0.1ppm steps, in 2's complement. This feature allow the user can digitally calibrate the freerun clock without physically adjusting the local oscillator.

Operation Mode

The STC5423 includes two timing generators, T0 and T4 timing generators. Each timing generator has its own PLL and can be individually operate in either external-timing or self-timing. In external timing, PLL of a timing generator phase-locks to a reference input. In self-timing, PLL simply operates with the external oscillator (MCLK). The STC5423 supports three operation modes: *freerun* (self-timing), *synchronized* (external-timing), *pseudo-holdover* (self-timing) and *holdover* (self-timing).

Freerun Mode

Freerun mode is typically used during system's initialization stage when none of reference inputs is available and the clock synchronization has not been achieved. The clock output generated from the STC5423 in freerun mode is based on the internal freerun clock which is synthesized from MCLK. Frequency of the internal freerun clock can be calibrated by writing to the register **Freerun Cali**.

Synchronized Mode

In synchronized mode, the built-in PLL of the timing generator locks to the selected reference input. Each timing generator's loop bandwidth is independently programmable from 0.1Hz to 100Hz by writing to the register **Loop Bandwidth**. The noise transfer function of the PLL is determined accordingly by the loop bandwidth and has maximum gain under 0.2dB. In synchronized mode, the phase relationship between the reference is arbitrary or aligned for T0 timing generator and only arbitrary for T4 timing generator.

Pseudo-Holdover Mode

In pseudo-holdover mode, the clock is synthesized from the MCLK and an accumulated short-term history. This history is accumulated by a built in programmable short-term history accumulator consecutively,

which presents the most recently updated fractional frequency offset of the synchronous clock output of each timing generator. The user can read the short-term history from register **Short Term Accu History**.

Holdover Mode

Holdover mode is used when none of reference inputs is available and the holdover history has been built. In this condition, the frequency offset of the clock output is maintained closely to previous value generated when the selected reference input was valid. User can select either device holdover history or user specified holdover history at the register **Control Mode** in holdover mode.

PLL Event In

The STC5423 provides direct communication with the PLL's timing generator by writing to the register **PLL Event In**. Following events can be triggered:

- Relock. PLL starts a relock process if this event is triggered

Frequency and Phase Transient

Severe frequency and phase transients of the clock output will cause lost of lock or buffer overflow/underflow on downstream circuit. By providing programmable maximum slew rate and phase rebuild function, both frequency and phase transient of the STC5423's clock output is controlled to minimize the impact on downstream circuits.

Frequency Transient

The STC5423 smoothly control the frequency transient on the clock output. During reference input switching or operation mode switching (etc., switch into/out freerun or holdover mode), if the clock output prior to switching has different frequency offset than the desired clock output, it smoothly approach to desired frequency offset with a maximum acceleration/deceleration rate by writing to the register **History Ramp**. The maximum slew rate can be programmed as 1.0, 1.5, 2.0 ppm/second. With a limited acceleration/deceleration, the pull-in process may last longer. However, it will minimize the frequency transient impact to the downstream clock and ensure meeting components' frequency impact tolerance.

Phase Transient

The STC5423 minimize the variation of the phase transient on the clock output when a phase hit occurs on the selected reference input. The overshoot in the clock output's phase transient response will be a small amount under 2%.

During reference input switching or recovering from LOS/LOL condition, the phase transient may also occurred on the clock output. The STC5423 can minimize it with a phase rebuild function. In synchronized mode, the phase relationship between the reference input and the clock output can be programmed to phase arbitrary or frame phase align at the register **Control Mode**. If phase arbitrary is selected, a phase rebuild function is performed before locking to the new/recovered reference input. His-less switching is achieved with this function and the phase hit to downstream circuits is eliminated. If frame phase align is selected and the reference input is at 8kHz, the clock output is in frame phase alignment with the 8kHz reference input. Only T0 timing generator supports frame phase alignment.

History of Fractional Frequency Offset

The STC5423 monitors and tracks the fractional frequency offset between the clock output and MCLK. The history data of the frequency offset is used by clock synthesizers to generate desire outputs while the timing generator is pending for reference input availability. Two weighted 3rd order low-pass filter are used internally as two history accumulators: the short term history accumulator and the long term history accumulator. A mature long term history is stored and further updated as device holdover history. It is used when the STC5423 operates in holdover mode. Short-term history is used in pseduo holdover mode. In addition, the STC5423 allows user to program an user specified history as needed of the application.

Short-Term History

Short-term history is an average frequency offset between the clock output and MCLK which is filtered internally using a weighted 3rd order low-pass filter with the small time constant. The -3dB filter response point can be programmed from 0.16Hz to 1.3Hz by writing to the register **History Ramp** register. Short-term history can be read from the register **Short_Term_Accu_History**. Typically, short-term

history is used by clock synthesizer in two conditions: First, it is used in between the transition of two different operation modes; second, it is used if LOS occurs when the STC5423 operates in synchronized mode with manually reference selection. In addition, short-term history is provided to perform failure diagnostics and evaluations.

Long-Term History

Long-term history is an average frequency offset between the clock output and MCLK which is filtered internally using a weighted 3rd order low-pass filter with the long time constant. The -3 dB filter response point can be programmed from 0.15mHz to 1.3Hz by writing to the register **History Ramp**. The history value can be read from the register **Long Term Accu History**.

Device Holdover History

Device holdover history is the history data used when the STC5423 runs in holdover mode. It is acquired from the long term history previously described. In synchronized mode, when timing generator's PLL has locked to the selected reference input for over 15 minutes, the long term history is stored and further updated as the device holdover history. If LOS or LOL occurs, the device holdover history will stay at the latest updated value until re-enter the synchronized mode and the PLL locks to the new selected reference input for another 15 minutes. Set bit HO_Usage of the register **Control Mode** to select using device holdover history. Its value can be read from the register **Device Holdover History**.

User-Specified History

The STC5423 allows user to provide the history data created from their own sophisticated history accumulation algorithms by writing to the register **User Specified History**. Set bit HO_Usage of the register **Control Mode** to select using user specified holdover history. Its value can be also read from the register **User Specified History**.

Phase-Locked Loop Status Details

The register **PLL Status** contains the detailed status of the PLLs, including the signal activity of the selected reference, the synchronization status, and the availability of the holdover histories.

SYNC bit

In external-timing mode, this bit indicates the achievement of synchronization. This bit will not be asserted in self-timing mode.

LOS bit

In external-timing mode, this bit indicates the loss of signal on the selected reference. This bit will not be asserted in self-timing mode.

LOL bit

In external-timing mode, the bit will be set if the PLL fails to achieve or maintain lock to the selected reference. This bit will not be asserted in self-timing mode. This bit is also not complementary to the SYNC bit. Both bits will not be asserted when the PLL is in the pull-in process. The pull-in process usually occur when switch to a new selected reference or recover from the LOS/LOL.

OOP bit

This bit indicates that the selected reference is out of the pull-in range. This is meaningful only if in external-timing mode. This bit will not be asserted in self-timing mode. The frequency offset is relative to the digitally calibrated freerun clock.

SAP bit

This bit when set indicates that the PLL's output clocks have stopped following the selected reference because the frequency offset of the selected reference is out of pull-in range (OOP). The user can write to the register **Control Mode** to program whether the PLL should follow the selected reference outside of the specified pull-in range or just stay within the pull-in range boundary.

DHT bit

This bit indicates whether the device holdover history is tracking on the current selected reference (updating by the long-term history).

HHA bit

This bit indicates the availability of the holdover history, which may be either the user provided history or the device holdover history.

Reference Inputs Details

The STC5423 accepts 2 external reference inputs at 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, 50MHz or 125MHz. The two reference inputs are LVCMOS and monitored continu-

ously for frequency, activity and quality. Each timing generator may select any of the reference inputs when the device is in external timing mode. T4 may accept T0's output as its input via internal feedback path.

Input Frequency and Frequency Offset Detection

Input frequencies are detected automatically in STC5423. The detector operates to detect the frequency of reference inputs continuously. Any carrier frequency change will be detected within 1ms. Each input is also monitored for frequency offset between input and the internal freerun clock. The frequency offset is a key element to determine qualification of the reference inputs. See register **Ref Info Selector** and **Ref Info**.

Activity Monitoring

Activity monitoring is also a consecutive process which is used to identify if the reference input is in normal. It is accomplished with a leaky bucket accumulation algorithm, as shown in Figure 2. The "leaky bucket" accumulator has a fill observation window that may be set from 1 to 16ms, where any hit of signal abnormality (or multiple hits) during the window increments the bucket count by one. The leak observation window is 1 to 16 times the fill observation window. The leaky bucket accumulator decrements by one for each leak observation window that passes with no signal abnormality. Both windows operate in a consecutive, non-overlapping manner. The bucket accumulator has alarm assert and alarm de-assert thresholds that can each be programmed from 1 to 64.

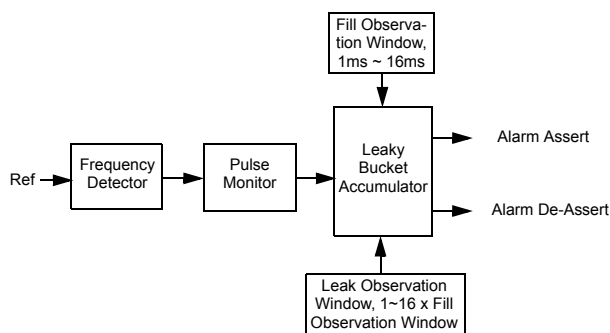


Figure 2: Activity Monitor

Applications can write to the following registers to configure the activity monitor: **Fill Obs Window**,

Leak Obs Window, Bucket Size, Assert Threshold, and De Assert Threshold.

The activity monitor can be bypassed by setting the bucket size to 0. This operation de-asserts the activity alarms of all the references. A non-zero bucket size must be greater than or equal to the alarm assert threshold value. The alarm assert threshold value must be greater than the alarm de-assert threshold value and less than or equal to the bucket size value. Attempted writes of invalid values will be ignored. Therefore, user must carefully plan an appropriate sequence of writes when re-configure the activity monitor. See the registers **Bucket Size**, **Assert Threshold** and **De Assert Threshold** for details.

Alarms appear in the **Refs Activity** register. A "1" indicates activity, and a "0" indicates an alarm, no activity. Note that if a reference is detected as a different frequency, the leaky bucket accumulator is set to the bucket size value and the reference will become inactive immediately.

Input Qualification

A selected reference is "qualified" if it passes the activity evaluation and its frequency offset is within the programmed qualification range for over a pre-programmed soaking time.

A reference qualification range may be programmed up to 102.3 ppm by writing to register **Qualification Range**, and a disqualification range set up to 102.3 ppm, by writing to the register **Disqualification Range**. The qualification range must be set less than the disqualification range. Additionally, qualification soaking time may be programmed from 0 to 63 seconds by writing to the register **Qualification Soaking Time**. The pull-in range is the same as the disqualification range.

The frequency offset of each reference is relative to the internal freerun clock may be read by selecting the reference in the register **Ref Info Selector** and then reading the offset value from the register **Ref Info**.

Figure 3 shows the reference qualification scheme. A reference is qualified if it has no activity alarm and is continuous within the qualification range for over the qualification soaking time. An activity alarm or frequency offset beyond the disqualification range will disqualify the reference. It may then be re-qualified if

the activity alarm is off and the reference is within the qualification range for more than the qualification time.

The reference qualification status of each reference may then be read from the register **Ref Qual**.

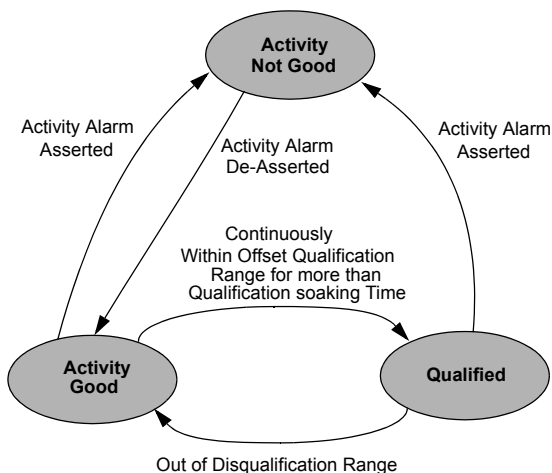


Figure 3: Reference Qualification Scheme

Automatic Reference Election Mechanism

The STC5423 has an auto reference elector always elect the most appropriate candidate input from the reference inputs according to the revertivity status, and each reference’s priority and qualification. This mechanism operates independent of reference selection mode. In other word, regardless what the current reference selection mode is, the auto reference elector always work in this mechanism. The detail description of the reference selection mode is in following sections.

The reference priority is indicated in the reference priority table which is shown in the register **Priority Table** individually for each timing generator. Each reference has one entry in the table, which may be set to value from 0 to 15. ‘0’ revokes the reference from the election, while 1 to 15 set the priority, where ‘1’ has the highest and ‘15’ has the lowest priority. The highest priority pre-qualified reference then is a candidate reference input selected by the automatic reference elector. If multiple references share the same priority, the one that has been qualified for the longest time will be elected. If the current highest priority reference input fails, the next-highest priority reference is elected.

In order to avoid disturbance of the clock output, the candidate reference elected by automatic reference elector should be handled in two different mode: revertive mode and non-revertive mode. The mode is determined by either enabling or disabling the “revertive” bit of the register **Control Mode** to “1” for revertive or to “0” for non-revertive operation.

In revertive mode, the automatic reference elector will pre-empted the current elected reference if the new reference has higher priority.

In non-revertive mode, the current elected reference will not be pre-empted by any new reference until it is disqualified.

If there is no elected reference available, freerun or holdover will be elected by the automatic reference elector depending on the holdover history availability.

Figure 4 shows the operation states for automatic reference elector.

Automatic Reference Selection

The T0 and T4 timing generators may be individually operated in automatic input reference selection mode. The mode is selected at the register **Control Mode**.

In automatic reference selection mode, the selected reference is the same reference elected by the automatic reference elector. The automatically selected reference for each PLL may be read from the register **Auto Select Ref**.

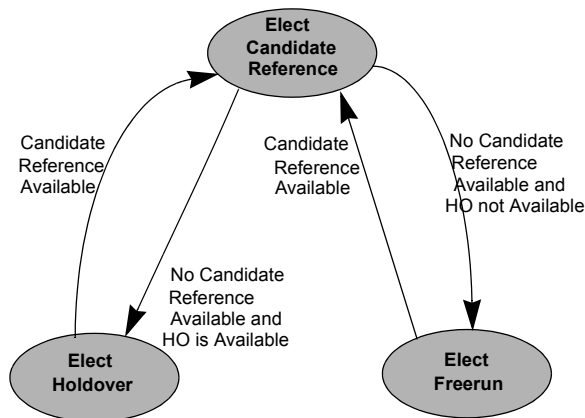


Figure 4: Automatic Reference Elector States

Manual Reference Selection Mode

In manual reference selection mode, the user may select the reference manually. This mode is selected at the **Control Mode**. The reference is selected by writing to the register **Manual Select Ref**. The user may also has the device enter freerun, pseudo-holdover or holdover manually by writing to the register **Manual Select Ref**. In addition, T4 may select T0's output as the selected reference.

Hard-Wired Manual Reference Selection

Besides the manual reference selection mode, the STC5423 provides a special mode to switch between two pre-selected reference directly from a dedicated pin SRC SW. The two pre-selected references are configured at the register **Hard Wired Switch Pre Selection**. It can make the device enter the freerun, pseudo-holdover or holdover by writing to the register **Hard Wired Switch Pre Selection**. In this mode, the pin SRC SW operates as a simple switch by setting high or low. The status of pin SRC SW can be read from the register **SRC SW Status**. Hard-wired manual reference selection is for T0 timing generator only.

Clock Outputs Details

The STC5423 generates 2 synchronized differential (LVPECL or LVDS) clock outputs: CLK1 and CLK2; 5 LVC MOS clock outputs: CLK3~CLK7, one 8kHz and one 2kHz frame pulse clock. Figure 5, Figure 6, and Figure 7 respectively shows the clock output section for CLK1/CLK2, CLK8K/CLK2K, and CLK3~CLK7. Each output has individual clock output section consist of synthesizer and clock generator. Clock generator of CLK1 or CLK2 has a LVPECL/LVDS driver to produce differential output. Clock generators of CLK3~CLK7 include a mux and a LVC MOS signal driver. Clock generator of frame output CLK8K and CLK2K consist of a duty cycle controller and a LVC MOS drive.

Clock Synthesizers

The STC5423 has 9 clock synthesizers, which of 8 is disciplined by the timing generator T0: synthesizer G₁~G₇ and one frame pulse clock synthesizer F. T4 disciplines a clock synthesizer G_{T4}. Clock synthesizers G₁~G₇ produce frequencies from 1MHz to 156.25MHz, in 1kHz steps. Phase skew of these synthesizers are all programmable individually up and

down 50ns. CLK1 and CLK2 are derived from synthesizer G₁ and G₂. CLK3 ~ CLK7 can be derived from synthesizer G₃~G₇ respectively, also can be derived from synthesizer G_{T4}, which is the synthesizer of timing generator T4 path. Synthesizer F produces frame pulse at 8kHz and 2kHz with 50% duty cycle or programmable pulse width.

Clock Generators

Clock generator of CLK1 or CLK2 consist of a LVPECL/LVDS signal driver. The signal level of clock outputs CLK1 and CLK2 can be programmed to either LVPECL or LVDS. Clock generators of CLK3~CLK7 consist of a mux and a LVC MOS driver. Each mux determines which synthesizer is selected for generator to output clock. CLK3~CLK7 are all LVC MOS. Signal level is driven from LVC MOS driver in clock generator. The clock generator of frame pulse output CLK8K and CLK2K contains a duty cycle controller and a LVC MOS driver. The duty cycle is programmable at the register **CLK8K Sel** and **CLK2K Sel**.

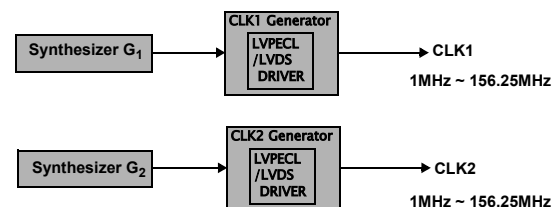


Figure 5: Output Clocks CLK1 and CLK2

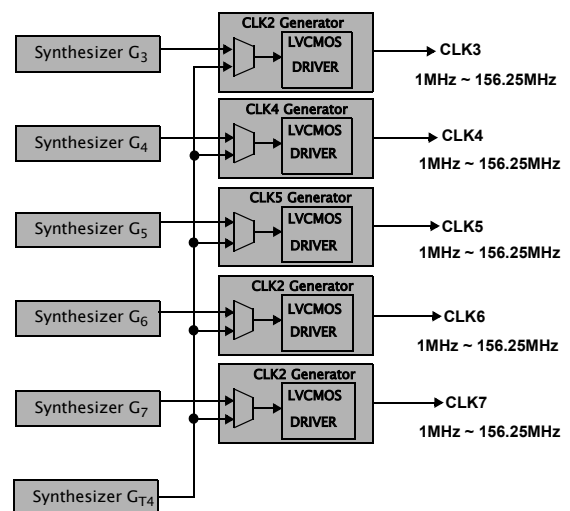


Figure 6: Output Clocks CLK3~CLK7

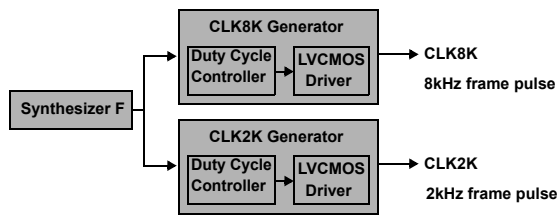


Figure 7: Output Clocks CLK8K and CLK2K

Clock Output Phase Alignment

If a clock output is derived from T0's synthesizer (synthesizer $G_1 \sim G_7$) and has frequency that is integer multiple of 8kHz, it is in phase alignment with the frame pulse output CLK8K when synthesizer phase skew is not programmed. Clock output derived from T4's synthesizer G_{T4} has no phase alignment relationship with CLK8K.

Synthesizer Skew Programming

The STC5423 allows user to program the phase skew of each clock synthesizer, up and down 50ns in roughly 0.024ns steps. Since each of clock outputs is dedicate derived from its synthesizer respectively, adjust phase skew of the synthesizer will provide the associated clock output a phase skew adjustment. Phase skew of the 9 synthesizers may be programmed at the register **Synth Skew Adj.**

Clock Outputs

Available frequencies of CLK1~CLK7 are from 1MHz to 156.25MHz, in 1kHz steps. Phase skew is adjustable at the associate synthesizer level. Two clock outputs, CLK8K and CLK2K, generate two frame pulse clock at 8kHz and 2kHz.

Redundant Application

Timing generator T0 supports multiple-master operation for redundant applications to allow system protection against single part failure.

Multiple Master Configuration

In multiple-master configuration, every unit locks to the same reference input and has consistent loop bandwidth settings. To enable phase alignment for all master's outputs, bit Phase Align of the register **Control Mode** is set to "Align" and the reference input has to be 8kHz.

Event Interrupts

The STC5423 events shown following below are interrupt events might occurred.

- Qualification status of the reference inputs change
- Selected reference of timing generator T0 changes in automatic reference selection
- Selected reference of timing generator T4 changes in automatic reference selection
- PLL status of timing generator T0 changes
- PLL status of timing generator T4 changes
- Out-Event of timing generator T0 asserts
- Out-Event of timing generator T4 asserts

The interrupt events can be read from the register **Interrupt Status**. Each bit indicates one events. The associate bit of the register **Interrupt Status** will not be changed automatically when the event is cleared. Therefore, the user need write '1' to the associate bit to erase the event.

The STC5423 has a pin EVENT_INTR (pin 8) for indicating the event interrupt occurrence. The pin may be wired to user's micro-controller. User can program the register **Interrupt Mask** to decide which of interrupt events will send an alarm to the micro-controller by asserting the EVENT_INTR pin. User can program at the register **Interrupt Configuration** to specify the logic level (active high or low) of the pin EVENT_INTR when it's trigged by the interrupt event. User may also program the register **Interrupt Configuration** to define pin states as tri-state or logic inactive when no interrupt event occurs.

Field Upgradability

The STC5423 supports field upgradability which allows the user to load size of 7600 byte firmware configuration data (provided as per request) via bus interface. Field upgrade can only be performed at least 3ms after reset.

1. User may read Bit READY of the register **Field Upgrade Status** to check if field upgrade is ready to start.
2. To begin the field upgrade, write to register **Field Upgrade Start** three times consecutively, with no intervening read/writes from/to other registers, see the register **Field Upgrade Start** for details.

3. Once the field upgrade process begins, the STC5423 is hold for data loading. Write 7600 bytes firmware configuration data to the register **Field Upgrade Data** one byte at a time to complete data loading. User can read the same register for the written byte. But no matter how many times the user read, only the last written byte will be read from the register.

4. Read the register **Field Upgrade Count** for how many bytes of configuration data has been loaded. Bit Load_Compelet of the register **Field Upgrade Status** will indicate whether the 7600 bytes loading is complete and meanwhile bit CHECKSUM will indicate the loading is failed or succeed. See register description of **Field Upgrade Status** for details.

Processor Interface Descriptions

The STC5423 supports four common microprocessor control interfaces: SPI, Motorola, Intel, and Multiplex. The control interface mode is selected with the MPU_MODE(0/1/2):

MPU_MODE2 (Pin 58)	MPU_MODE1 (Pin 59)	MPU_MODE0 (Pin 60)	Bus Mode
0	0	1	Reserved
0	1	0	Multiplex
0	1	1	Intel
1	0	0	Motorola
1	0	1	SPI

The following sections describe each bus mode's interface timing:

SPI Bus Mode

The SPI interface bus mode uses the \overline{CS} , SCLK, SDI, SDO pins, with timing as shown in Figure 8, Figure 9 and Figure 10. For read operation, serial data output can be read out from the STC5423 on either the rising or falling edge of the SCLK. The edge selection depends on pin CLKE logic level.

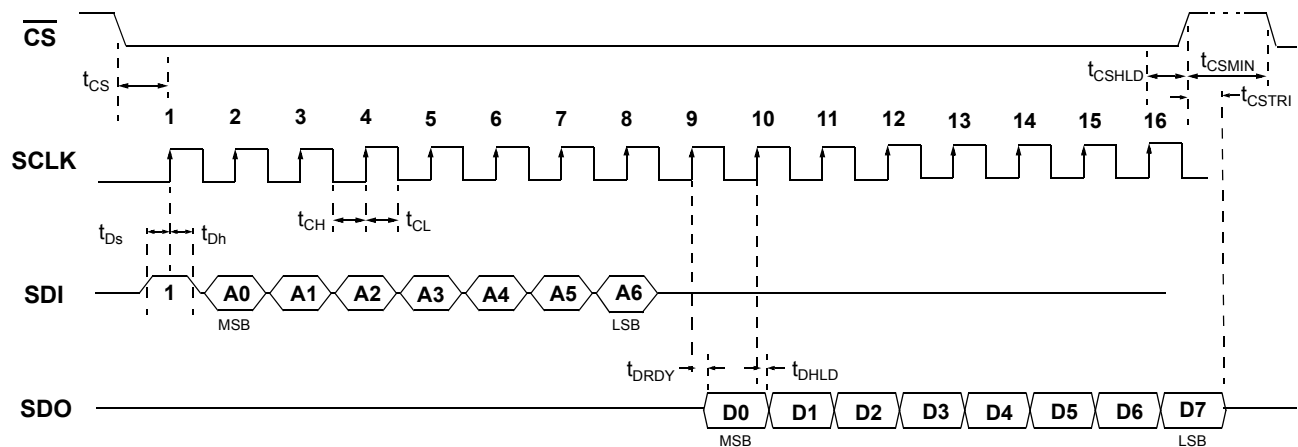


Figure 8:SPI Bus Timing, Read access (Pin CLKE = Low)

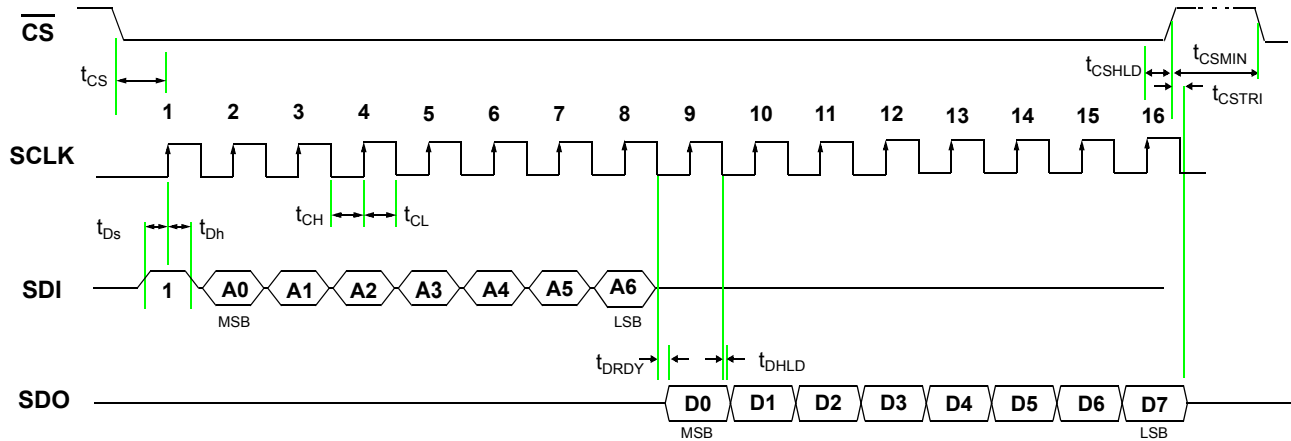


Figure 9: SPI Bus Timing, Read access (Pin CLKE = High)

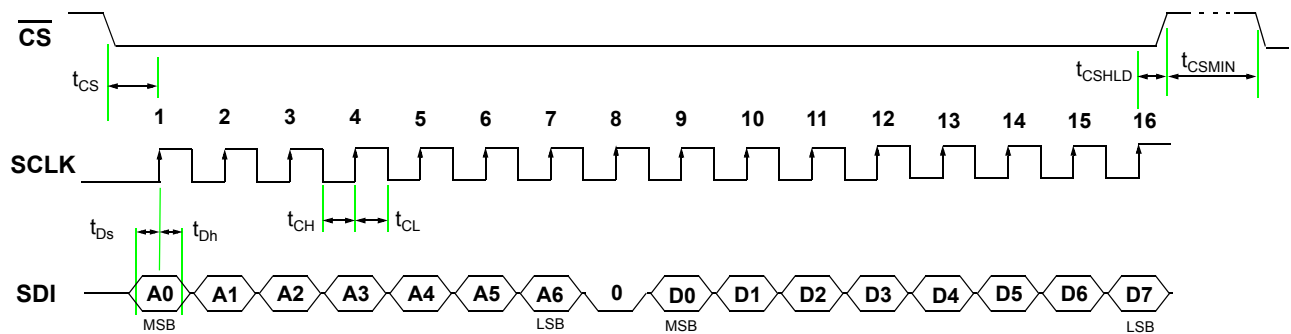


Figure 10: SPI Bus Timing, Write access

Table 7: SPI Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	CS low to SCLK high	10		ns
t_{CH}	SCLK high time	25		ns
t_{CL}	SCLK low time	25		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHL}	Data hold	3		ns
t_{CSHLD}	Chip select hold	30		ns
t_{CSTRI}	Chip select to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Motorola Bus

In Motorola mode, the device will interface to 680xx type processors. The \overline{CS} , \overline{WR} , A(0-6), AD(0-7) and RDY pins are used. Timing is as follows in Figure 11 and Figure 12:

Motorola Bus Timing

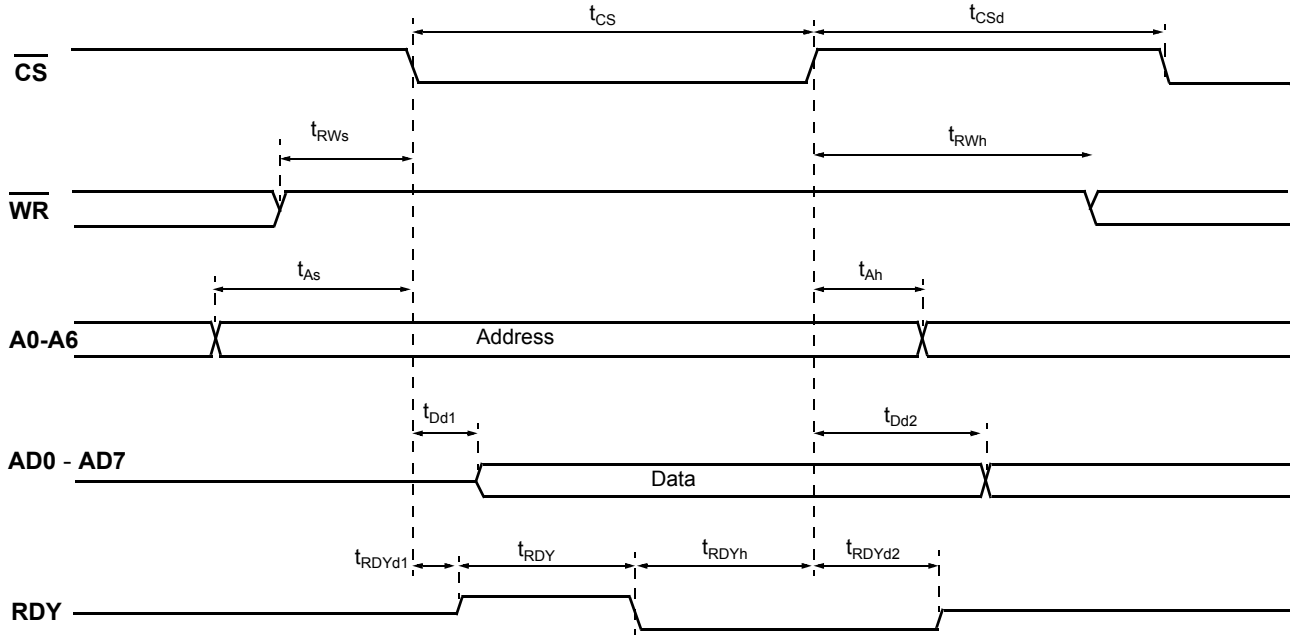


Figure 11: Motorola Bus Read Timing

Table 8: Motorola Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{CS}	CS low time	50		ns
t_{CSd}	CS minimum high time between reads/writes	50		ns
t_{RWs}	Read/write setup time	0		ns
t_{RWh}	Read/write hold time	0		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Dd1}	Data valid delay from CS low		50	ns
t_{Dd2}	Data high-z delay from CS high		10	ns
t_{RDYd1}	CS low to RDY high delay		13	ns
t_{RDY}	RDY high time	37	50	ns
t_{RDYh}	CS hold after RDY low	0		ns
t_{RDYd2}	RDY high-z delay after CS high		9	ns

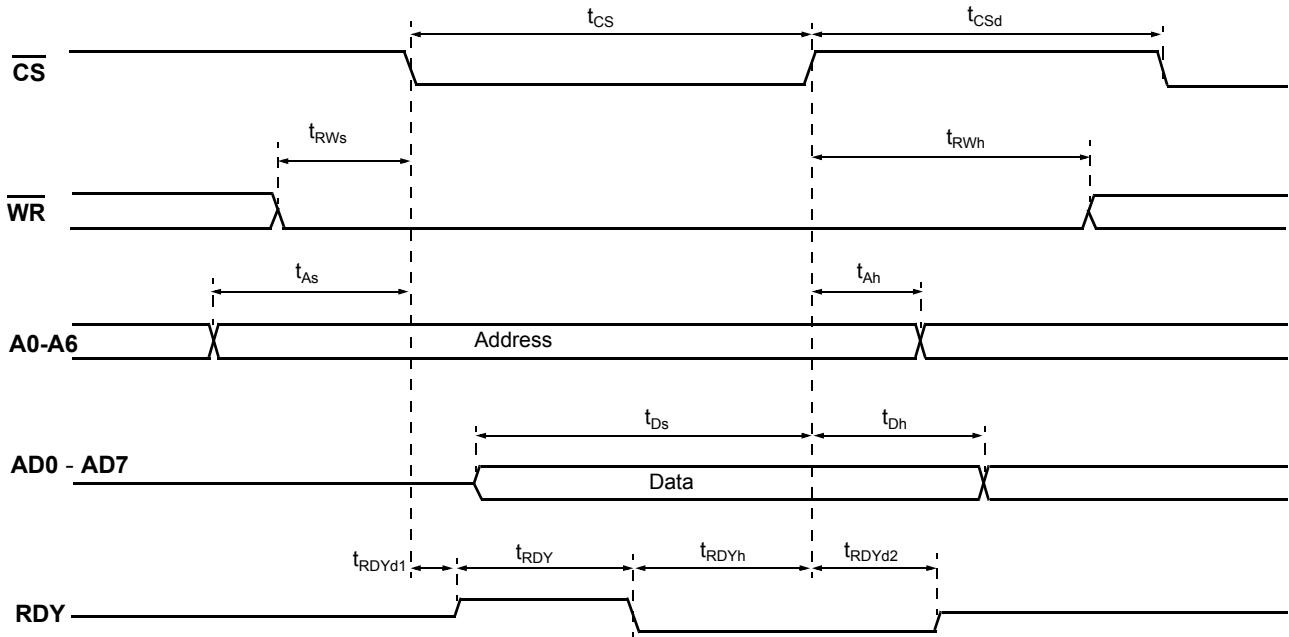


Figure 12: Motorola Bus Write timing

Table 9: Motorola Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{CS}	CS low time	50		ns
t_{CSd}	CS minimum high time between writes/reads	50		ns
t_{RWs}	Read/write setup time	0		ns
t_{RWh}	Read/write hold time	0		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Ds}	Data setup time before CS high	10		ns
t_{Dh}	Data hold time after CS high	10		ns
t_{RDYd1}	\overline{CS} low to RDY high delay		13	ns
t_{RDY}	RDY high time	37		ns
t_{RDYh}	CS hold after RDY low	0		ns
t_{RDYd2}	RDY high-z delay after CS high		7	ns

Intel Bus Mode

In Intel mode, the device will interface to 80x86 type processors. The \overline{CS} , \overline{WR} , \overline{RD} , A(0-6), AD(0-7), and RDY pins are used. Timing is as follows in Figure 13 and Figure 14:

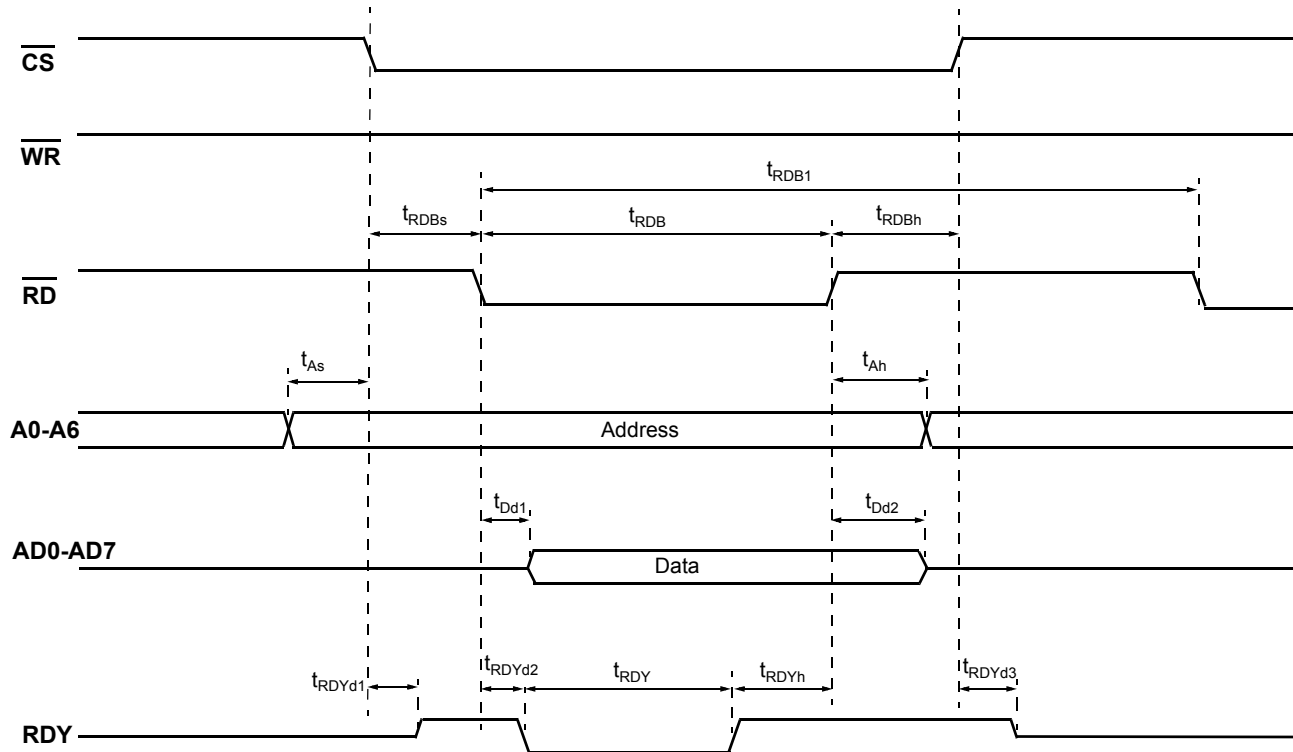


Figure 13: Intel Bus Read Timing

Table 10: Intel Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{RDBs}	Read setup time	0		ns
t_{RDB}	Read low time	40		ns
t_{RDBh}	Read hold time	0		ns
t_{RDB1}	Time between consecutive reads	50		ns
t_{As}	Address setup			ns
t_{Ah}	Address hold	0		ns
t_{Dd1}	Data valid delay from RD low		50	ns
t_{Dd2}	Data high-z delay from RD high		10	ns
t_{RDYd1}	\overline{CS} low to RDY high delay		13	ns
t_{RDYd2}	\overline{RD} low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	RD hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after \overline{CS} high		11	ns

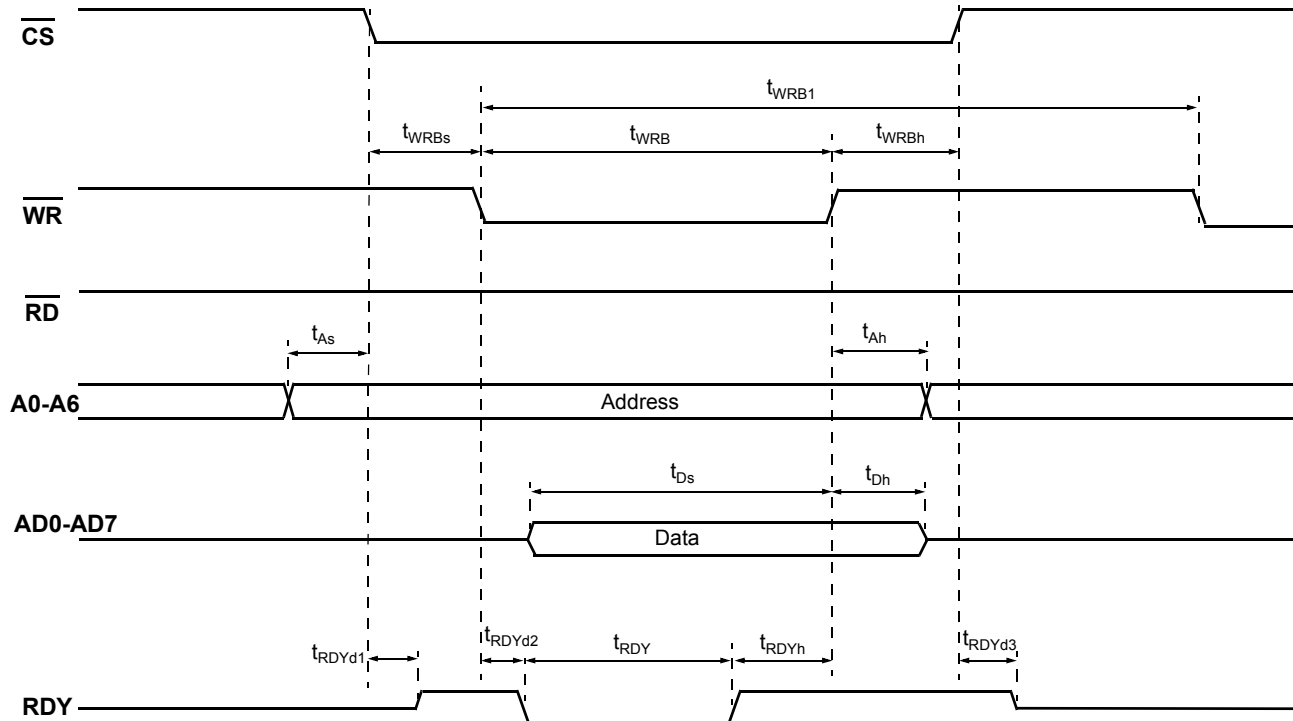


Figure 14: Intel Bus Write Timing

Table 11: Intel Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{WRBs}	Write setup time	0		ns
t_{WRB}	Write low time	40		ns
t_{WRBh}	Write hold time	0		ns
t_{WRB1}	Time between consecutive writes	50		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Ds}	Data setup time before WR high	10		ns
t_{Dh}	Data hold time after WR high	10		ns
t_{RDYd1}	CS low to RDY high delay		13	ns
t_{RDYd2}	WR low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	WR hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after CS high		10	ns

Multiplex Bus Mode

In multiplex bus mode, the device can interface with microprocessors which share the address and data on the same bus signals. The ALE, CS, WR, RD, AD(0-7), and RDY pins are used. Timing is as follows in Figure 15 and Figure 16.

Multiplex Bus Timing

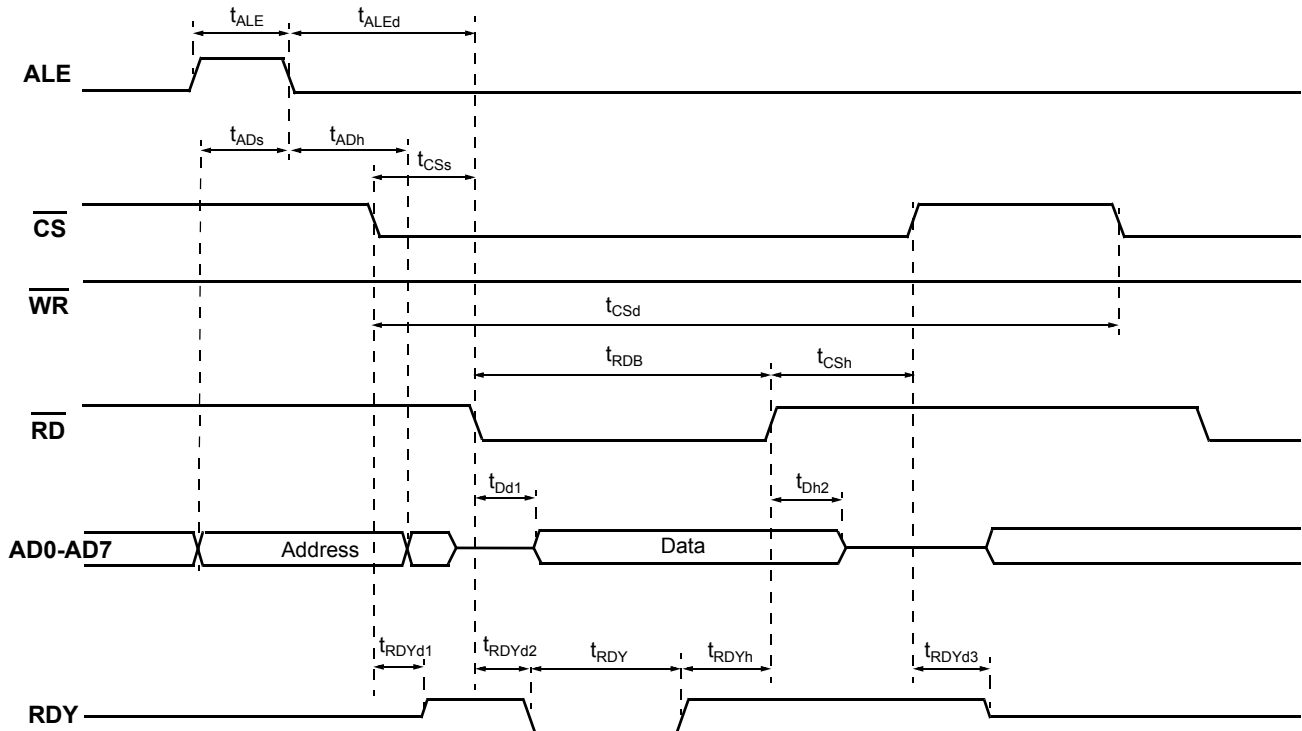


Figure 15: Multiplex Bus Read Timing

Table 12: Multiplex Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{ALE}	ALE high time	10		ns
t_{ALEd}	ALE falling edge to \overline{RD} low	0		ns
t_{ADs}	Address setup time	10		ns
t_{ADh}	Address hold time	10		ns
t_{CSs}	Read setup time	0		ns
t_{RDB}	Read time	40		ns
t_{CSh}	\overline{CS} hold time	0		ns
t_{CSd}	\overline{CS} delay for multiple read/writes	50		ns
t_{Dd1}	Data valid delay from \overline{RD} low		50	ns
t_{Dh2}	Data high-z from \overline{RD} high		10	ns
t_{RDYd1}	\overline{CS} low to RDY active		13	ns
t_{RDYd2}	\overline{RD} low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	\overline{RD} hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after CS high		10	ns

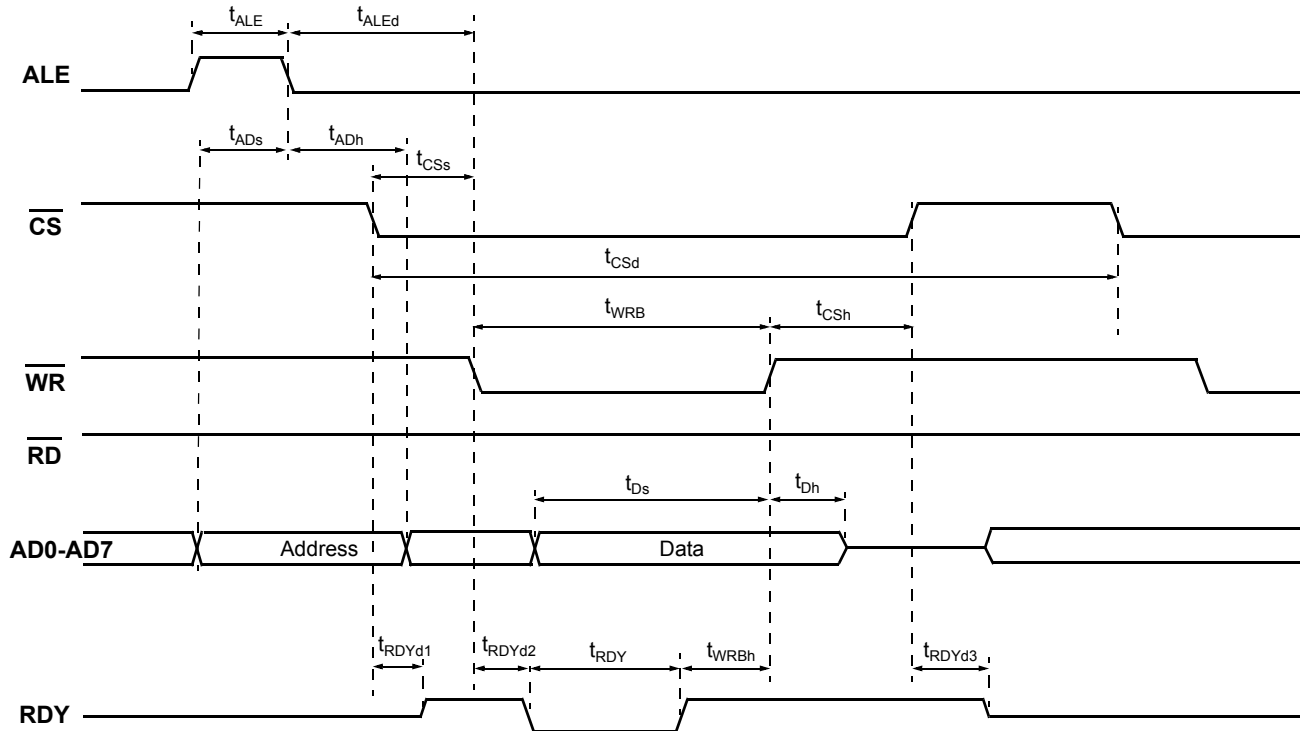


Figure 16: Multiplex Bus Write Timing

Table 13: Multiplex Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{ALE}	ALE high time	10		ns
t_{ALEd}	Time between ALE falling edge and WR low	0		ns
t_{ADs}	Address setup time	10		ns
t_{ADh}	Address hold time	10		ns
t_{CSs}	Write CS setup time	0		ns
t_{WRB}	Write time	40		ns
t_{CSh}	CS hold time	10		ns
t_{CSd}	CS delay for multiple write/reads	50		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{RDYd1}	CS low to RDY active		13	ns
t_{RDYd2}	WR low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{WRBh}	WR hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after CS high		9	ns

Register Descriptions and Operation

General Register Operation

The STC5423 device has 1, 2, 3, and 4 byte registers. One-byte registers are read and written directly. Multiple -byte registers must be read and written in a specific manner and order, as follows:

Multibyte register reads

A multibyte register read must commence with a read of the least significant byte first. This triggers a transfer of the remaining byte(s) to a holding register, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte(s) must be read consecutively with no intervening read/writes from/to other registers.

Multibyte register writes

A multi byte register write must commence with a write to the least significant byte first. Subsequent writes to the remaining byte(s) must be performed in ascending byte order, consecutively, with no intervening read/writes from/to other registers, but with no timing restrictions. Multibyte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x23							
0x01	0x54							

Indicates chip's ID number

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Indicates the revision number of STC5423

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

Indicates the sub-revision number of STC5423

Fill_Obs_Window, 0x07 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	Not used				Leaky bucket fill observation window, $m = 0 \sim 15$			

Sets the fill observation window size for the reference activity monitor to $(m+1)$ ms. The window size can be set from 1ms to 16ms.

Default value: $m = 0$, (1ms)

Leak_Obs_Window, 0x08 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x08	Not used				Leaky bucket leak observation window, $n = 0 \sim 15$			

Sets the leak observation window size of the reference activity monitor to $(n + 1)$ times the fill observation window size. The size can be set from 1 to 16ms times the fill observation window size.

Default value: $n = 3$,

Bucket_Size, 0x09 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	Not used		Leaky bucket size, 0 ~ 63					

Sets the leaky bucket size for the reference activity monitor. Bucket size equal to 0 will set the leaky bucket active monitor off, this de-asserts the activity alarms of all the references. The bucket size must be greater than or equal to the alarm assert value. Otherwise, the value will not be written to the register.

Default value: 20

Assert_Threshold, 0x0A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	Not used		Leaky bucket alarm assert threshold, 1 ~ 63					

Sets the leaky bucket alarm assert threshold for the reference activity monitor. The alarm assert threshold value must be greater than the de-assert threshold value and less than or equal to the bucket size value. Otherwise, the value will not be written to the register.

Default value: 15

De_Assert_Threshold, 0x0B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	Not used		Leaky bucket alarm de-assert threshold, 0 ~ 62					

Sets the leaky bucket alarm de-assert threshold for the reference activity monitor. The de-assert threshold value must be less than the assert threshold value. Otherwise, the value will not be written to the register.

Default value: 10

Freerun_Cali, 0x0C (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0C	Lower 8 bits of freerun calibration							

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0D	Not used					Upper 3 bits of freerun calibration		

Freerun calibration, from -102.4 to +102.3 ppm, in 0.1ppm steps, 2's complement.

Default value: 0

Disqualification_Range, 0x0E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0E	Lower 8 bits of disqualification range							
0x0F	Not used					Upper 2 bits of disqualification range		

Reference disqualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. This also sets the pull-in range. (See section Activity Monitoring and Input Qualification). New disqualification range must be greater than qualification range in the register **Qualification_Range**. Otherwise, the value will not be written to the register.

Default value: 110 (range = 11.0 ppm).

Qualification_Range, 0x10 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	Lower 8 bits of qualification range							
0x11	Not used					Upper 2 bits of qualification range		

Reference qualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. New qualification must be less than disqualification range. Otherwise, the value will not be written to the register.

Default value: 100 (range = 10.0 ppm).

Qualification_Soaking_Time, 0x12 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	Not used		Reference qualification soaking time 0 ~ 63 s					

Sets the soaking time for reference qualification, from 0 to 63s, in 1s step.

Default value: 10 (10s)

Ref_Info_Selector, 0x13 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	Not used				Ref1, Ref2			

Determines what reference information is indicated in register Ref_Info.

1 = Ref1, 2 = Ref2

Invalid values will not be written to the register.

Default value: 1

Ref_Info, 0x14 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	Lower 8 bits of frequency offset							
0x15	Reference frequency				Upper 4 bits of frequency offset			

Indicates the frequency offset and frequency of the reference input selected by the register **Ref_Info_Selector** (0x13). Frequency offset is from -204.7 to +204.7 ppm relative to calibrated freerun, in 0.1 ppm steps, 2's complement. A value of -2048 indicates the reference input is out of range.

The reference frequency is determined as follows ("Unknown" indicates a signal is present, but frequency is undetermined):

Field Value	Frequency
0	No signal
1	8 kHz
2	64 kHz
3	1.544 MHz
4	2.048 MHz
5	19.44 MHz
6	38.88 MHz
7	77.76 MHz
8	6.48MHz
9	8.192MHz
10	16.384MHz
11	25 MHz
12	50 MHz
13	125 MHz
14	Unknown
15	Reserved

Ref_Activity, 0x16 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	Not used						Ref 2	Ref 1

Indicates reference activity

0 = inactive, 1 = active

Ref_Qual, 0x18 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	Not used						Ref 2	Ref 1

Indicates reference qualification

0 = not qualified, 1 = qualified

Interrupt_Event_Status, 0x1A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A	Event 7: T4 timing generator's out-event occurred	Event 6: T4 PLL status changed	Event 5: T4 selected reference changed in auto selection mode	Event 4: T0 timing generator's out-event occurred	Event 3: T0 PLL status changed	Event 2: T0's selected reference changed in auto-selection mode	Event 1: Reserved	Event 0: Reference qualification status changed

Interrupt event status.

0 = no event, 1 = event occurred

Interrupts are cleared by writing "1" to the bit positions to be cleared.

Default value: 0

Interrupt_Event_Enable, 0x1B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	Event 7: T4 timing generator's out-event occurred	Event 6: T4 PLL status changed	Event 5: T4 selected reference changed in auto selection mode	Event 4: T0 timing generator's out-event occurred	Event 3: T0 PLL status changed	Event 2: T0's selected reference changed in auto-selection mode	Event 1: Reserved	Event 0: Reference qualification status changed

Selects which of events will assert the pin EVENT_INTR to active mode (See register **Interrupt_Config**).

0 = Mask out, 1 = Enable

Default value: 0

Interrupt_Config, 0x1C (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1C	Not used						Idle mode	Active signal level

Configures the interrupt pin EVENT_INTR.

Active signal level

Sets the signal level in active mode.

0 = active low. 1 = active high

Idle mode

Specify the state of pin EVENT_INTR when no interrupt event occurs.

0 = tri-state. 1 = logic inactive

Default value: 0

Hard_Wired_Switch_Pre_Selection, 0x1D (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	Pre-selected reference number 2				Pre-selected reference number 1			

Pre-selects reference number 1 and reference number 2 in hard-wired manual reference selection mode (T0 timing generator only). This mode is controlled by pin SRCSW. When pin SRCSW is LOW, reference number 1 is pre-selected. When pin SRCSW is HIGH, reference number 2 is pre-selected.

Field Value	Selection
0	Freerun
1	Ref1
2	Ref2
3~12	Reserved
13	Holdover
14	Pseudo Holdover
15	Reserved

Default value: 0

SRCSW_Status, 0x1E (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E	Not used							Pin Status

Indicates status of pin SRCSW.
0 = Low, 1 = High

Default value: 0

T0/T4_Tag_Select, 0x1F (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1F	Not used							Tag_Select

Selects between timing generator T0 and T4 for the sharing registers 0x20~0x3F.
0 = T0; 1 = T4

Default value: 0

Control_Mode, 0x20 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	Hard_Wired_Switch	Reserved	OOP	Ref_Sel_Mode	Revertive	HO_Usage	Reserved	Phase_Align

Mode control bits for individual timing generator. Select between timing generator T0 and T4 at the register **T0/T4_Tag_select** (0x1F).

Phase_Align (T0 timing generator only)

Determines the phase relationship is arbitrary or frame phase align.

0 = Arbitrary; 1 = Align (Frame phase align is only enabled when frequency of reference input is at 8kHz)

HO_Usage

Determines which holdover history is used.

0 = Device Holdover History (DHH); 1 = User specified history

Revertive

Selects the revertive mode or non-revertive mode of the auto-electror.

0 = Non-revertive; 1 = Revertive

Ref_Sel_Mode

Determines reference selection mode.

0 = Manual; 1 = Auto

This bit may be overridden by bit **Hard_Wired_Switch** of this register.

OOP

In manual mode, the selected reference is out of the pull-in range, as specified in the register

Disqualification_Range (0x10). OOP will determine if the reference is to be followed

0 = Follow, 1 = Stop following at pull-in range boundary

Hard_Wired_Switch (T0 timing generator only)

0 = Not Hard-wired Switch, selects reference in manual selection mode or auto selection mode

1 = Hard-wired Switch, selects reference in hard-wired manual selection mode by using control pin

SRCSW to fast manual switch between two pre-selected reference inputs. See the register

***Hard_Wired_Switch_Pre_Selection** (0x1D) for details.*

Default value: 0

Loop_Bandwidth, 0x21 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x21	Bandwidth select							

Sets each timing generator's loop bandwidth, select between timing generator T0 and T4 at the register **T0/T4_Tag_select** (0x1F):

Field Value	Bandwidth, Hz
0	103
1	52
2	27
3	13
4	6.7
5	3.4
6	1.7

Field Value	Bandwidth, Hz
7	0.84
8	0.42
9	0.21
10	0.10
255 ~ 11	Reserved

Default value: 6 (1.7Hz)

Auto_Elect_Ref, 0x22 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	Not used				Auto selected reference			

Indicates the auto-elect reference. The auto-elect reference is elected by the reference elector according to revertivity status, and each reference's priority and qualification. Reference auto-elect or keep electing the reference even though manual reference mode is selected.

Bit 3 ~ Bit 0	Selection
0	Freerun
1	Sync with Ref1
2	Sync with Ref 2
3~12	Reserved
13	Holdover
14 ~15	Reserved

Manual_Select_Ref, 0x23 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x23	Not used				Manually selected reference			

Selects the reference in manual reference selection mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1	Sync with Ref 1
2	Sync with Ref 2
3~12	Reserved
13	Holdover
14	Pseudo-Holdover
15	Reserved (for T0); Lock to T0 (for T4)

The register is read only in hard-wired manual switch mode. It indicates the current reference defined by pin SRCSW and the register **Hard_Wired_Switch_Pre_Selection** (0x1D).

Default value: 0

Selected_Ref, 0x24 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	Not used				Current selected reference			

Indicates the current selected reference.

Field Value	Current selected reference
0	Freerun
1	Sync with Ref 1
2	Sync with Ref 2
3~12	Reserved
13	Holdover
14	Pseudo-Holdover
15	Reserved (for T0); Lock to T0 (for T4)

Device_Holdover_History, 0x25 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x25	Bits 0 - 7 of 32 bit Holdover History							
0x26	Bits 8 - 15 of 32 bit Holdover History							
0x27	Bits 16 - 23 of 32 bit Holdover History							
0x28	Bits 24 - 31 of 32 bit Holdover History							

The accumulated device holdover history relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Long_Term_Accu_History, 0x29 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x29	Bits 0 - 7 of 32 bit Long Term History							
0x2A	Bits 8 - 15 of 32 bit Long Term History							
0x2B	Bits 16 - 23 of 32 bit Long Term History							
0x2C	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated holdover history relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Short_Term_Accu_History, 0x2D (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2D	Bits 0 - 7 of 32 bit Short term History							
0x2E	Bits 8 - 15 of 32 bit Short term History							
0x2F	Bits 16 - 23 of 32 bit Short term History							
0x30	Bits 24 - 31 of 32 bit Short term History							

Short term accumulated holdover history relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

User_Specified_History, 0x31 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x31	Bits 0 - 7 of 32 bit User Holdover History							
0x32	Bits 8 - 15 of 32 bit User Holdover History							
0x33	Bits 16 - 23 of 32 bit User Holdover History							
0x34	Bits 24 - 31 of 32 bit User Holdover History							

User specified holdover history relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Default value: 0

History_Ramp, 0x35 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x35	Long Term History Accumulator Bandwidth				Short Term History Accumulator Bandwidth		Ramp Control	

History accumulator holdover bandwidth and ramp controls.

Bits 7 ~ 4	Long Term History -3dB Bandwidth
0	4.9 mHz
1	2.5 mHz
2	1.2 mHz
3	0.62 mHz
4	0.31 mHz
5	0.15 mHz
6, 7	Reserved
8	1.3Hz
9	0.64Hz
10	0.32Hz
11	0.16Hz
12	79mHz
13	40mHz
14	20mHz
15	9.9mHz

Bits 3 ~ 2	Short Term History -3dB Bandwidth
0	1.3 Hz
1	0.64 Hz
2	0.32 Hz
3	0.16 Hz

Bits 1 ~ 0	Ramp control
0	No Control

Bits 1 ~ 0	Ramp control
1	1.0 ppm/sec
2	1.5 ppm/sec
3	2.0 ppm/sec

Default value: 0x27 (1.2mHz; 0.64Hz; 2ppm/sec)

Ref_Priority_Table, 0x36 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x36	Ref 2 Priority				Ref 1 Priority			

Reference priority selection for automatic reference elector. Lower values have higher priority:

Bits 3~0/Bits 7~4	Reference Priority
0	Revoke from auto reference elector
1 ~ 15	1 ~ 15

Default value: 0

PLL_Status, 0x3C (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3C	HHA	DHT	Reserved	SAP	OOP	LOL	LOS	SYNC

SYNC Indicates whether synchronization has been achieved

- 0 = *Not synchronized*
- 1 = *Synchronized*

LOS Loss of signal of the selected reference.

- 0 = *No Loss*
- 1 = *Loss (Indicate loss of signal, freerun, and holdover)*

LOL Loss of lock (Failure to achieve or maintain locking)

- 0 = *No loss of lock*
- 1 = *Loss of lock*

OOP Out of pull-in range. Indicate the frequency offset of the selected reference input is out of pull-in range.

- 1 = *Out of pull-in range*
- 0 = *In range*

SAP Indicates whether the clock output has stopped following the selected reference, caused by out of pull-in range. Refer to bit OOP of the register **Control_Mode** (0x20).

- 1 = *Stop following at pull-in range boundary*
- 0 = *Following*

DHT Device Holdover History Tracking

- 1 = *Device holdover history is being tracked*
- 0 = *Device holdover history is not tracked, the value based on the latest available history*

HHA Holdover History Available. Config the register **Control_Mode** (0x20) to select which of holdover history is used: Device Holdover History or User Specified History.
1 = Available
0 = Not available

Holdover_Accu_Flush, 0x3D (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3D	Not used							HO Flush

Writing to this register will perform a flush of the accumulated holdover history. Bit HO Flush determines which history is flushed.

HO Flush:

- 0 = Flush and reset long term holdover history to 0*
- 1 = Flush/reset both long term holdover history and the device holdover history to 0.*

PLL_Event_Out, 0x3E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3E	TBD							

Default value: 0

PLL_Event_In, 0x3F (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3F	Reserved							Relock

Writing 1 to trigger the event. If the event is acknowledged by the STC5423, event bit is cleared to be 0.

Event Relock:

Sets PLL to relock the selected reference input. If the device operates in phase-align mode, PLL reselects the frame edge, relocks and frame phase align to the reference input. If the device operates in non phase-align mode, PLL relocks to the reference input and restart phase rebuild process.

Default value: 0

Synth_Index_Select, 0x4A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4A	Synthesizer index selection for synthesizer frequency and phase skew adjustment							

Determines which synthesizer is selected for setting frequency value at the register **Synth_Freq_Value** (0x4B~0x4D) and adjusting phase skew at the register **Synth_Skew_Adj** (0x4E~0x4F). When value of written is 0, it can only adjust phase skew for synthesizer F at the register **Synth_Phase_Adj** (0x4E~0x4F). Since frequency of synthesizer F is fixed at 8kHz and 2kHz, the register **Synth_Freq_Value** (0x4B~0x4D) is not writable to set frequency for synthesizer F.

Field Value	Synthesizer
0	Synthesizer F
1	Synthesizer G ₁
2	Synthesizer G ₂
3	Synthesizer G ₃
4	Synthesizer G ₄
5	Synthesizer G ₅
6	Synthesizer G ₆
7	Synthesizer G ₇
8	Reserved
9	Synthesizer G _{T4}

Default value: 0

Synth_Freq_Value 0x4B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4B	Bits 0-7 of 18 bits Synthesizer Frequency Selection							
0x4C	Bits 15-8 of 18 bits Synthesizer Frequency Selection							
0x4D	Not used						Bits 17-16 of 18 bits Synthesizer Frequency Selection	

Selects synthesizer frequency value from 1MHz to 156.25MHz, in 1kHz steps, based on which synthesizer index is selected at register **Synth_Index_Select** (0x4A). See register description of the register **Synth_Index_Select**. If index of synthesizer F is selected at the register **Synth_Index_Select**, this register is read only.

Default value varies with synthesizer index selection at the register **Synth_Index_Select**, refer to table below:

Synthesizer Index Selection	Default Value
Synthesizer G ₁	155520 (155.52MHz)
Synthesizer G ₂	125000 (125MHz)
Synthesizer G ₃	19440 (19.44MHz)
Synthesizer G ₄	38880 (38.88MHz)
Synthesizer G ₅	2048 (2.048MHz)
Synthesizer G ₆	25000 (25MHz)
Synthesizer G ₇	50000 (50MHz)
Synthesizer G _{T4}	2048 (2.048MHz)

Synth_Skew_Adj, 0x4E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4E	Lower 8 bits of Synthesizer Phase Skew Adjustment							
0x4F	Not used				Higher 4 bits of Synthesizer Phase Skew Adjustment			

Phase skew adjust for synthesizers based on which synthesizer index is selected at the register **Synth_Index_Select**. See description of the register **Synth_Index_Select**. The adjustment is from -6400/128 ns to 6396.875/128 ns, which is -50ns ~ 49.976 ns, in 3.125/128 ns steps, 2's complement.

Default value: 0 (For all the synthesizers)

CLK1/2_Signal_Level 0x50 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x50	Not used						CLK2 Signal Level	CLK1 Signal Level

Selects the signal level for clock outputs CLK1 and CLK2.

0 = LVPECL, 1 = LVDS

Default value: 0

CLK1_Sel, 0x51(R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x51	Not used						CLK1 Synthesizer Select	

Selects clock output CLK1 derived from synthesizer G₁ or put in tri-state.

Bits 2 ~ 0	CLK1 Synthesizer Select
0	Put CLK1 in tri-state mode
1	Synthesizer G ₁
2	Put CLK1 in tri-state mode
3	Put CLK1 in tri-state mode

Default value: 0

CLK2_Sel, 0x52(R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x52	Not used						CLK2 Synthesizer Select	

Selects clock output CLK2 derived from synthesizer G₂ or put in tri-state.

Bits 2 ~ 0	CLK2 Synthesizer Select
0	Put CLK2 in tri-state mode
1	Synthesizer G ₂
2	Put CLK2 in tri-state mode
3	Put CLK2 in tri-state mode

Default value: 0

CLK3_Sel, 0x53 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x53	Not used						CLK3 Synthesizer Select	

Selects the clock output CLK3 derived from synthesizer G_3 (T0) or synthesizer G_{T4} (T4). Signal level of CLK3 is LVCMOS.

Bits 1 ~ 0	CLK3 Synthesizer Select
0	Put CLK3 in tri-state mode
1	Synthesizer G_3 (T0)
2	Reserved
3	Synthesizer G_{T4} (T4)

Default value: 0

CLK4_Sel, 0x54 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x54	Not used						CLK4 Synthesizer Select	

Selects the clock output CLK4 derived from synthesizer G_4 (T0) or synthesizer G_{T4} (T4). Signal level of CLK4 is LVCMOS.

Bits 1 ~ 0	CLK4 Synthesizer Select
0	Put CLK4 in tri-state mode
1	Synthesizer G_4 (T0)
2	Reserved
3	Synthesizer G_{T4} (T4)

Default value: 0

CLK5_Sel, 0x55 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x55	Not used						CLK5 Synthesizer Select	

Selects the clock output CLK5 derived from synthesizer G_5 (T0) or synthesizer G_{T4} (T4). Signal level of CLK5 is LVCMOS.

Bits 1 ~ 0	CLK5 Synthesizer Select
0	Put CLK5 in tri-state mode

Bits 1 ~ 0	CLK5 Synthesizer Select
1	Synthesizer G ₅ (T0)
2	Reserved
3	Synthesizer G _{T4} (T4)

Default value: 0

CLK6_Sel, 0x56 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x56	Not used						CLK6 Synthesizer Select	

Selects the clock output CLK6 derived from synthesizer G₆ (T0) or synthesizer G_{T4} (T4). Signal level of CLK6 is LVCMOS.

Bits 1 ~ 0	CLK6 Synthesizer Select
0	Put CLK6 in tri-state mode
1	Synthesizer G ₆ (T0)
2	Reserved
3	Synthesizer G _{T4} (T4)

Default value: 0

CLK7_Sel, 0x57 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x57	Not used						CLK7 Synthesizer Select	

Selects the clock output CLK7 derived from synthesizer G₇ (T0) or synthesizer G_{T4} (T4). Signal level of CLK7 is LVCMOS.

Bits 1 ~ 0	CLK7 Synthesizer Select
0	Put CLK7 in tri-state mode
1	Synthesizer G ₇ (T0)
2	Reserved
3	Synthesizer G _{T4} (T4)

Default value: 0

CLK8K_Sel, 0x59 (R/W)

CLK2K_Sel, 0x5A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59		Invert	Duty Cycle Select					
0x5A		Invert	Duty Cycle Select					

Selects duty cycle of the 8kHz and 2kHz frame clock for T0 timing generator. Both clock outputs CLK8K and CLK2K derive from synthesizer F.

Bit 5 ~ 0	Duty Cycle Select
0	Disabled and tri-state
1~62	Pulse width 1 to 62 cycle of 155.52MHz
63	50% duty cycle

Bit 6	Invert
0	Not inverted (frame on rising edge)
1	Inverted (frame on falling edge)

Default value: 63 (50% duty cycle, not inverted)

Field_Upgrade_Status, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Not used					Load_Complete	READY	Checksum

Checksum

Checks whether the 7600 bytes firmware configuration data is loaded successfully.

0 = Fail, 1 = Success

READY

Indicates if field upgrade is ready to begin, normally is set to 1 at 3 milliseconds (3ms) after the reset.

0 = Not ready

1 = Ready

Load_Complete

Indicates whether the loading of 7600 bytes firmware configuration data is complete.

0 = Not complete

1 = Complete

Field_Upgrade_Data, 0x71 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	Field upgrade of firmware configuration data							

Writes the firmware configuration data (7600 bytes) to this register one byte at a time to complete data loading. Only the last written byte can be read from this register, no matter how many times of reads performed.

Default value: 0

Field_Upgrade_Count, 0x72 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	Lower 8 bits of byte count for firmware configuration data							
0x73	Not used			Higher 5 bits of byte count for firmware configuration data				

Reads this register for how many bytes of 7600 bytes firmware configuration data has been loaded through the register **Field_Upgrade_Data**.

Default value: 0

Field_Upgrade_Start, 0x74 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x74	Start field upgrade							

If bit READY of the register **Field Upgrade Status** is set to 1, user can write three values to this register consecutively, with no intervening read/writes from/to other registers to start the process of field upgrade. 7600 bytes firmware configuration data can only start loading after the three values are written successfully.

Order to Write	Bit 7 ~ 0
First	0x51
Second	0x52
Third	0x53

MCLK_Freq_Reset, 0x7F (R/W)

Register Writes:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	External oscillator frequency selection							

Select accepted frequency of MCLK input by writing the associated value to this register three times consecutively, with no intervening read/writes from/to other register. The associated values for the four accepted frequency (10MHz, 12.8MHz, 19.2MHz, 20MHz) are as shown in table below. Three times of consecutive writes will trigger internal soft-reset. Initial default accepted frequency for STC5423 is 12.8MHz. The accepted frequency of MCLK input returns to 12.8MHz following any regular reset.

Perform writes at least 50us after the regular reset has done.

Written value is shown below:

Bit 7 ~ 0	External Oscillator Frequency Selection
0x11	10MHz
0x22	12.8MHz
0x44	19.2MHz
0x88	20MHz

Register Read:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	FRQID		COUNT		ID_Written_Value			

This register allows the user read back three values as follows:

FRQID

Indicates the ID of the frequency of MCLK that the STC5423 currently accept. Constant 1 can be read from FRQID initially since the default accepted frequency for the STC5423 is 12.8MHz. The value of FRQID can only be updated when three consecutive valid writes are written to the register **MCLK_Freq_Rest** completely.

Bit 7 ~ 6 FRQID	MCLK Frequency
0	10MHz
1	12.8MHz
2	19.2MHz
3	20MHz

COUNT

Indicates how many times this register has been written to. COUNT is set to 1 when each time a different valid associated value is written to for the first time and is clear to 0 after three times valid writes are completed.

As described above in Register Writes, the associated value should be written to this register three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, COUNT is clear to 0.

Bit 5 ~ 4 COUNT	Counter
0	No written or invalid
1	Once
2	Twice
3	Three times

ID_Written_Value

Indicates the ID of associated value that is being written to this register. The ID is updated when each time a different valid associated value is written to this register for the first time.

As described above in Register Writes, the associated value should be written to this register three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, ID_Written_Value is clear to 0.

Bit 3 ~ 0 ID_Written_Value	Written value to this register (0x7F)
0	No written or invalid
1	0x11
2	0x22
4	0x44
8	0x88

Default value: 0x40 (12.8MHz)

Noise Transfer Functions

The user may write to the register **Loop Bandwidth** to set the loop bandwidth of the PLL of each timing generator. The noise transfer function of the PLL filter is determined by the loop bandwidth. Figure 17 shows the noise transfer functions as the loop bandwidths vary from 100mHz to 103Hz.

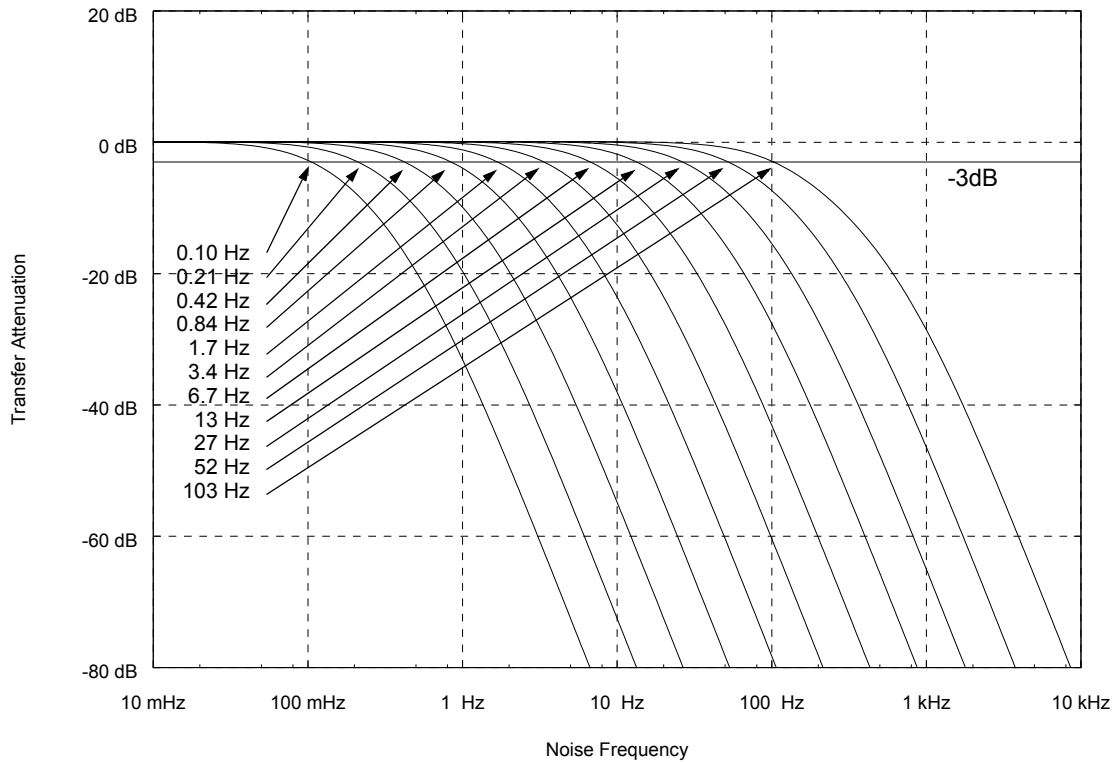


Figure 17: Noise Transfer Functions

Order Information

All STC5423 parts are RoHS 6/6 compliant

<u>Part Number</u>	<u>Description</u>
STC5423-I	Industrial Temperature Range Model (-40°C ~ +85 °C)

Application Notes

This section describes typical application use of the STC5423 device. The General section applies to all application variations.

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3V digital power and analog power input.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints.

Ground should be provided by as continuous a ground plane as possible. A separated analog ground plane is recommended.

Note: un-used reference inputs must be grounded.

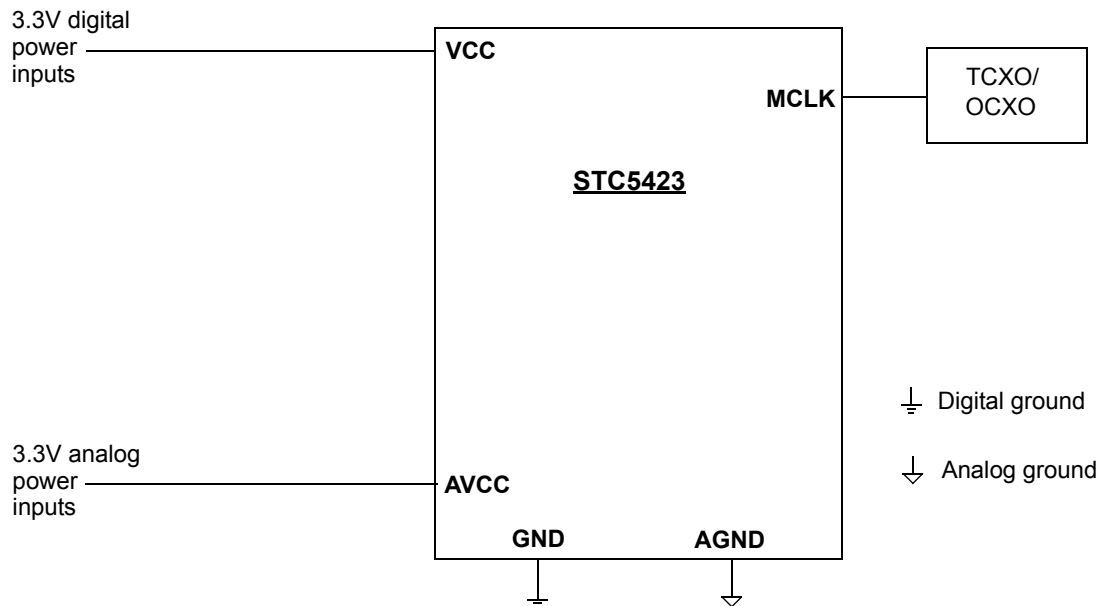
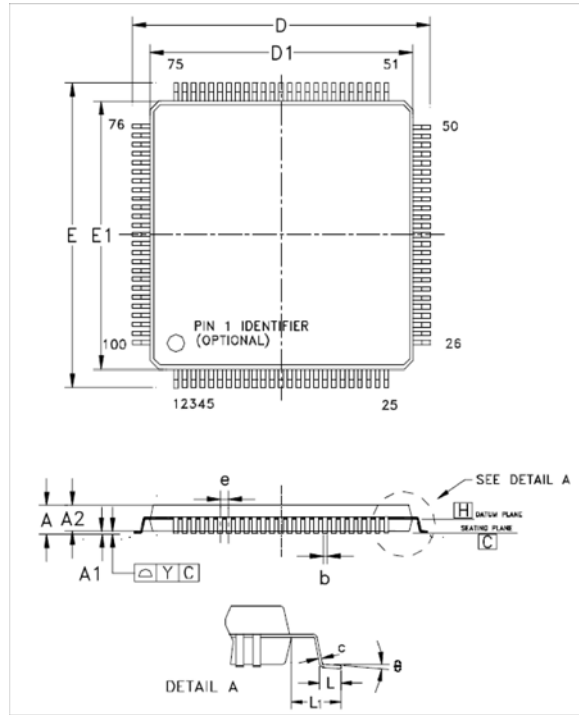


Figure 18: Power and Ground

Master Oscillator

An external 3.3V LVCMOS level clock (generally derived from TCXO or OCXO) is supplied at pin MCLK as master clock. TCXO or OCXO should be carefully chosen as required by application. It is recommended that the oscillator is placed close to the STC5423. Frequency of the master oscillator has four options, see description of the register **MCLK Freq Rest** for details.

Mechanical Specifications



Symbol	Millimeter			Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D	16.00 BSC			0.630 BSC		
E	16.00 BSC			0.630 BSC		
e	0.50 BSC			0.020 BSC		
D1	14.00 BSC			0.551 BSC		
E1	14.00 BSC			0.551 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
Y		0.08			0.003	
θ	0°	3.5°	7°	0°	3.5°	7°

Controlling dimensions are in millimeters

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
0.4	Initial datasheet and minor releases at Preliminary status (For engineer samples).	See particular revision
0.4.1		
0.9		
1.0	First release at final status. (Completely revised for new design).	All pages
1.1	Add Clock Output Jitter section	12
	Add G.8262 EEC Option1 and Option2	1, 14
	Correct description of the register 0x7F in Table 2	10
	Add the section Master Clock Frequency	11
	Remove word "reboot"	17, 23, 49, 51
	Correct description of t_{Dd2} in Motorola Bus Read Timing	29
	Correct description of t_{Dd1} in Intel Bus Read Timing	29
	Correct \overline{CS} and RDB to \overline{WR} in the description of Intel Bus Write Timing	32
	Correct description of t_{ALEd} of Multiplex Bus Write Timing	32
	Add more detail description to section Chip Master Clock	17
	Add more detail description of the register MCLK_Freq_Reset	50, 51, 52

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