

IH5040-IH5047

High-Level CMOS Analog Switch

IH5040-IH5047

GENERAL DESCRIPTION

The IH5040 family of solid state analog switches use an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches.

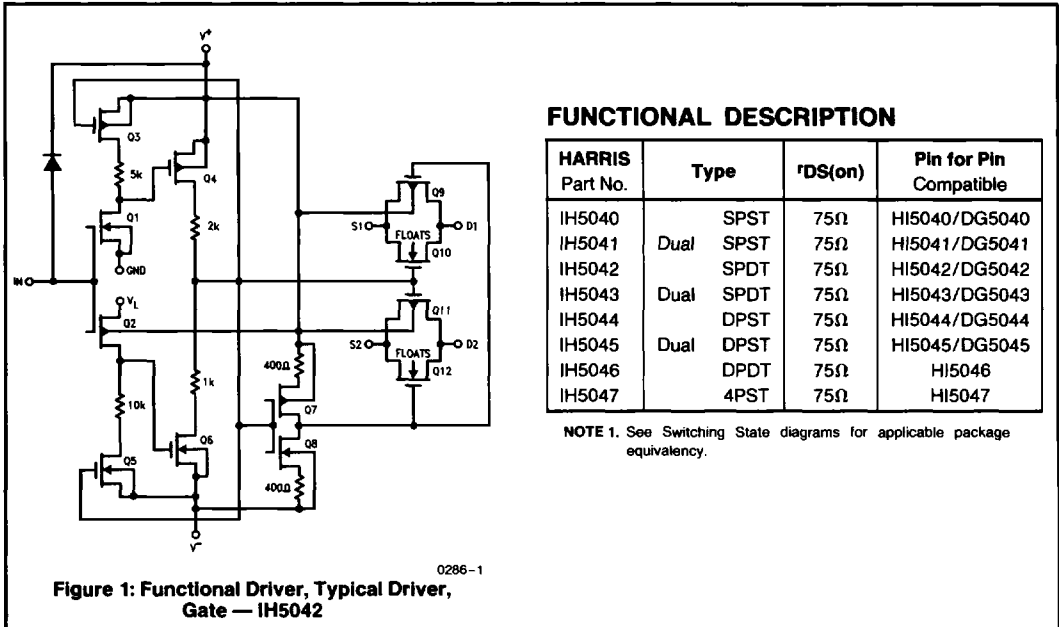
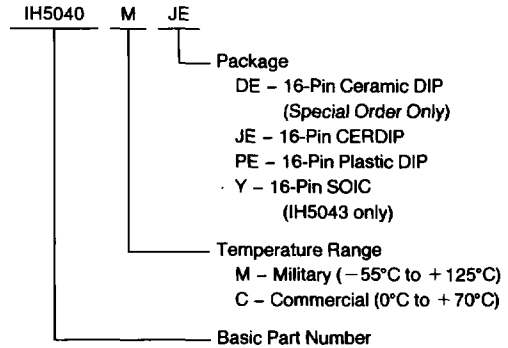
Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than $1\mu\text{A}$. Also, the 5040 guarantees Break-Before-Make switching, accomplished by extending the t_{on} time (300ns TYP.) so that it exceeds t_{off} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FEATURES

- Switches Greater Than 20Vpp Signals With $\pm 15\text{V}$ Supplies
- Quiescent Current Less Than $1\mu\text{A}$
- Break-Before-Make Switching t_{off} 200ns, t_{on} 300ns Typical
- TTL, DTL, CMOS, PMOS Compatible
- New DPDT & 4PST Configurations

ORDERING INFORMATION



FUNCTIONAL DESCRIPTION

HARRIS Part No.	Type	$r_{\text{DS(on)}}$	Pin for Pin Compatible
IH5040	SPST	75Ω	HI5040/DG5040
IH5041	Dual SPST	75Ω	HI5041/DG5041
IH5042	SPDT	75Ω	HI5042/DG5042
IH5043	Dual SPDT	75Ω	HI5043/DG5043
IH5044	DPST	75Ω	HI5044/DG5044
IH5045	Dual DPST	75Ω	HI5045/DG5045
IH5046	DPDT	75Ω	HI5046
IH5047	4PST	75Ω	HI5047

NOTE 1. See Switching State diagrams for applicable package equivalency.

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ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	<36V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	< $\pm 22V$
$V_L - V^-$	<33V
$V_L - V_{IN}$	<30V
$V_L - GND$	<20V
$V_{IN} - GND$	<20V

Current (Any Terminal)	<30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
M	-55°C to +125°C
C	0°C to +70°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6mW/°C Above 70°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Commercial			
			-55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 2.4V$	± 1	± 1	10	± 1	± 1	10	μA
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 0.8V$	± 1	± 1	10	± 1	± 1	10	μA
$r_{DS(on)}$	Drain-Source On Resistance	$I_S = 10mA$ $V_{ANALOG} = -10V$ to +10V	75	75	150	80	80	130	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			± 11 (typ)			± 10 (typ)		V
$I_{D(OFF)}/I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -10V$ to +10V		± 1	100		± 5	100	nA
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to +10V		± 2	200		± 10	100	nA
t_{on}	Switch "ON" Time	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to +10V See Fig. 3		1000			1000		ns
t_{off}	Switch "OFF" Time	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to +10V See Fig. 3		500			500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. 5		54 (typ)			50 (typ)		dB
$I^+ Q$	V^+ Power Supply Quiescent Current		± 1	± 1	10	10	10	100	μA
$I^- Q$	V^- Power Supply Quiescent Current	$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$	± 1	± 1	10	10	10	100	μA
$I^- LQ$	+5V Supply Quiescent Current		± 1	± 1	10	10	10	100	μA
I_{GND}	Gnd Supply Quiescent Current		± 1	1	10	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Fig. 6		54 (typ)			50 (typ)		dB

Note: Typical values are for design aid only, not guaranteed and not subject to production testing.

NOTE: All typical values have been characterized but are not tested.

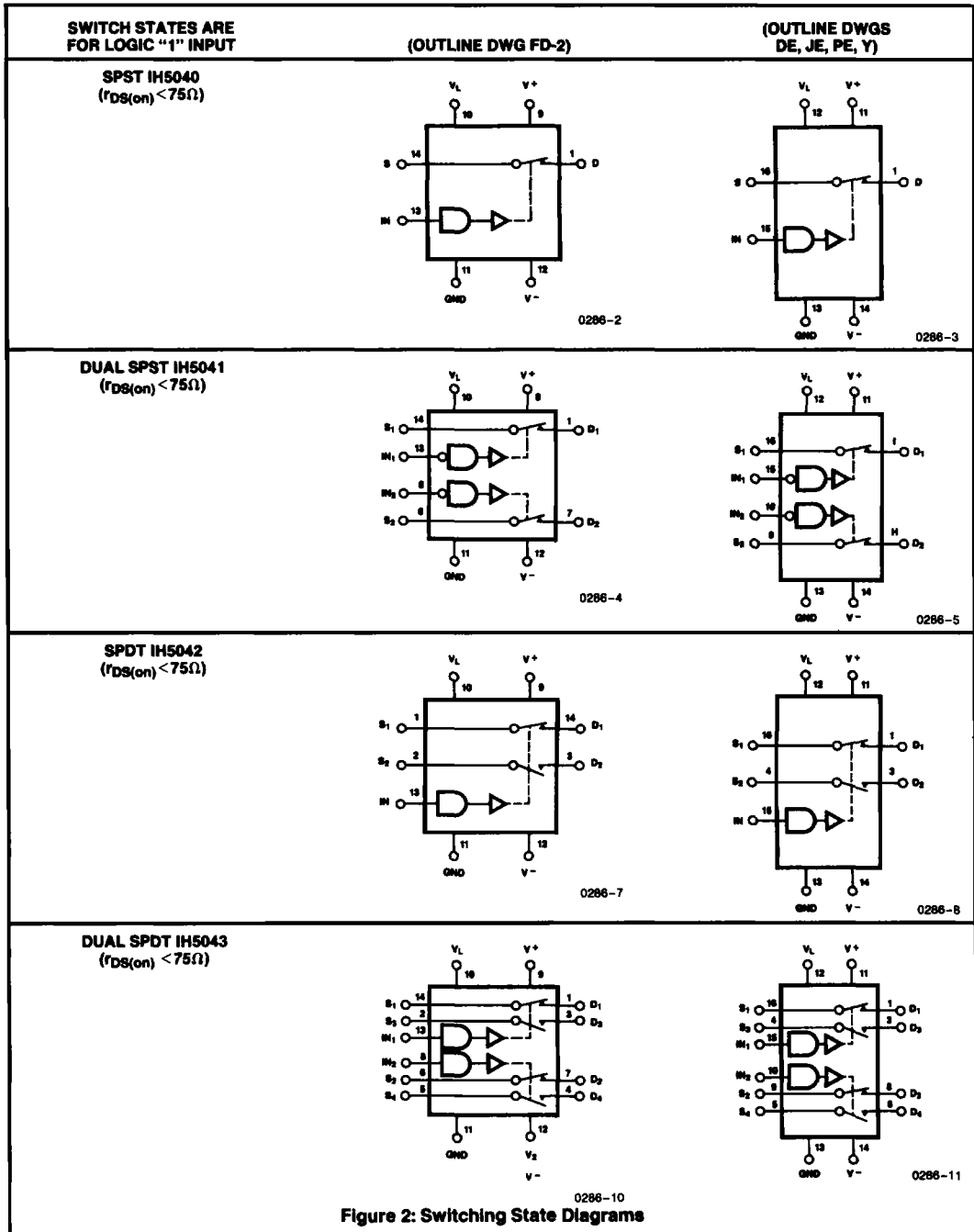


Figure 2: Switching State Diagrams

NOTE: All typical values have been characterized but are not tested.

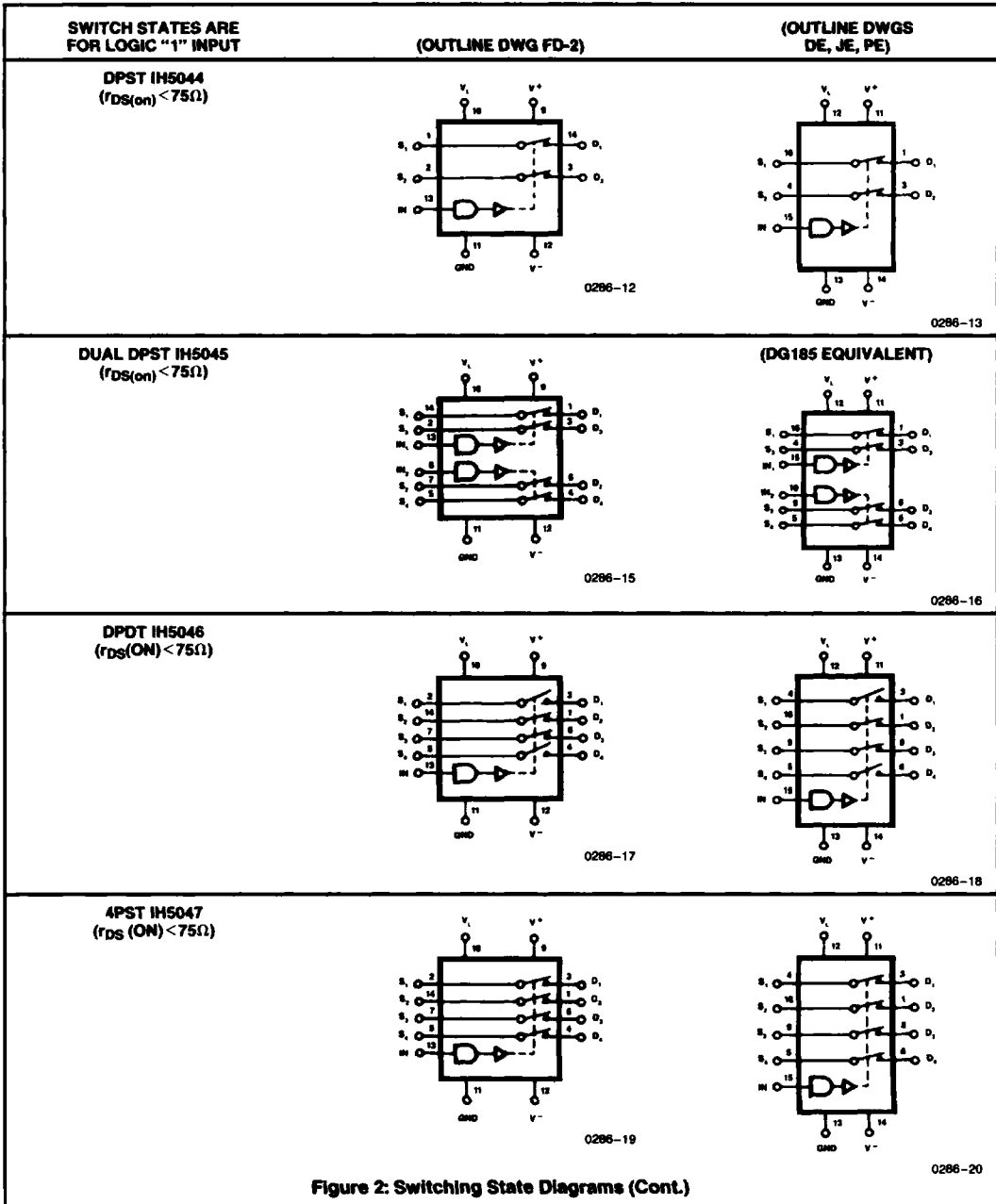
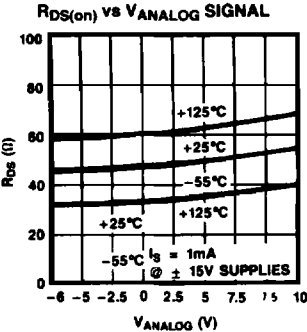


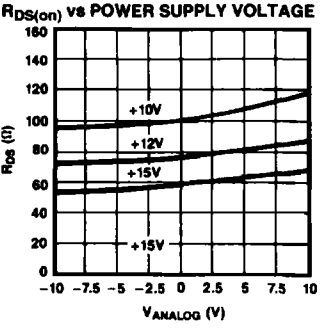
Figure 2: Switching State Diagrams (Cont.)

NOTE: All typical values have been characterized but are not tested.

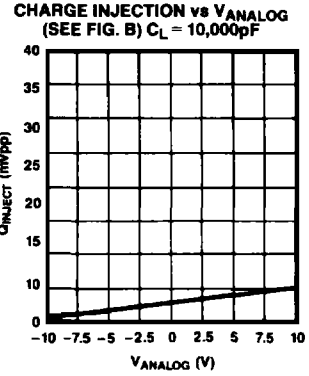
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)



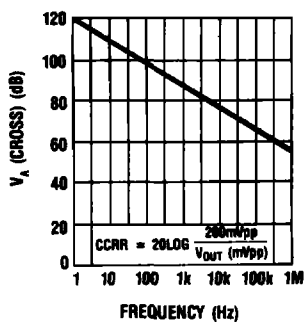
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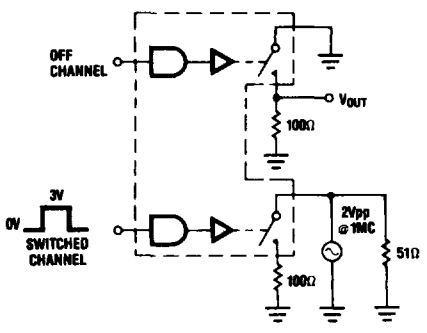
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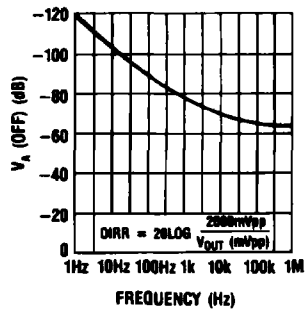
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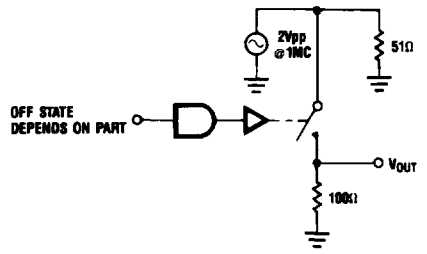
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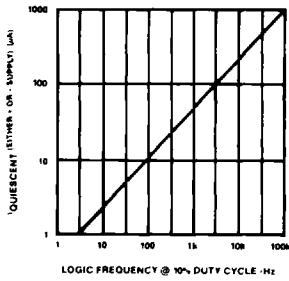


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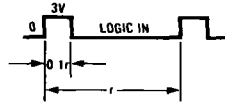
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TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



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TEST CIRCUITS

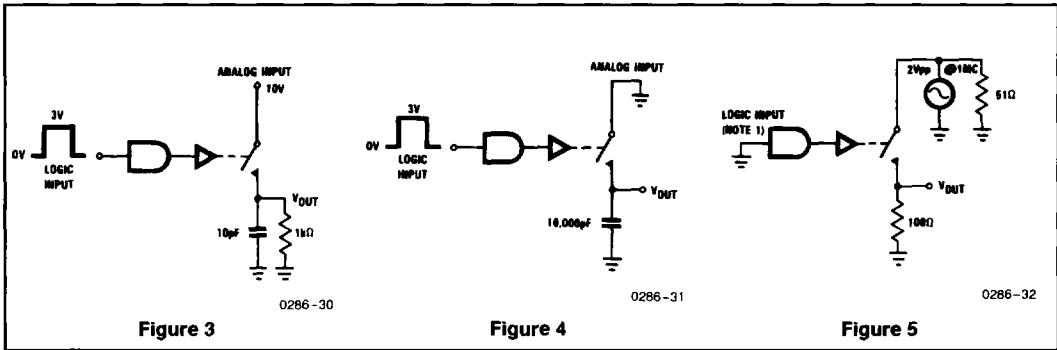


Figure 3

Figure 4

Figure 5

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

APPLICATIONS

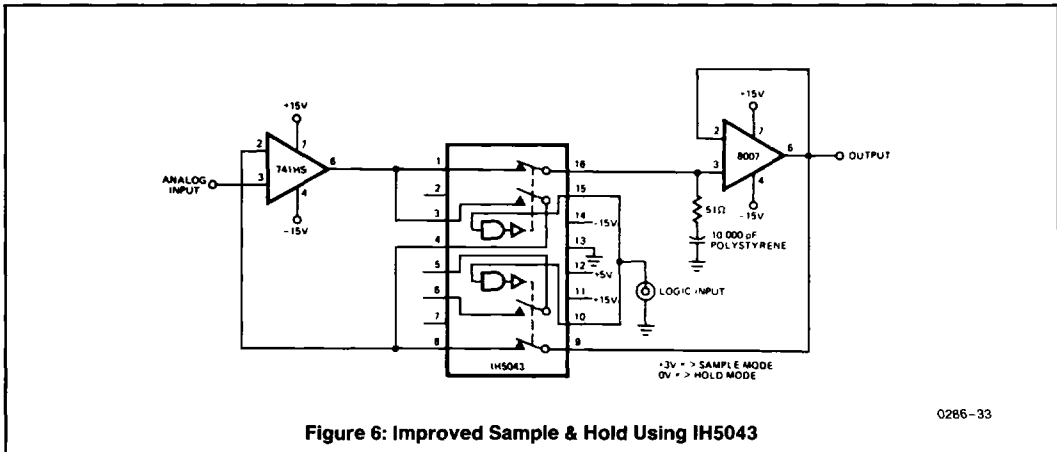


Figure 6: Improved Sample & Hold Using IH5043

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

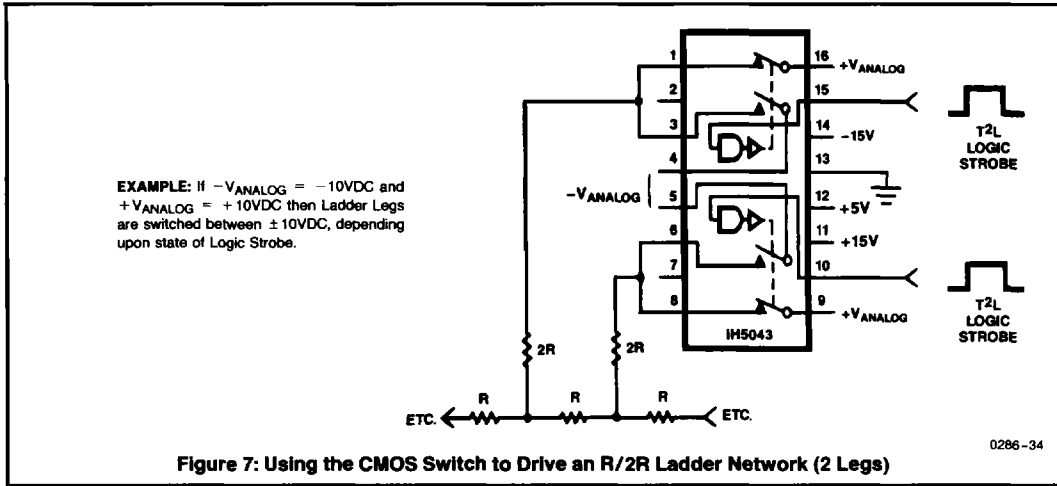


Figure 7: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

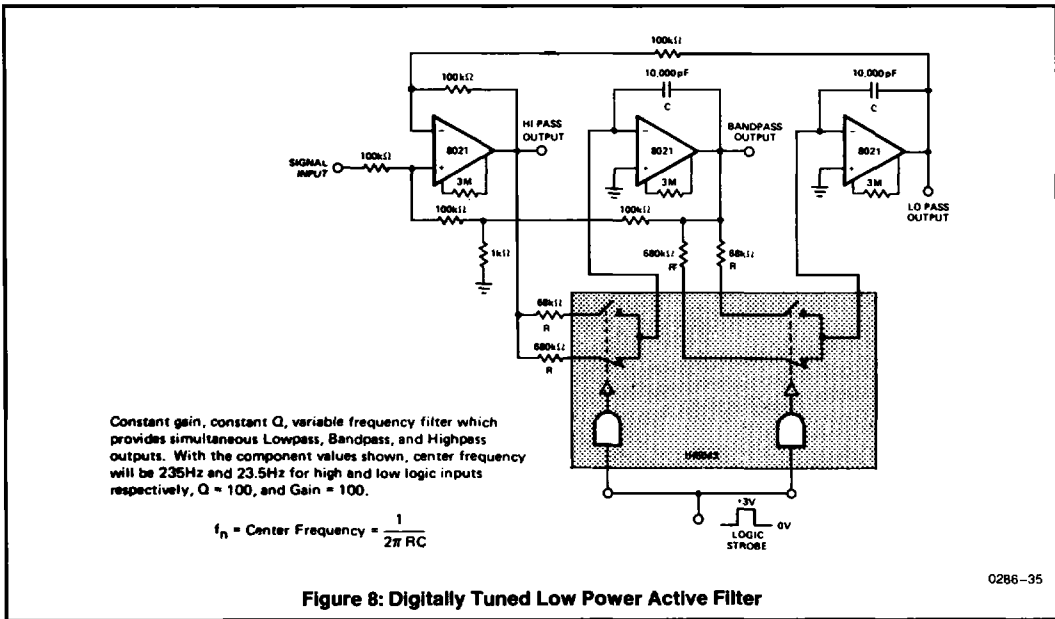
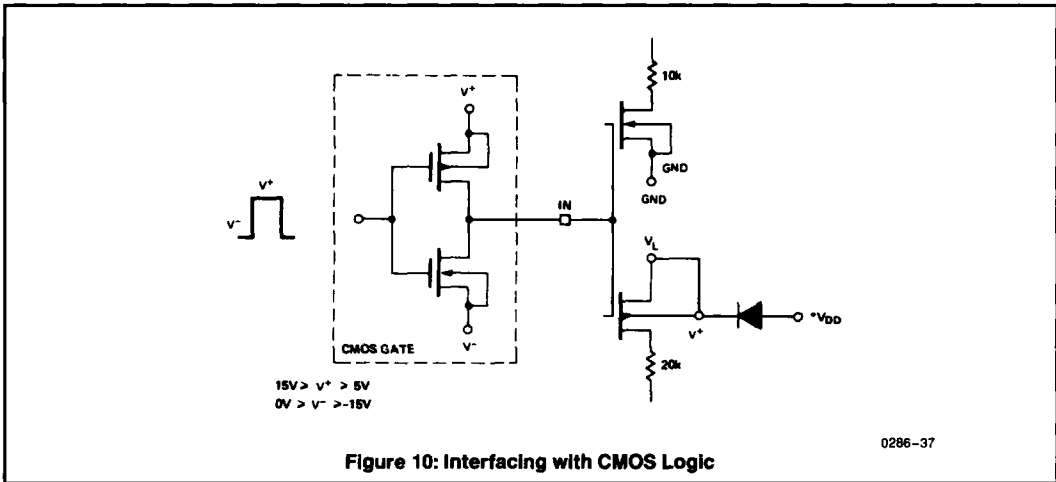
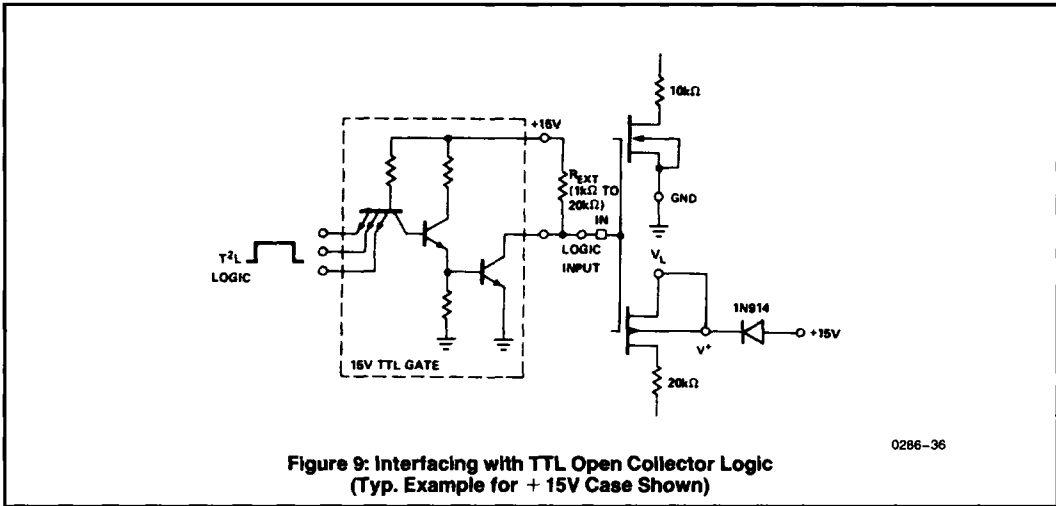


Figure 8: Digitally Tuned Low Power Active Filter

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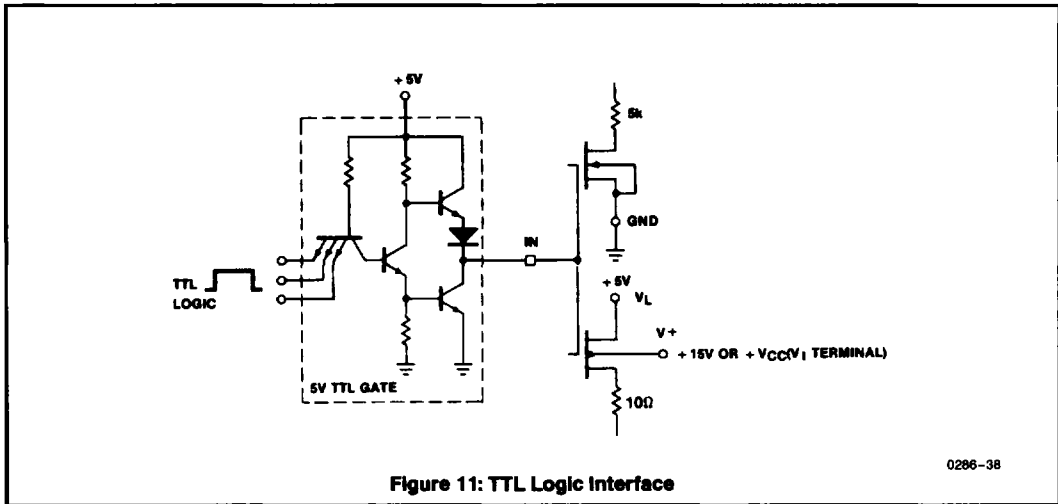
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APPLICATIONS (Continued)



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