NEC
NEC Electronics Inc.

μPD7759
ADPCM Speech Processor

Description

The μPD7759 is a speech processing LSI that, with an external ROM, utilizes adaptive differential pulse-code modulation (ADPCM) to produce high-quality, natural-sounding speech. By combining melody mode with the ADPCM method and pause compression, the device achieves a compressed bit rate that can reproduce sound effects and melodies in addition to speech sound.

The μPD7759 can directly address up to 1M bits of external data ROM, or the host CPU can control the speech data transfer. The μPD7759 is also suitable for applications requiring small production quantities or long messages, and for emulating the μPD7755/56/P56/57/P57/58.

Features

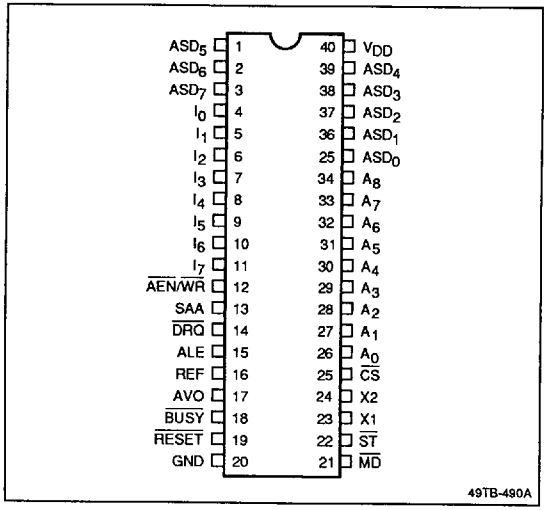
- High-quality speech reproduction using ADPCM
- Low bit-rates (10 to 32 kb/s) realized by combined use of ADPCM and pause compression
- Bit rates to less than 1 kb/s for sound effects, melodies, and tones (DTMF) using melody mode
- Sampling frequency: 5, 6, or 8 kHz
- D/A converter with 9-bit resolution; unipolar current waveform output
- Up to 1M bits addressing for external data ROM
- Reproduction time: 50 seconds typical (for 6 kHz sampling)
- Standby function
- Circuit to eliminate popcorn noise when entering or releasing standby mode
- Control signal interface; general purpose 4- or 8-bit CPU
- Wide operating voltage range: 2.7 to 5.5 V
- CMOS technology
- 40-pin plastic DIP; 52-pin plastic QFP package

Ordering Information

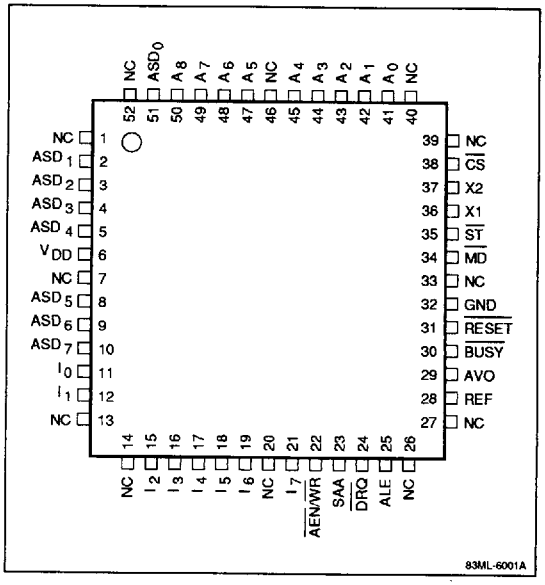
Part Number	Package
μPD7759C	40-pin plastic DIP
μPD7759GC	52-pin plastic QFP

Pin Configurations

40-Pin Plastic DIP



52-Pin Plastic QFP



Pin Identification

Symbol	Name
A_0 - A_8	Lower 9 bits of address output for speech data
$\overline{AEN}/\overline{WR}$	Address valid output/Write strobe input for speech data
ALE	High address latch enable output
ASD_0 - ASD_7	Higher 8 bits of address output/Speech data input (multiplexed)
AVO	Analog voice output
$\overline{BUSY}$	Busy output
$\overline{CS}$	Chip select input
$\overline{DRQ}$	Data request output
I_0 - I_7	Message select code input
$\overline{MD}$	Mode select input (stand alone/$\overline{slave}$)
REF	D/A converter reference current input
$\overline{RESET}$	Reset input
SAA	Directory data output address valid
$\overline{ST}$	Start input
X1, X2	Ceramic resonator clock terminals
V_{DD}	+5-volt power supply
GND	Ground
NC	No connection

PIN FUNCTIONS

A_0 - A_8 (Address Bus)

These are output lines for the lower 9 bits of the address bus. They are ineffective in the slave mode.

$\overline{AEN}/\overline{WR}$ (Address Enable Output/Write Signal Input)

$\overline{AEN}$ is high when the address signal is valid in standalone mode. $\overline{WR}$ is the write input signal for speech data in slave mode.

ALE (Address Latch Enable)

This signal defines the higher address bit timing latched externally. It is ineffective in the slave mode.

ASD_0 - ASD_7 (Address/Speech Data)

ASD_0 - ASD_7 are the output lines for the higher 8 bits of the address signal and the input lines for speech data in standalone mode. In slave mode, these are input lines for speech data.

AVO (Analog Voice Output)

AVO outputs speech from the D/A converter. This is a unipolar sink-load current. No current flows in standby mode.

$\overline{BUSY}$ (Busy)

$\overline{BUSY}$ outputs the status of the μPD7759. It goes low during speech decode and output operations. When $\overline{ST}$ is received, $\overline{BUSY}$ goes low. While $\overline{BUSY}$ is low, another $\overline{ST}$ will not be accepted. In standby mode, $\overline{BUSY}$ becomes high impedance. This is an active low output.

$\overline{CS}$ (Chip Select)

When the $\overline{CS}$ input goes low, $\overline{ST}$ is enabled. In standalone mode and $\overline{WR}$ is enabled in slave mode.

$\overline{DRQ}$ (Data Request)

This is the data request output signal for slave mode.

I_0 - I_7 (Message Select Code)

I_0 - I_7 input the message number of the message to be reproduced. The inputs are latched at the rising edge of the $\overline{ST}$ input. Unused pins should be grounded. In standby mode, these pins should be set high or low. If they are biased at or near typical CMOS switch input, they will drain excess current.

$\overline{MD}$ (Mode Select Input)

$\overline{MD}$ is low to specify slave mode operation. Transition between two operation modes is not accepted during speech output or in the standalone mode.

REF (D/A Converter Reference Current)

REF inputs the sink-load current that controls the D/A converter output. REF should be connected to V_{DD} via a resistor. In standby mode, REF becomes high impedance.

$\overline{RESET}$ (Reset)

The $\overline{RESET}$ input initialized the chip. Use $\overline{RESET}$ following power-up to abort speech reproduction or to release standby mode. $\overline{RESET}$ must remain low at least 12 oscillator clocks. At power-up or when recovering from standby mode, $\overline{RESET}$ must remain low at least 12 more clocks after clock oscillation stabilizes.

SAA (Start Address)

SAA indicates that the start address of a message stored in the directory of the data memory is being read out. It is ineffective in the slave mode.

$\overline{ST}$ (Start)

Setting the $\overline{ST}$ input low while $\overline{CS}$ is low will start speech reproduction of the message in the speech ROM locations addressed by the contents of I_0 - I_7. If the device is in standby mode, standby mode will be released.

X1, X2 (Clock)

Pins X1 and X2 should be connected to a 640-kHz ceramic resonator. In standby mode, X1 goes low and X2 goes high.

V_{DD} (Power)

+ 5-V power supply.

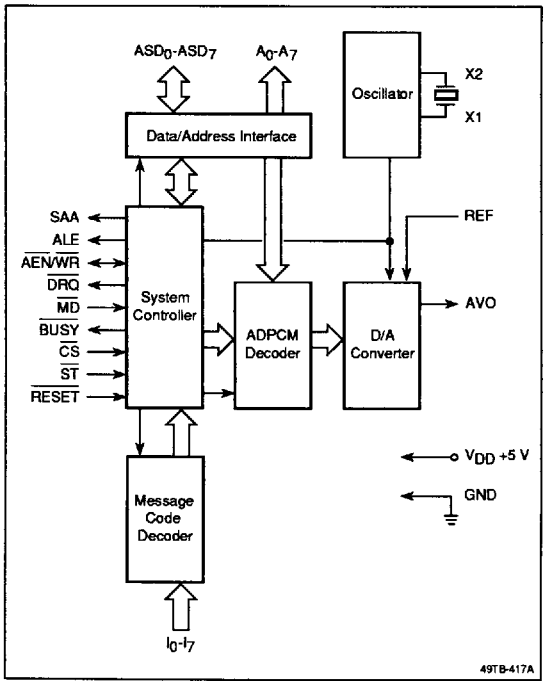
GND (Ground)

Ground.

NC (No Connection)

These pins are not connected.

Block Diagram



OPERATION

The clock pins should be connected to a ceramic resonator at 640 kHz

The $\overline{RESET}$ input pin is used to initialize the device. To reset, assert the pin for a minimum of 12 oscillator clock cycles.

The μPD7759 can operate with a wide range of supply voltages: 2.7 to 5.5 V. It also has a standby function; it goes to a standby mode when it has been idle (that is, when $\overline{CS}$, $\overline{ST}$, or $\overline{RESET}$ have not been asserted) for more than 3 seconds. The device will automatically release from standby mode when $\overline{CS}$ and $\overline{ST}$ are asserted again, or when $\overline{RESET}$ is asserted.

The μPD7759 has a very simple message selection interface with 1 Mbit of external ROM and can store a maximum of 256 different messages and up to 50 seconds of speech. The message is selected by using input pins I_0 - I_7. The selection is latched at the rising edge of $\overline{ST}$ when $\overline{CS}$ is asserted. When $\overline{ST}$ is asserted, $\overline{BUSY}$ will go low until the selected audio speech output is completed. While $\overline{BUSY}$ is low, a new $\overline{ST}$ will not be accepted.

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The μPD7759 has an internal D/A converter—a unipolar, current-output type with 9-bit resolution. The converter output current can be controlled by the voltage applied at the REF pin.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−40 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Capacitance

T_A = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			10	pF	fc = 1 MHz
Output capacitance	C_O			20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = 2.7 to 5.5 V; f_{OSC} = 640 kHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Common to I_0-I_7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$, $\overline{MD}$, $\overline{WR}$
	V_{IH2}	2.2		V_{DD}	V	Common to ASD_0 - ASD_7; V_{DD} = 5 V ±10%
Input voltage, low	V_{IL}	0		0.3 V_{DD}	V	Common to I_0-I_7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$, $\overline{MD}$, $\overline{WR}$
	V_{IL2}	0		0.8	V	Common to ASD_0 - ASD_7; V_{DD} = 5 V ±10%
Output voltage, high	V_{OH}	V_{DD} − 0.5		V_{DD}	V	I_{OH} = −100 μA
Output voltage, low	V_{OL}	0		0.4	V	I_{OL} = −1.6 mA; V_{DD} = 5 V ±10%
Input leakage current	I_{LI}			3	μA	Common to I_0-I_7, $\overline{ST}$, $\overline{WR}$, $\overline{CS}$, $\overline{MD}$, ASD_0 - ASD_7
Output leakage current	I_{LO}			3	μA	$\overline{BUSY}$, A_0 - A_8
Supply current	I_{DD1}			10	mA	V_{DD} = 5 V
	I_{DD2}			20	μA	V_{DD} = 5 V in standby mode
	I_{DD3}			1	μA	V_{DD} = 2.7 to 3.5 V
	I_{DD4}			10	μA	V_{DD} = 2.7 to 3.5 V in standby mode
Reference input high current area (figure 1)	I_{REF1}	140	250	440	μA	V_{DD} = 2.7 V, R_{REF} = 0 Ω
	I_{REF2}	500	760	1200	μA	V_{DD} = 5.5 V, R_{REF} = 0 Ω
Reference input low current area (figure 1)	I_{REF3}	21	30	39	μA	V_{DD} = 2.7 V, R_{REF} = 50 kΩ
	I_{REF4}	68	78	88	μA	V_{DD} = 5.5 V, R_{REF} = 50 kΩ
D/A converter output current (figure 1)	I_{AVO}	32	34	36	I_{REF}	V_{DD} = 2.7 to 5.5 V, V_{AVO} = 2.0 V; D/A input = 1FFH
D/A converter output leakage current	I_{LA}			±5	μA	Standby mode; V_{AVO} = 0 to V_{DD}

Figure 1. Measuring Diagram for IREF and IAVO

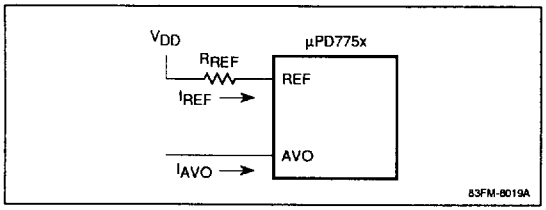
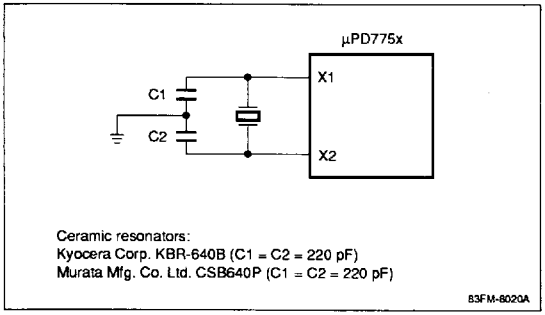


Figure 2. External Oscillator



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AC Characteristics

T_A = −10 to +70°C; V_{DD} = 2.7 to 5.5 V; f_{OSC} = 640 kHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Timing for All Modes						
$\overline{CS}$ setup time	t_{CS}	0			ns	When $\overline{ST}$ ↓
$\overline{CS}$ hold time	t_{SC}	0			ns	After $\overline{ST}$ ↑
$\overline{ST}$ pulse width	t_{CC1}	350			ns	V_{DD} = 5 V ±10%
	t_{CC2}	5			μs	V_{DD} = 2.7 to 5.5 V
Message code setup time	t_{DW1}	350			ns	V_{DD} = 5 V ±10%
	t_{DW2}	5			μs	V_{DD} = 2.7 to 5.5 V
Message code hold time	t_{WD}	0			μs	After $\overline{ST}$ ↑
Switching Characteristics for All Modes						
$\overline{BUSY}$ rise time	t_{R1}			800	ns	C_L = 150 pF; V_{DD} = 5 V ±10%
	t_{R2}			2	μs	C_L = 150 pF; V_{DD} = 2.7 to 5.5 V ±10%
$\overline{BUSY}$ fall time	t_{F1}			800	ns	C_L = 150 pF; V_{DD} = 5 V ±10%
	t_{F2}			2	μs	C_L = 150 pF; V_{DD} = 2.7 to 5.5 V ±10%
Timing for Standalone Mode						
$\overline{RESET}$ pulse width	t_{RST}	18.5			μs	
$\overline{CS}$ setup time	t_{CS}	0			ns	When $\overline{ST}$ ↓
$\overline{CS}$ hold time	t_{SC}	0			ns	After $\overline{ST}$ ↑
$\overline{ST}$ pulse width	t_{CC1}	2			μs	V_{DD} = 2.7 to 5.5 V
	t_{CC2}	350			ns	V_{DD} = 4.5 to 5.5 V
Message code setup time	t_{DW1}	2			μs	V_{DD} = 2.7 to 5.5 V
	t_{DW2}	350			ns	V_{DD} = 4.5 to 5.5 V
Message code hold time	t_{WD}	0			ns	After $\overline{ST}$ ↑
Speech data setup time	t_{RD}	8			μs	When $\overline{DRQ}$ ↓
Speech data hold time	t_{RDH}	1.25			μs	After $\overline{DRQ}$ ↑
$\overline{ST}$ setup time	t_{RS}	12.5			μs	After $\overline{RESET}$ ↑
$\overline{BUSY}$ hold time	t_{RB}			9.5	μs	After $\overline{RESET}$ ↓
Switching Characteristics for Standalone Mode						
$\overline{BUSY}$ output delay	t_{SBO}		6.25	10	μs	Operation mode after $\overline{ST}$ ↓
Speech output delay	t_{SSO}		2.1	2.2	ms	Operation mode after $\overline{BUSY}$ ↓
$\overline{BUSY}$ hold time	t_{BD}			15	μs	After speech reproduction
ALE pulse width	t_{LL}		3.13		μs	
Higher address setup time	t_{AL}		3.13		μs	When ALE ↓
	t_{AE}		0		μs	When $\overline{AEN}$ ↑
	t_{LA}		3.13		μs	After ALE ↓
	t_{EA}		0		μs	After $\overline{AEN}$ ↑
$\overline{AEN}$ pulse width	t_{AEN}		14.1		μs	
$\overline{DRQ}$ output time	t_{LC}		3.13		μs	After ALE ↓
Pulse width timing	t_{AC}		6.25		μs	
$\overline{DRQ}$ pulse duration	t_{DCC}		7.81		μs	
ROM read cycle time	t_{MRO}		37.5		μs	

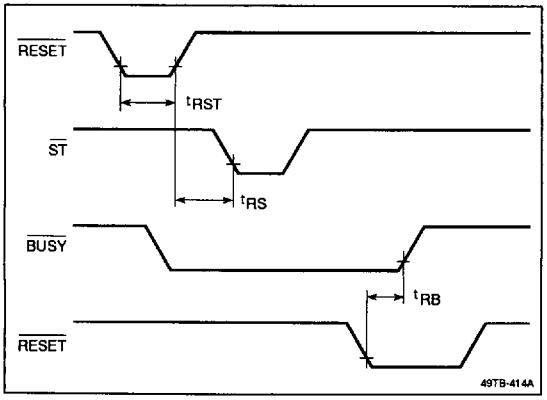
AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Timing for Slave Mode						
$\overline{MD}$ input timing	t_{RM}	6.2			μs	After $\overline{RESET}$ ↑
	t_{BM}	0			ns	After $\overline{BUSY}$ ↑
	t_{MD}	6.2			μs	After $\overline{MD}$ ↑
Speech data setup time	t_{DW}	350			ns	When $\overline{WR}$ ↑; V_{DD} = 5 V ±10%
Speech data hold time	t_{DW}	0			ns	When $\overline{WR}$ ↑; V_{DD} = 5 V ±10%
Data write time	t_{WR}			31.7	μs	After $\overline{DRQ}$ ↓
$\overline{WR}$ pulse width	t_{CC}	350			ns	V_{DD} = 5 V ±10%
$\overline{CS}$ setup time	t_{CW}	0			ns	When $\overline{WR}$ ↓
$\overline{CS}$ hold time	t_{WC}	0			ns	After $\overline{WR}$ ↑
$\overline{MD}$ pulse width	t_{MD2}	6.2			ns	
Switching Characteristic for Slave Mode						
$\overline{BUSY}$ output delay	t_{SBO}			9.5	μs	After $\overline{MD}$ ↓
$\overline{DRQ}$ output delay	t_{MDR}	50		70	μs	After $\overline{MD}$ ↓
Data request timing	t_{WRQ}			3	μs	After $\overline{WR}$ ↓
Timing for Standby Mode						
Pulse width standby escape signal (Note)	t_{AW}	350			ns	V_{DD} = 5 V ±10%
Switching Characteristics for Standby Mode						
Operation mode hold time	t_{STB}		2.9	3	s	After speech reproduction
Activate/Inactivate D/A converter time	t_{DA}		46.5	47	ms	
$\overline{BUSY}$ ↓	t_{SB}		6.25	10	μs	After L ↓ (Note)
Speech reproduction start time	t_{SSS}		2.1	2.2	ms	After t_{DA}
$\overline{BUSY}$ output delay	t_{SBS}		4	80	ms	After L ↓ (Note)

Note: L = Signal to escape standby mode or $\overline{ST}$ ↓ following $\overline{CS}$ ↓ when operation is standalone mode or $\overline{WR}$ ↓ following $\overline{CS}$ ↓ when operation is slave mode

Timing Waveforms

Reset



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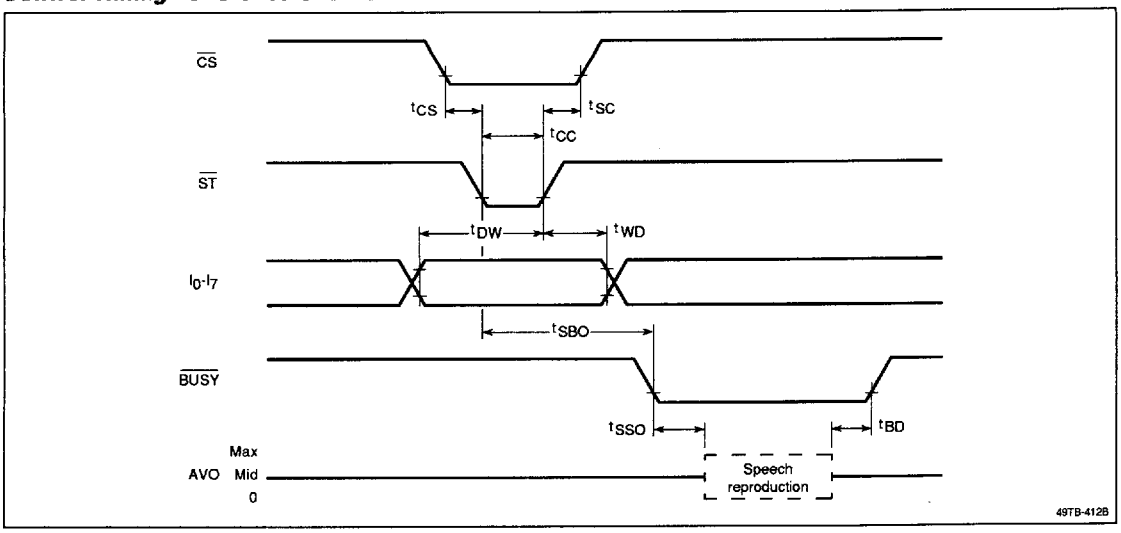
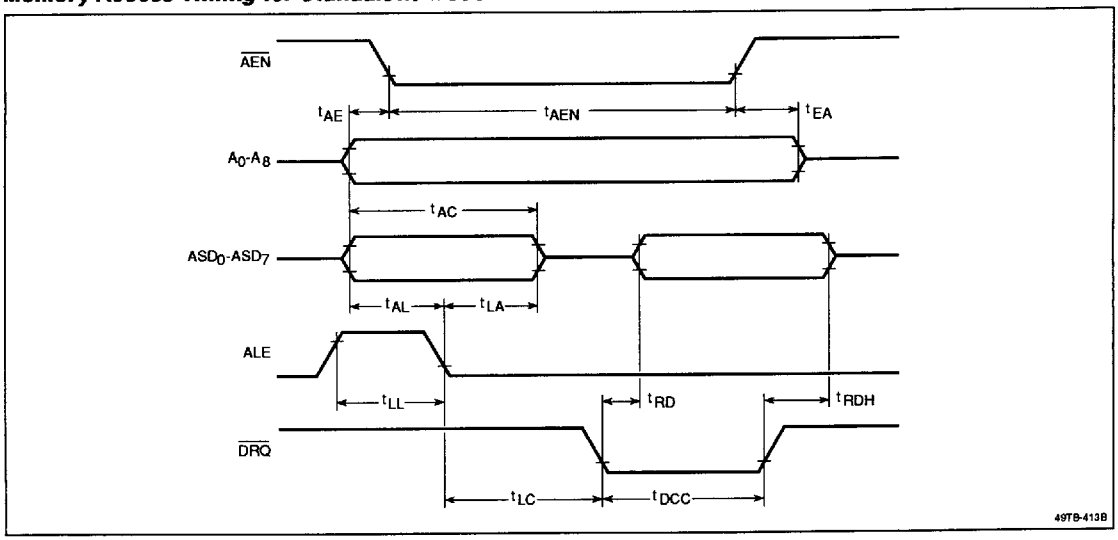
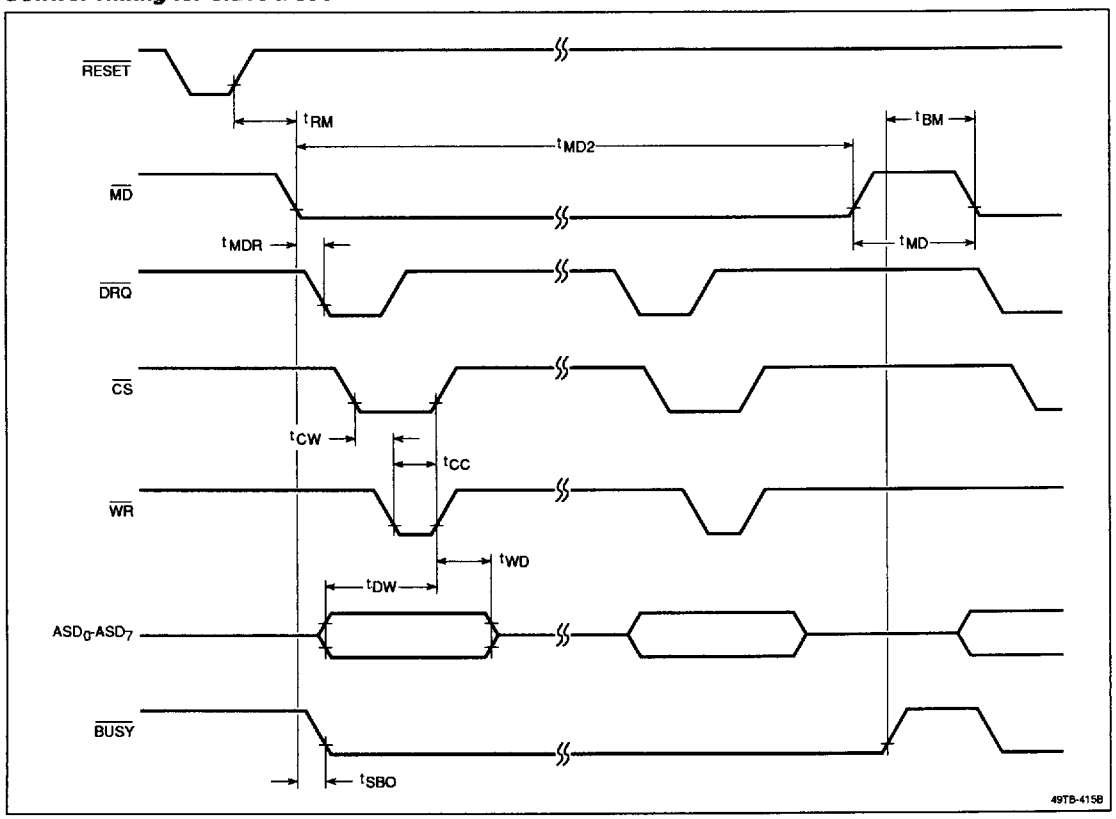
Control Timing For Standalone Mode



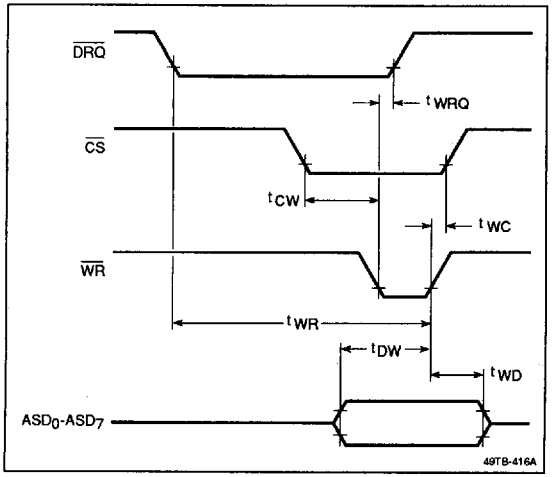
Memory Access Timing for Standalone Mode



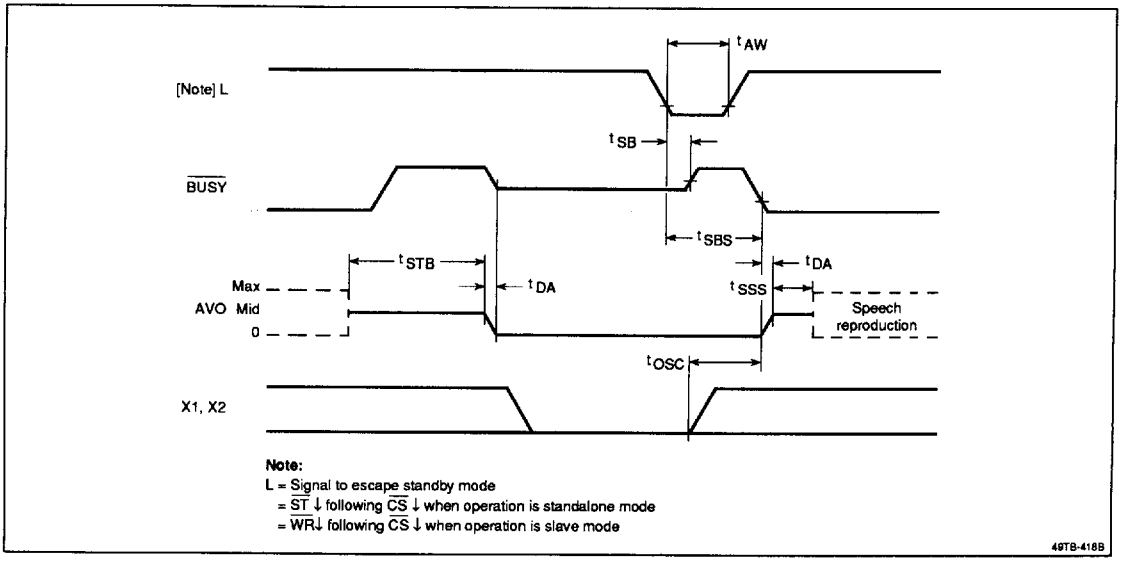
Control Timing for Slave Mode



Data Transfer for Slave Mode



Timing for Standby Mode



Note:
L = Signal to escape standby mode
= $\overline{ST}$ ↓ following $\overline{CS}$ ↓ when operation is standalone mode
= $\overline{WR}$↓ following $\overline{CS}$ ↓ when operation is slave mode