SN10KHT5563, SN100KT5563 OCTAL TTL/ECL BUS TRANSCEIVERS T-52-11 WITH 3-STATE OUTPUTS

- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{GC1} V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

The SN10KHT5563 and SN100KT5563 are inverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50- Ω load terminated to -2 V.

The A and B ports have complementary outputenable inputs, both of which are ECL-compatible. When the A-port output enable (GBA) is high, the device transmits data from the B bus to the A bus; when GBA is low, the A outputs are in the high-impedance state. When $\overline{G}AB$ is low, the device transmits data from the A bus to the B bus; when $\overline{G}AB$ is high, the B outputs are in the high-impedance state.

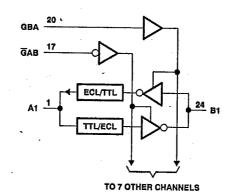
When GAB is low and $\overline{G}BA$ is high, the device is in the isolation mode.

The SN10KHT5563 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5563 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW (DW OR NT PACKAGE (TOP VIEW)			
A1[A2[A3[VCC] GND[GND[A5[A6[A7[A8]	1 2 3 4 5 6 7 8 9	24 23 22 21 20 19 18 17	B1 B2 B3 B4 GBA VEE GND GAB B5 B6 B7 B8	

logic diagram (positive logic)



PRODUCT PREVIEW

