20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Current drive ± 24 mA at 3.0 V
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

When $n\overline{OE}$ is LOW, the data in the register appears at the outputs. When $n\overline{OE}$ is HIGH, the outputs are in high impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16821 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ_n	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.6 2.5	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	33	pF
			Outputs disabled	17	
F_{max}	Maximum clock frequency	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		250 350	MHz

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in W):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16821 DL	ACH16821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16821 DGG	ACH16821 DGG	SOT364-1

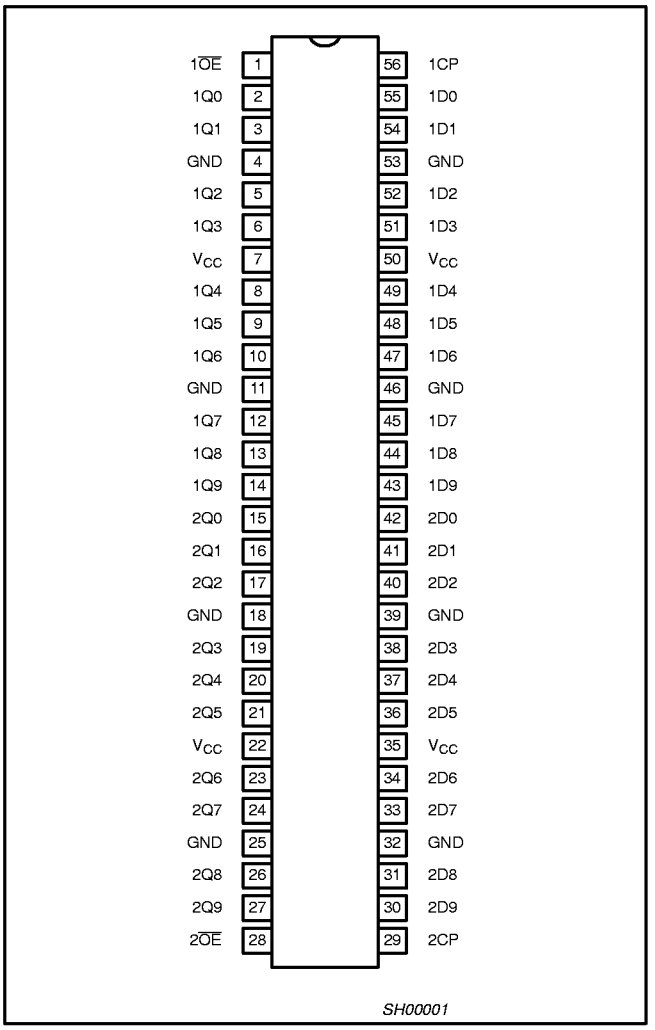
20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 - 1D9	Data inputs
42, 41, 40, 38, 37, 36, 34, 33, 31, 30	2D0 - 2D9	
2, 3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 - 1Q9	Data outputs
15, 16, 17, 19, 20, 21, 23, 24, 26, 27	2Q0 - 2Q9	
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION

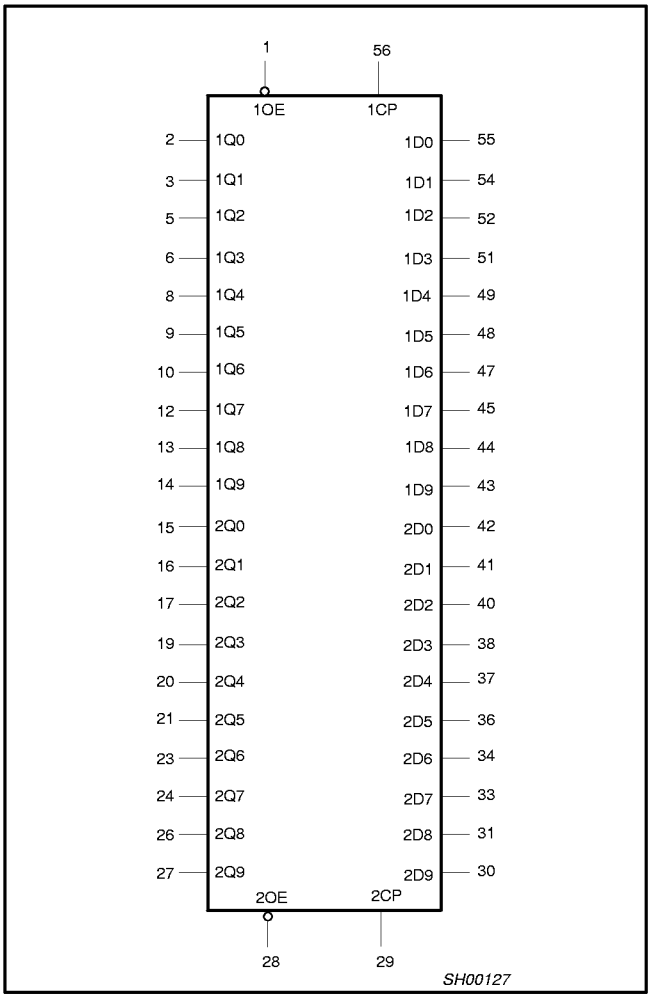


FUNCTION TABLE

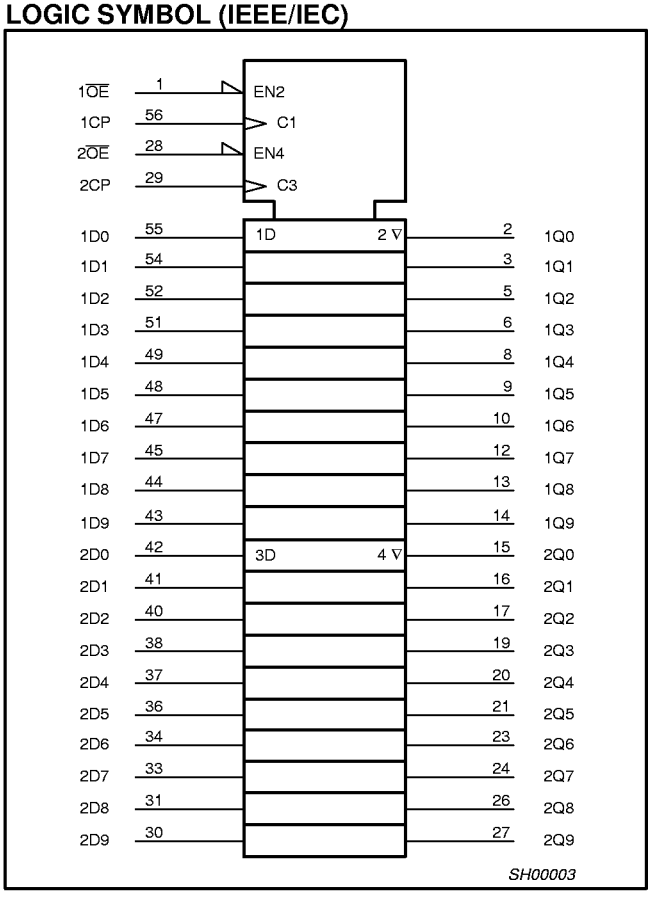
INPUTS			OUTPUT
$n\overline{OE}$	CP	Dx	Q
L	↑	L	L
L	↑	H	H
L		X	Q0
H	~~X~~	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF state
↑ = LOW to HIGH clock transition
= Not a LOW-to-HIGH clock transition

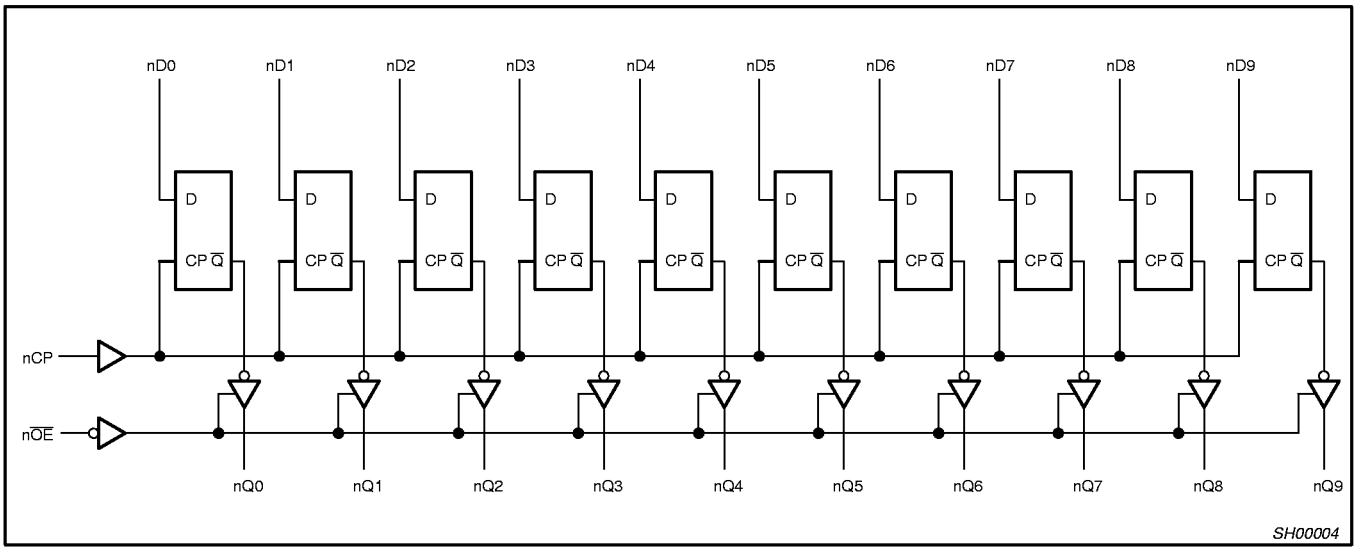
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I 0	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O V_{CC} or V_O 0	50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC}* 0.2	V_{CC}		V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC}* 0.3	V_{CC}* 0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC}* 0.6	V_{CC}* 0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC}* 0.5	V_{CC}* 0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC}* 0.6	V_{CC}* 0.09		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC}* 1.0	V_{CC}* 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PLH}/t_{PHL}	Propagation delay nCP to nQ_n	1, 4	1.0	2.6	5.8	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.8	6.6	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.2	5.7	ns
t_W	nCP pulse width HIGH or LOW	3, 4	3.0	1.8		ns
t_{SU}	Set up time nD_n to nCP	3, 4	1.4	0.3		ns
t_h	Hold time nD_n to nCP	3, 4	0.4	0.0		ns
F_{max}	Maximum clock pulse frequency	1, 4	150	250		MHz

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3 \pm 0.3$V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ_n	1, 4	1.0	2.5	4.5	1.0	2.8	5.3	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.3	5.1	1.0	3.2	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.8	4.6	1.0	3.1	5.0	ns
t_W	nCP pulse width HIGH or LOW	3, 4	3.3	0.2		3.3	1.7		ns
t_{SU}	Set up time nD_n to nCP	3, 4	1.0	0.2		1.2	0.3		ns
t_h	Hold time nD_n to nCP	3, 4	0.8	0.4		0.6	–0.3		ns
F_{max}	Maximum clock pulse frequency	1, 4	150	350		150	300		MHz

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. All typical values are at V_{CC} = 3.3V

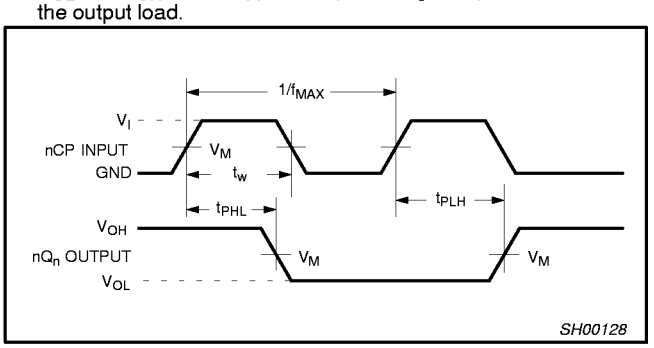
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

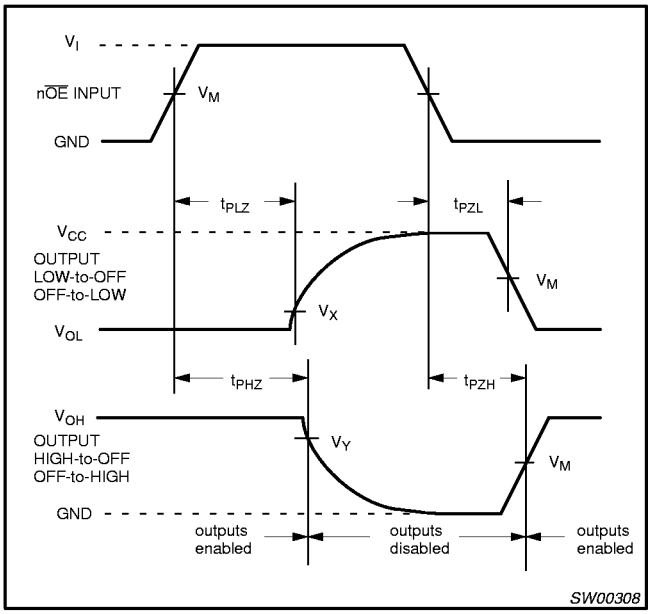
1. V_M = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH} - 0.15V$
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

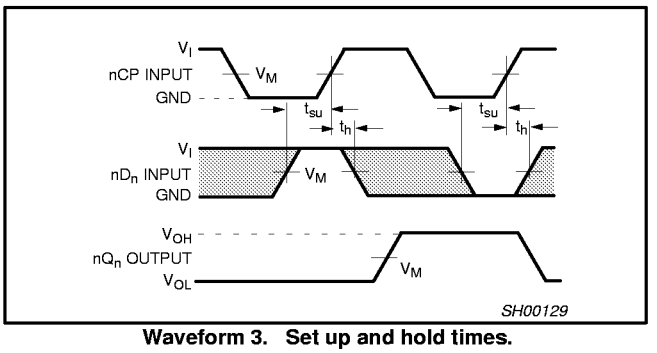
1. V_M = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH} - 0.3V$
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. The input (nCP) to output propagation delays.

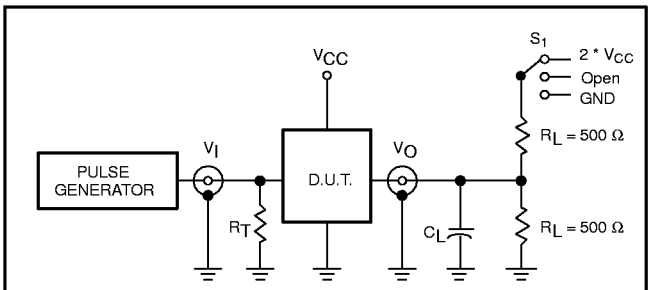


Waveform 2. The 3-State enable and disable times.



Waveform 3. Set up and hold times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

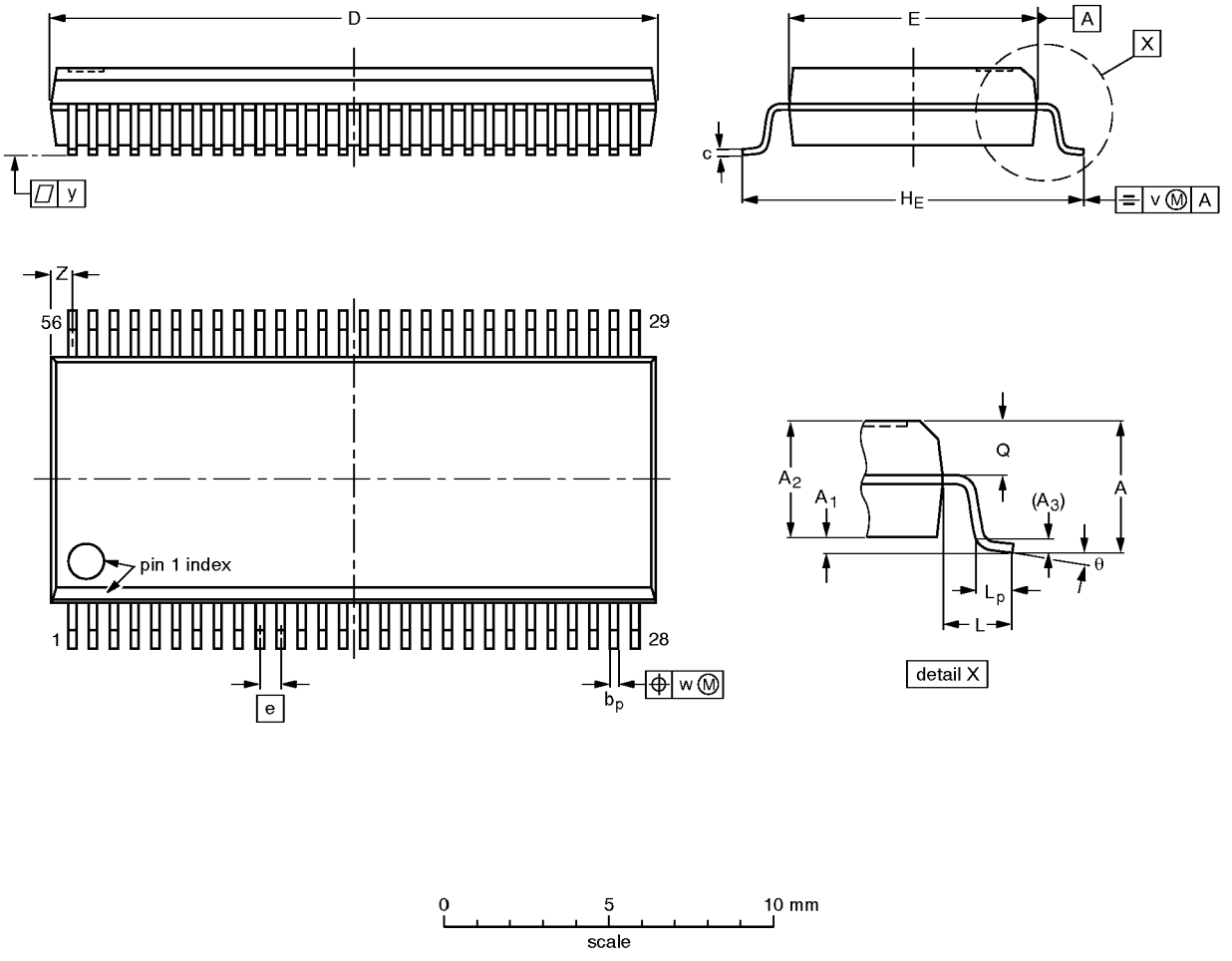
SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 < V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Waveform 4. Load circuitry for switching times

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

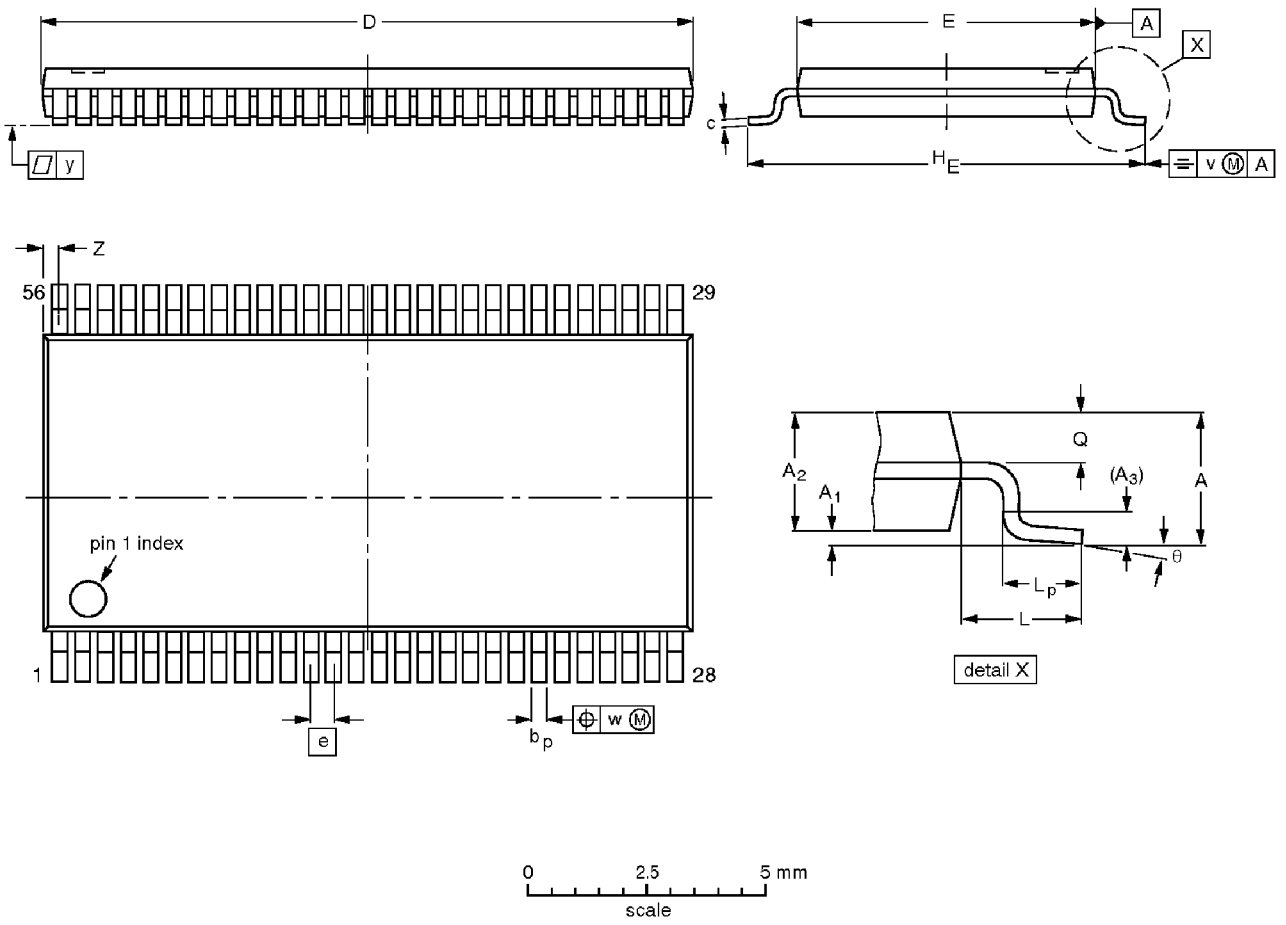
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10