ZL50075

32 K Channel Digital Switch with High Jitter Tolerance, Rate Conversion per Group of 2 Streams (8, 16, 32 or 64 Mbps), and 64 Inputs and 64 Outputs

Data Sheet

January 2004

Features

- 32,768 channel x 32,768 channel non-blocking digital Time Division Multiplex (TDM) switch at 65.536 Mbps or 32.768 Mbps or using a combination of rates
- 16,384 channel x 16,384 channel non-blocking digital TDM switch at 16.384 Mbps
- 8,192 channel x 8,192 channel non-blocking digital TDM switch at 8.192 Mbps
- High jitter tolerance with multiple input clock sources and frequencies
- Up to 64 serial TDM input streams, divided into 32 groups with 2 input streams per group
- 64 serial TDM output streams, divided into 32 groups with 2 output streams per group
- Per-group input and output data rate conversion selection at 65.536 Mbps, 32.768 Mbps, 16.384 Mbps and 8.192 Mbps. Input and output data group rates can differ
- Per-stream input bit delay for flexible sampling point selection
- Per-stream output fractional bit advancement
- Three sets of output timing signals for interfacing additional devices

Ordering Information

ZL50075GA 3244 Ball PBGA

-40°C to +85°C

- Per-channel A-Law/μ-Law Translation
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per-stream Bit Error Rate (BER) test circuits
- Per-channel high impedance output control
- Per-channel force high output control
- Per-channel message mode
- Control interface compatible with Intel and Motorola 16 bit non-multiplexed buses
- Connection memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE 1149.1 (JTAG) test port
- 3.3 V I/O with 5V tolerant inputs; 1.8 V core voltage

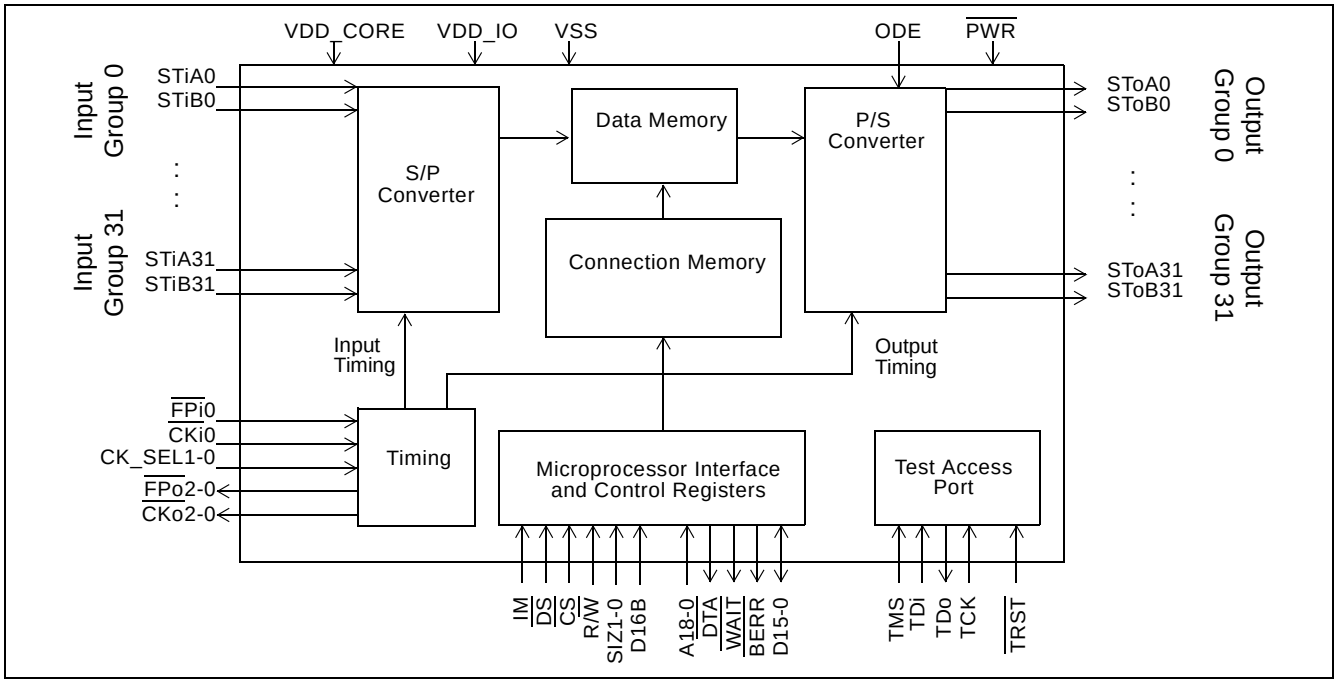

Figure 1 - ZL50075 Functional Block Diagram

Applications

- Large Switching Platforms
- Central Office Switches
- Wireless Base Stations
- Multi-service Access Platforms
- Media Gateways

Description

The ZL50075 is a maximum, 32,768 x 32,768 channel non-blocking Time Division Multiplex (TDM) switch. The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. With a number of enhanced features, the ZL50075 is designed for high capacity voice and data switching applications.

The ZL50075 has 64 input streams and 64 output data streams which can be programmed to operate at 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. The large number of inputs and outputs maintains full 32K x 32 K channel switching capacity at bit rates of 65 Mbps or 32 Mbps. Up to 32 input and output data streams may operate at 65 Mbps. Up to 64 input and output data streams may operate at 32 Mbps, 16 Mbps or 8 Mbps. The data rate can be independently set in groups of 2 input or output streams. In this way it is possible to provide rate conversion from input data channel to output data channel.

The ZL50075 uses a master clock ($\overline{\text{CKi0}}$) and frame pulse ($\overline{\text{FPi0}}$) to define the TDM data stream frame boundary and timing.

The ZL50075 has a variety of user configurable options designed to provide flexibility when data streams are connected to multiple TDM components or circuits. These include:

- Variable input bit delay and output advancement, to accommodate delays and frame offsets of streams connected through different data paths
- Four timing outputs, $\overline{\text{CKo}}$1 - 0 and $\overline{\text{FPo}}$1 - 0, which can be configured independently to provide a variety of clock and frame pulse options
- Support of both ST-BUS and GCI-Bus formats

The ZL50075 also has a number of value added features for voice and data applications:

- Per-channel variable delay mode for low latency applications and constant delay mode for frame integrity applications
- Per-channel A-Law/µ-Law Conversions for voice
- 64 separate Pseudo-random Bit Sequence (PRBS) test circuits; one per stream. This provides an integrated Bit Error Rate (BER) test capability to facilitate data path integrity checking

The ZL50075 has two modes of operation: Connection Mode (normal) and Message Mode. In Connection Mode, data bytes received at the TDM inputs are switched to timeslots in the output data streams, with mapping controlled by the Configuration Memory. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

A non-multiplexed microprocessor port provides access to the internal Data Memory, Connection Memory and Control Registers used to program ZL50075 options. The port is configurable to interface with either 16 bit Motorola or Intel-type microprocessors.

The mandatory requirements of IEEE 1149.1 standard are supported via the dedicated Test Access Port.

Pin Diagram (as viewed through top of package)

A1 corner identified by metallized marking.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	D[15]	D[14]	D[5]	D[4]	D[3]	A[18]	A[17]	A[13]	A[12]	A[11]	A[8]	A[4]	A[2]	A[0]	R/$\overline{W}$	$\overline{DS}$	IC	$\overline{DTA}$
B	STOA [1]	IM	D[11]	D[10]	D[8]	D[7]	D[6]	D[1]	A[15]	A[10]	A[5]	A[1]	NC	$\overline{CS}$	SIZ[0]	$\overline{PWR}$	STOA [31]	SIZ[1]
C	STIA [2]	STIB [1]	STIA [0]	STIB [0]	STOA [0]	D[13]	D[9]	D[0]	A[14]	A[9]	A[6]	$\overline{BERR}$	$\overline{WAIT}$	STIB [31]	TDO	STIA [31]	$\overline{TRST}$	NC
D	STOB [2]	$\overline{CKO}$ [0]	STIA [1]	STOB [0]	VDD_CORE	D[12]	D[2]	VDD_CORE	A[16]	VDD_IO	A[7]	A[3]	VDD_IO	TCK	VDD_CORE	TMS	STOB [30]	STOB [31]
E	STIA [3]	STIB [2]	STOB [1]	$\overline{FPO}$ [0]	VSS	VSS	VDD_CORE	VDD_IO	VSS	VDD_CORE	VDD_IO	VSS	VDD_CORE	VDD_IO	TDI	STOA [30]	STIB [30]	STIA [30]
F	STOB [3]	STIB [3]	STOA [2]	VDD_CORE	VDD_IO	VSS	VSS	VDD_CORE	VDD_IO	VSS	VDD_CORE	VDD_IO	VSS	VDD_CORE	STOB [29]	STIB [29]	STOA [29]	STIA [29]
G	STOA [3]	STIB [4]	STIA [4]	VDD_IO	VDD_CORE	VDD_IO	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO	VSS	VDD_IO	STIB [28]	STOB [28]	STOA [28]
H	VSS	VSS	STOA [4]	STOB [4]	VSS	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	VDD_IO	VSS	STOA [27]	STOB [27]	STIA [28]
J	STIA [5]	STOA [5]	STIB [5]	STOB [5]	VDD_IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	STOA [26]	STOB [26]	VSS	STIB [27]
K	ODE	STIA [6]	STIA [7]	STOA [6]	VDD_CORE	VDD_IO	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO	VSS	STIB [25]	IC	STOA [25]	STIA [27]
L	STIB [6]	STOB [6]	IC	STIA [8]	VSS	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	VDD_IO	STIA [24]	STOA [24]	STOB [24]	IC
M	STIB [7]	STOA [7]	STOB [8]	VDD_CORE	VDD_IO	VDD_IO	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO	VDD_CORE	VDD_CORE	STIA [23]	STOB [23]	STIB [26]
N	STOB [7]	STIB [8]	STIB [9]	VDD_IO	VDD_CORE	VSS	VSS	VDD_CORE	VDD_IO	VSS	VDD_CORE	VDD_IO	VSS	VSS	VDD_IO	STOA [22]	STOB [22]	STIA [26]
P	IC	STIA [9]	STIA [10]	STOB [10]	VSS	VSS	VDD_CORE	VDD_IO	VSS	VDD_CORE	VSS	VSS	VDD_CORE	VDD_IO	STOA [21]	STOB [21]	NC	STOB [25]
R	STOA [8]	STOB [9]	STOA [10]	STIA [12]	VDD_IO	STOA [13]	STIA [15]	VDD_CORE	STOA [15]	VDD_IO	STIB [17]	IC	VDD_IO	STIB [19]	VDD_CORE	STIA [21]	STIA [22]	STIA [25]
T	STOA [9]	STIB [10]	STIA [11]	STOA [11]	STOA [12]	STIA [13]	STOB [13]	STIB [15]	STOB [16]	$\overline{FPI}$ [0]	STIA [17]	IC	STIA [18]	STIA [19]	STIA [20]	STOA [20]	NC	STIB [24]
U	STIB [11]	STOB [11]	STIB [12]	$\overline{CKO}$ [1]	STIA [14]	STIB [14]	STOB [15]	STIA [16]	STOA [16]	IC	NC	STOB [17]	CK_SEL[0	STOB [18]	STOB [19]	STOB [20]	STIB [21]	STOA [23]
V	STOB [12]	$\overline{FPO}$ [1]	STIB [13]	STOA [14]	STOB [14]	STIB [16]	$\overline{CKI}$ [0]	NC	IC	IC	STOA [17]	CK_SEL[1]	STIB [18]	STOA [18]	STOA [19]	STIB [20]	STIB [22]	STIB [23]

Table 1 - ZL50075 19 mm x 19 mm 484 Ball PBGA

Pin Description

Pin	Name	Description
TDM Interface		
C3, D3, C1, E1, G3, J1, K2, K3, L4, P2, P3, T3, R4, T6, U5, R7, U8, T11, T13, T14, T15, R16, R17, M16, L15, R18, N18, K18, H18, F18, E18, C16,	STiA0-31	**Serial TDM Input Data 'A' Streams (5 V Tolerant Input with Internal Pull-down)** 32 serial TDM input data streams. All streams are at the same rate: either 65.536 Mbps, 32.678 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Group Control Registers, see Section 18.0. Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.
C4, C2, E2, F2, G2, J3, L1, M1, N2, N3, T2, U1, U3, V3, U6, T8, V6, R11, V13, R14, V16, U17, V17, V18, T18, K15, M18, J18, G16, F16, E17, C14	STiB0-31	**Serial TDM Input Data 'B' Streams (5 V Tolerant Input with Internal Pull-down)** 32 serial TDM input data streams. All streams are at the same rate: 32.678 Mbps, 16.384 Mbps or 8.192 Mbps. These pins are activated only when inputs are programmed for 32 Mbps, 16 Mbps or 8 Mbps operation via the Group Control Registers, see Section 18.0. When not activated, or not used, these pins are pulled low by internal pull-down resistors and may be left unconnected.
C5, B1, F3, G1, H3, J2, K4, M2, R1, T1, R3, T4, T5, R6, V4, R9, U9, V11, V14, V15, T16, P15, N16, U18, L16, K17, J15, H16, G18, F17, E16, B17	SToA0-31	**Serial TDM Output Data 'A' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** 32 serial TDM output data streams. All streams are at the same rate: either 65.536 Mbps, 32.678 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Group Control Registers, see Section 18.0.
D4, E3, D1, F1, H4, J4, L2, N1, M3, R2, P4, U2, V1, T7, V5, U7, T9, U12, U14, U15, U16, P16, N17, M17, L17, P18, J16, H17, G17, F15, D17, D18	SToB0-31	**Serial TDM Output Data 'B' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** 32 serial TDM output data streams. All streams in are at the same rate: 32.678 Mbps, 16.384 Mbps or 8.192 Mbps. These pins are activated when outputs are programmed for 32 Mbps, 16 Mbps or 8 Mbps operation via the Group Control Registers, see Section 18.0. When not activated, these outputs are high impedance.
V7	$\overline{\text{CKi0}}$	**ST-BUS/GCI-Bus Clock Input (5 V Tolerant Schmitt-Triggered Input)** This pin accepts an 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz clock. This clock must be provided for correct operation of the ZL50075. The frequency of the $\overline{\text{CKi0}}$ input is selected by the CK_SEL1-0 inputs. The active clock edge may be either rising or falling, programmed by the Input Clock Control Register, see Section 18.1.

Pin Description (continued)

Pin	Name	Description
T10	$\overline{\text{FPi0}}$	**ST-BUS/GCI-Bus Frame Pulse Input (5 V Tolerant Input)** This pin accepts the 8 kHz frame pulse which marks the frame boundary of the TDM data streams. The pulse width is nominally one $\overline{\text{CKi0}}$ clock period (Assuming ST-BUS mode) selected by the CK_SEL1-0 inputs. The active state of the frame pulse may be either high or low, programmed by the Input Clock Control Register, see Section 18.1.
D2, U4	$\overline{\text{CKo}}$0-1	**ST-BUS/GCI-Bus Clock Outputs (3.3 V Outputs with Slew-Rate Control)** These clock outputs can be programmed to generate an 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz TDM clock output. The active edge can be programmed to be either rising or falling. The source of the clock outputs can be derived from either the $\overline{\text{CKi0}}$ inputs or the internal system clock. The frequency, active edge and source of each clock output can be programmed independently by the Output Clock Control Register, see Section 18.2.
E4, V2	$\overline{\text{FPo}}$0-1	**ST-BUS/GCI-Bus Frame Pulse Outputs (3.3 V Outputs with Slew-Rate Control)** These 8 kHz output pulses mark the frame boundary of the TDM data streams. The pulse width is nominally one clock period of the corresponding $\overline{\text{CKo}}$ output. The active state of each frame pulse may be either high or low, independently programmed by the Output Clock Control Register, see Section 18.2.
U13, V12	CK_SEL0-1	**TDM Master Clock Input Select** Inputs used to select the frequency and frame alignment of $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$: CK_SEL1 = 0, CK_SEL0 = 0, 8.192 MHz CK_SEL1 = 0, CK_SEL0 = 1, 16.384 MHz CK_SEL1 = 1, CK_SEL0 = 0, 32.768 MHz CK_SEL1 = 1, CK_SEL0 = 1, 65.536 MHz
K1	ODE	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)** This is the asynchronous output enable control for the output streams. When it is high, the streams are enabled. When it is low, the output streams are tristated.
Microprocessor Port and Reset		
A1, A2, C6, D6, B3, B4, C7, B5, B6, B7, A3, A4, A5, D7, B8, C8	D15-0	**Microprocessor Port Data Bus (5 V Tolerant Bi-directional with Slew-Rate Output Control)** 16 bit bi-directional data bus. Used for microprocessor access to internal memories and registers.
A6, A7, D9, B9, C9, A8, A9, A10, B10, C10, A11, D11, C11, B11, A12, D12, A13, B12	A18-1	**Microprocessor Port Address Bus (5 V Tolerant Inputs)** 17 bit address bus. Note A0 is not used and should be connected to logic 0.
B14	$\overline{\text{CS}}$	**Chip Select Input (5 V Tolerant Input)** Active low input used with $\overline{\text{DS}}$ to enable read and write access to the ZL50075.

Pin Description (continued)

Pin	Name	Description
A16	$\overline{DS}$	**Data Strobe Input (5 V Tolerant Input)** Active low input used with $\overline{CS}$ to enable read and write access to the ZL50075.
A15	R/$\overline{W}$	**Read/Write Input (5 V Tolerant Input)** Input signal, controls the type of access 0 - Microprocessor write to the ZL50075 1 - Microprocessor read from the ZL50075
A18	$\overline{DTA}$	**Data Transfer Acknowledge (5V Tolerant, 3.3V Tri-state Output with Slew-Rate)** Active low output which indicates a data bus transfer is complete. An external pull-up resistor is required to hold a HIGH level when output is high-impedance.
C12	$\overline{BERR}$	**Transfer Bus Error Output with Slew Rate Control (5 V Tolerant, 3.3 V Tri-state Outputs with Slew-Rate Control)** Active low This pin is active low whenever the microprocessor attempts to access an invalid memory space inside the device. In Motorola bus mode, if this bus error signal is activated, the data transfer acknowledge signal, $\overline{DTA}$, will not be generated. In Intel bus mode, the generation of the $\overline{DTA}$ is not affected by this $\overline{BERR}$ signal. An external pull-up resistor is required to hold a HIGH level when output is high-impedance.
C13	$\overline{WAIT}$	**Data Transfer Wait Output (5 V Tolerant, 3.3 V Tri-state Output with Slew Rate)** Active low wait signal output.
B15, B18	SIZ0-1	**Data Transfer Size/Upper and Lower Data Strobe Inputs (5 V Tolerant Inputs)** Motorola mode: SIZ0 - $\overline{LDS}$, SIZ1 - $\overline{UDS}$. Active low upper and lower data strobes, $\overline{UDS}$ and $\overline{LDS}$, indicate whether the upper byte, D15-8, and/or lower byte, D7-0, is being transferred. Intel mode: SIZ0 - $\overline{BE0}$, SIZ1 - $\overline{BE1}$. Active low Intel type bus-enable signal $\overline{BE1}$ and $\overline{BE0}$ signals
B2	IM	**Microprocessor Port Bus Mode Select (5 V Tolerant Input)** Control input: 0 = Motorola mode 1 = Intel mode
B16	$\overline{PWR}$	**Device Reset (5 V Tolerant Schmitt-Triggered Input)** Asynchronous reset input used to initialize the ZL50075. 0 = Reset 1 = Normal See Section 11.3, Initialization for detailed description of Reset state.
IEEE 1149.1 (JTAG) Test Access Port (TAP)		
E15	TDI	**Test Data (5 V Tolerant Input with Internal Pull-up)** Serial test data input. When not used, this input may be left unconnected.
C15	TDO	**Test Data (3.3 V Output)** Serial test data output.

Pin Description (continued)

Pin	Name	Description
D14	TCK	**Test Clock (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)** Clock input used by TAP Controller. When not used, this input may be left unconnected.
D16	TMS	**Test Reset (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)** Input which controls the state transitions of the TAP Controller. When not used, this input may be left unconnected.
C17	$\overline{\text{TRST}}$	**Test Mode Select (5 V Tolerant Input with Internal Pull-up)** Active low, asynchronous test reset input which initializes the TAP Controller during JTAG testing. This pin must be held at logic 0 for normal operation of the ZL80009.
Unused		
U10, V9, V10, R12, L18, A17, L3, P1, T12, K16, A14	IC, A0	**Internal Connections** In normal mode these pins **MUST** be connected low.
B13, C18, P17, T17, U11, V8	NC	**No Connection** In normal mode these pins **MUST** be left unconnected.
Power		
E5, E6, E9, E12, F6, F7, F10, F13, G7, G8, G9, G10, G11, G12, G14, H1, H2, H5, H7, H8, H9, H10, H11, H12, H15, J6, J7, J8, J9, J10, J11, J12, J13, J17, K7, K8, K9, K10, K11, K12, K14, L5, L7, L8, L9, L10, L11, L12, M7, M8, M9, M10, M11, M12, N6, N7, N10, N13, N14, P5, P6, P9, P11, P12	V_{SS}	**Ground**
D5, D8, D15, E7, E10, E13, F4, F8, F11, F14, G5, H6, H13, J14, K5, L13, L6, M4, M14, M15, N5, N8, N11, P7, P10, P13, R8, R15	V_{DD_CORE}	**Power Supply for the Core Logic:** +1.8 V
D10, D13, E8, E11, E14, F5, F9, F12, G4, G6, G13, G15, H14, J5, K6, K13, L14, M5, M6, M13, N4, N9, N12, N15, P8, P14, R5, R10, R13	V_{DD_IO}	**Power Supply for the I/O:** +3.3 V

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1.0 Functional Description

1.1 Overview

The device has 64 ST-BUS/GCI-Bus inputs (STiA0 - 31 and STiB0 - 31) and 64 ST-BUS/GCI-Bus outputs (SToA0 - 31 and SToB0 - 31). It is a non-blocking digital switch with 32,768 64 kbps channels and is capable of performing rate conversion between groups of 2 inputs and 2 outputs. The inputs accept serial input data streams with data rates of 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. There are 32 input groups with each group consisting of 2 streams (‘A’ and ‘B’). Each group can be set to any of the data rates. The outputs deliver serial data streams with data rates of 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. There are 32 output groups with each group consisting of 2 streams (‘A’ and ‘B’). Each group can be set to any of the data rates.

By using Zarlink’s message mode capability, the microprocessor can store data in the connection memory which can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The ZL50075 uses the ST-BUS/GCI-Bus master input frame pulse ($\overline{\text{FPi0}}$) and the ST-BUS/GCI-Bus master input clock ($\overline{\text{CKi0}}$) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates (8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps). The rate of the input clock is defined by setting the CK_SEL1 - 0 pins.

A selectable Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port is a 16 bit data bus and a 17 bit address bus. There are seven control signals ($\overline{\text{CS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, $\overline{\text{DTA}}$, $\overline{\text{WAIT}}$, $\overline{\text{BERR}}$ and IM).

The device supports the mandatory requirements for the IEEE 1149.1 (JTAG) standard via the test port.

1.2 Switch Operation

The ZL50075 switches 64 kbps and Nx64 kbps data and voice channels from the TDM input streams, to timeslots in the TDM output streams. The device is non-blocking; all 32 K input channels can be switched through to the outputs. Any input channel can be switched to any available output channel.

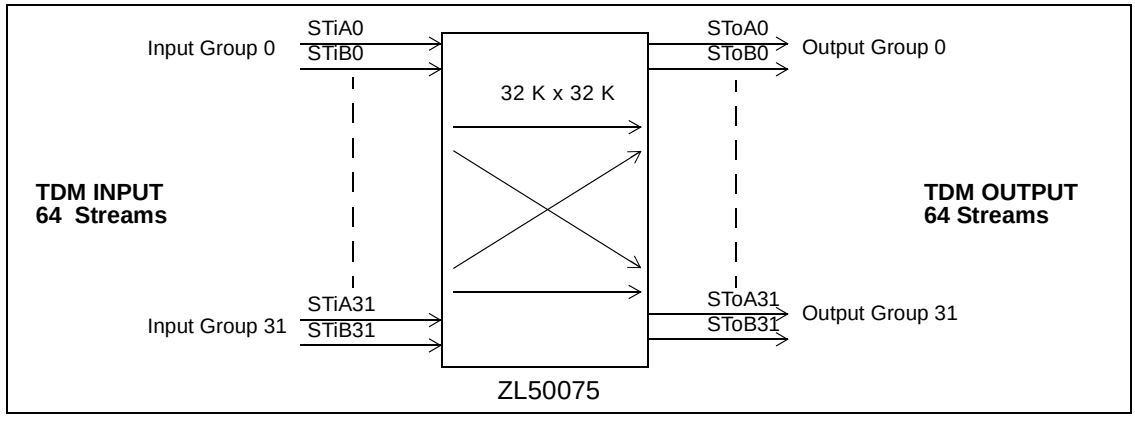


Figure 2 - 32 K x 32 K Channel Basic Switch Configuration

The maximum channel switching capacity is determined by the number of streams and their rate of operation, see Table 1.

TDM Group Data Rate	Maximum Number of Input TDM Data Streams	Maximum Number of Output TDM Data Streams	Number of 64 kbps Channels per Stream	Maximum Switch Capacity† (streams x channels = total)
65.536 Mbps	32	32	1024	32x1024 = 32,768
32.768 Mbps	64	64	512	64x512 = 32,768
16.384 Mbps	64	64	256	64x256 = 16,384
8.192 Mbps	64	64	128	64x128 = 8,192‡

Table 1 - Data Rate and Maximum Switch Size

† The maximum capacity shown is when all streams are at the same rate, and none are operating at 8.192 Mbps.

‡ Switch capacity is limited to less than 32 K channels, only when streams are provisioned at 16 Mbps or 8 Mbps. The maximum switch capacity in this case is given by 32,768 - (N x 128), where N is the number of 16 Mbps or 8 Mbps input or output streams.

1.3 Stream Provisioning

The ZL50075 is a large switch with a comprehensive list of user configurable, 'per-group' programmable features. In order to facilitate ease of use, the ZL50075 offers a simple programming model. Streams are grouped in sets of two, with each group sharing the same configured characteristics. In this way it is possible to reduce programming complexity, while still maintaining flexible 'per-stream' configuration options:

- Input and output rate selection, see Section 1.4
- Input stream clock source selection, see Section 2.0
- Output stream clock source selection, see Section 3.0
- Input stream sampling point selection, see Section 5.1
- Output stream fractional bit advance, see Section 5.2
- Input and output stream inversion control, see Section 8.0

The streams are grouped, one from the TDM 'A' streams, combined with the corresponding 'B' stream. For example, input stream group #12 is STiA12 and STiB12, and output stream group #4 is SToA4 and SToB4. There are 32 input and 32 output groups. Depending on the data rate set for the group there will be between 1 and 2 streams activated. If the data rate is set for 65.536 Mbps, the 'A' stream will be activated and the 'B' stream will not be activated. If the data rate is set for 32.768 Mbps, 16.384 Mbps or 8.192 Mbps, the 'A' and 'B' streams will be activated. The maximum channel capacity of a group is 1024 channels when operating at 65 Mbps or 32 Mbps. The switch capacity is reduced to 512 channels when operating at 16 Mbps and to 256 channels when operating at 8 Mbps.

1.4 Input and Output Rate Selection

Table 1 shows the maximum number of streams available at different bit rates. The ZL50075 deactivates unused streams when operating at the higher bit rates as shown in Table 2.

Input or Output Group n (n = 0 - 31)	65 Mbps	32 Mbps	16 Mbps	8 Mbps
STiAn / SToAn	Active	Active	Active	Active
STiBn / SToBn	Not Active	Active	Active	Active

Table 2 - TDM Stream Bit Rates

For 65 Mbps operation, only those inputs and outputs in the TDM 'A' streams are active. For 32 Mbps, 16 Mbps and 8 Mbps operation, the inputs and outputs in the TDM 'A' and 'B' streams are active.

1.4.1 Per Stream Rate Selection

See Section 18.0, Group Control Registers, for programming details. The data rates are set with the Input Stream Bit Rate (bits 3 - 2) and the Output Stream Bit Rate (bits 19 - 18) in the Group Control Register0 - 31 (SCR0 - 31)

For the ZL50075, the bit rate of the inputs and outputs is programmed independently, in groups of 2 streams. Depending on the rate programmed, the active streams in the group will be as indicated in Table 2.

For example:

- if input stream group #1 is programmed for 65 Mbps: STiA1 is active; STiB1 is not active
- if output stream group #15 is programmed for 32 Mbps, 16 Mbps or 8 Mbps: SToA15 and SToB15 are active

1.5 Rate Conversion

The ZL50075 supports rate conversion from any input stream rate to any output stream rate.

The output stream rates do not have to follow the input stream rates, and the total capacity of both the input and the output is 32,768 channels. For example, on the input side of the switch you can have 24 streams operating at 65.536 Mbps (24,576 channels - 24 groups with 1 stream in each group), 8 streams operating at 32.768 Mbps (4096 channels - 4 groups with 2 streams in each group) and 8 streams operating at 16.384 Mbps (2048 channels - 4 groups with 2 streams in each group) with no streams operating at 8.192 Mbps. This results in an input capacity of 30,720 input channels. This is less than the full capacity of the device as some groups are operating at less than 32 Mbps. As the output streams do not have to follow the input streams, they can be configured so that 15 streams operate at 65.536 Mbps (15,360 channels - 15 groups with 1 stream in each group), 28 streams operate at 32.768 Mbps (14,336 channels - 14 groups with 2 streams in each group), 2 streams operate at 16.384 Mbps (512 channels - 1 group with 2 streams in the group) and 4 streams operate at 8.192 Mbps (512 channels - 2 groups with 2 streams in each group). This results in an output capacity of 30,720 output channels. This is less than the full capacity of the device as some groups are operating at less than 32 Mbps.

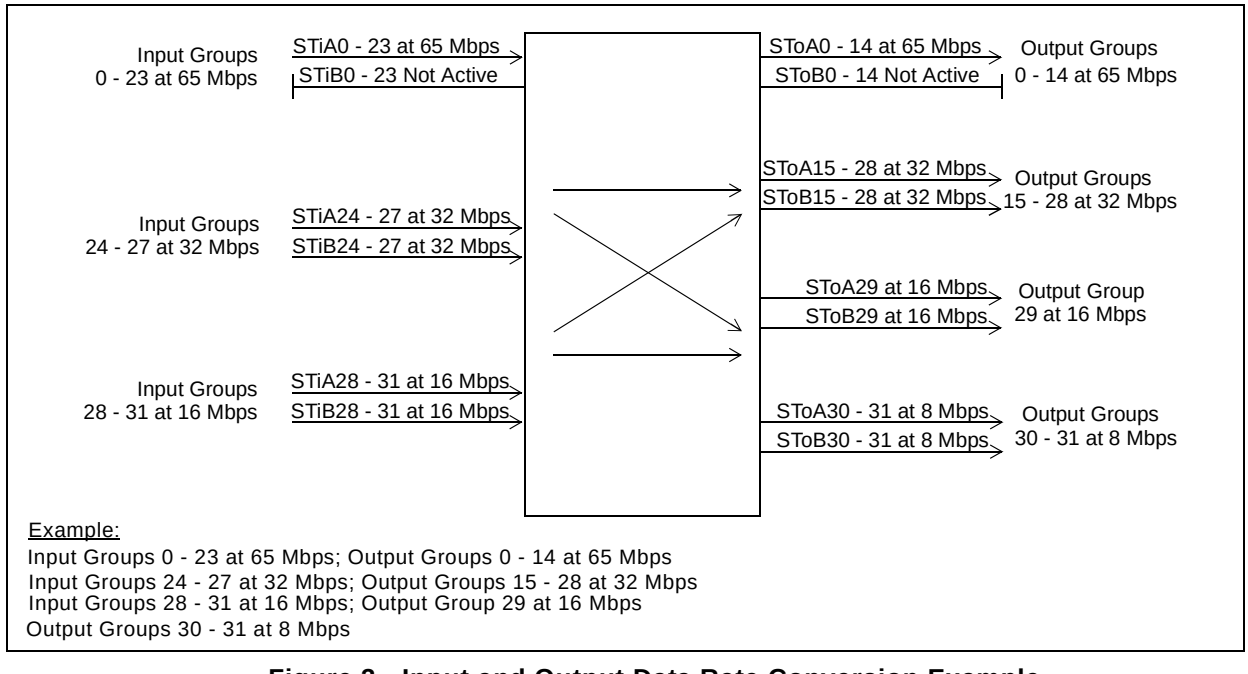


Figure 3 - Input and Output Data Rate Conversion Example

2.0 Input Clock ($\overline{CKi}$) and Input Frame Pulse ($\overline{FPi}$) Timing

The input timing for the ZL50075 can be set for one of four different input values. They can be set for ST-BUS or GCI-Bus with positive or negative input. The $\overline{CKi}$0 and $\overline{FPi}$0 input timing must be provided in order for the device to be used. There are two additional input clocks and frame pulses that can be provided. $\overline{CKi}$0 is used to generate the internal clock. This clock is used for all internal logic and can be used as one of the clocks that defines the timing for the input and output data. The input stream clock source is selected by the ISSRC1 - 0 (bits 1 - 0) in the Group Control Register. The output stream clock source is selected bt the OSSRC1 - 0 (bits 17 - 16) in the Group Control Register.

The $\overline{CKi}$0 and $\overline{FPi}$0 input values are set via the CK_SEL1 - 0 pins as shown in Table 3. By default the $\overline{CKi}$0 and $\overline{FPi}$0 pins accept ST-BUS, negative input timing. By setting the GCISEL0 (bit 2) in the Input Clock Control Register (ICCR) the input timing is set for GCI-Bus mode. The FPIPOL0 (bit 1) in the Input Clock Control Register (ICCR) sets the input frame pulse is positive. The CKIPSL0 (bit 0) in the Input Clock Control Register (ICCR) sets the input clock is positive.

CK_SEL1	CK_SEL0	Input $\overline{CKi}$0 and $\overline{FPi}$0
0	0	8.192 MHz
0	1	16.384 MHz
1	0	32.768 MHz
1	1	65.536 MHz

Table 3 - $\overline{CKi}$0 and $\overline{FPi}$0 Setting via CK_SEL1 - 0

3.0 Output Clock ($\overline{CKo}$) and Output Frame Pulse ($\overline{FPo}$) Timing

There are two output timing pairs, $\overline{CKo}$1 - 0 and $\overline{FPo}$1 - 0. By default these signals generate ST-BUS, negative timing. Each can be set individually to produce 8.192 MHz, 16.384 MHz, 32.768 MHz or 65.536 MHz timing through the programming of the CKO1RATE1 - 0 (bits 10 - 9) and CKO0RATE1 - 0 (bits 3 - 2) in the Output Clock Control Register (OCCR). With the setting of the GCOSEL1 (bit 13) and GCOSEL0 (bit 6) in the Output Clock Control Register (OCCR) the output conforms the GCI-Bus standard. The signals can be adjusted to provide positive frame pulses with the setting of the FPOPOL1 (bit 12) and FPOPOL0 (bit 5) in the Output Clock Control Register (OCCR). The signals can be adjusted to provide positive clocks with the setting of the CKOPOL1 (bit 11) and CKOPOL0 (bit 4) in the Output Clock Control Register (OCCR). The output clocks use the CKO1SRC1 - 0 (bits 8 - 7) and CKO0SRC1- 0 (bits 1 - 0) in the Output Clock Control Register (OCCR) to set their timing reference to either the internal clock or one of the three input clock signals. If the input clocks are selected as the reference source, the output clock can not be programmed to generate a higher clock frequency than the reference source. As each output timing pair has its own bit settings, they can be set to provide different output timing.

4.0 Output Channel Control

To be able to interface with external buffers, the output signals can be set to enter a high impedance or drive high state on a per-channel basis. The Per Channel Function (bits 31 - 29) in the Connection Memory Bits can be set to 001 to drive the channel output high or to any one of the following, 000, 110 or 111 to set the channel into a high impedance state.

5.0 Data Input Delay and Data Output Advancement

The Group Control Register (SCR) is used to adjust the input delay and output advancement for each input and output data groups. Each group is independently programmed.

5.1 Input Sampling Point Delay Programming

The input sampling point delay programming feature provides users with the flexibility of handling different wire delays when incoming traffic is from different sources.

By default, all input streams have zero delay, such that bit 7 is the first bit that appears after the input frame boundary (Assuming ST-BUS formatting). The nominal input sampling point with zero delay is at the 3/4 bit time. The input delay is enabled by the Input Sample Point Delay (bit 8 - 4) in the Group Control Register0 - 31 (SCR0 - 31) as described in Section 18.0 on page 35. The input sampling point delay can range from 0 delay to 7 3/4 bit delay with a 1/4 bit resolution on a per group basis.

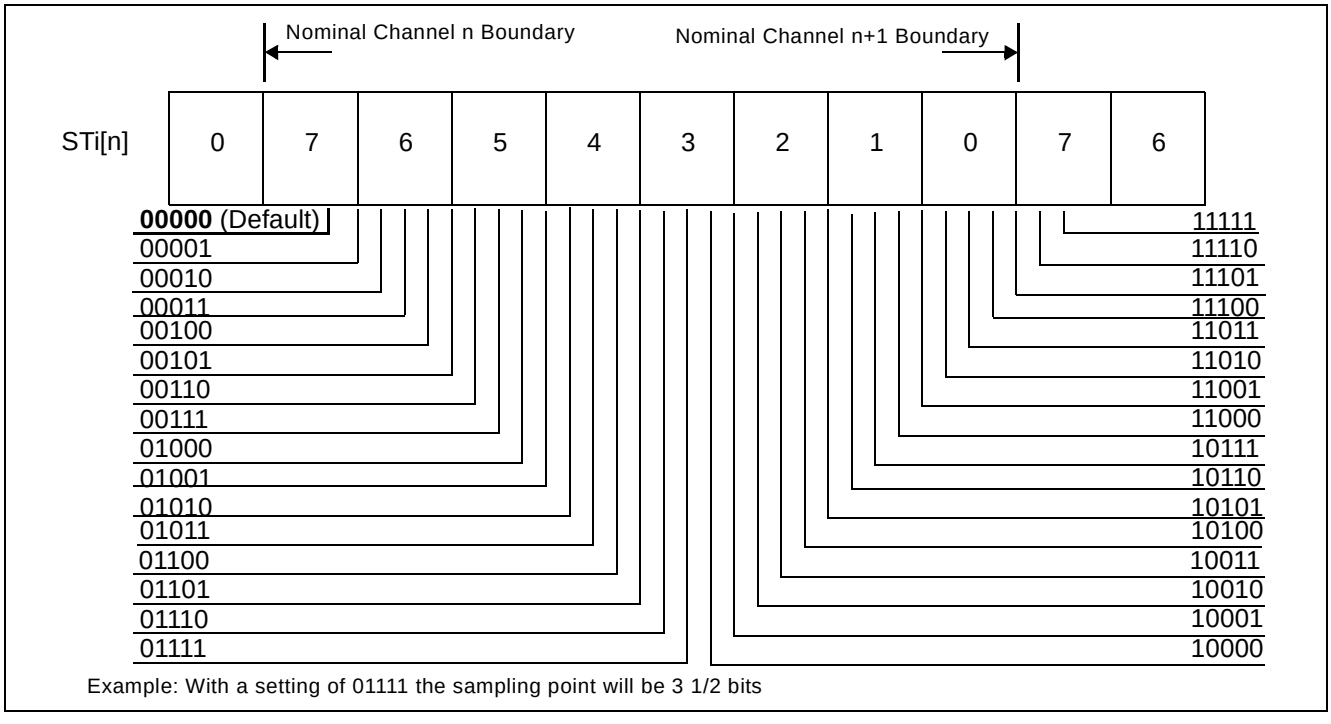


Figure 4 - Input Sampling Point Delay Programming

There are limitations when the ZL50075 is programmed to use $\overline{CKi}$2 - 0 as the input stream clock source as opposed to the internal clock:

- The granularity of the delay becomes 1/2 the selected reference clock period, or 1/4 bit, whichever is longer
- If the selected reference clock frequency is the same as the stream bit rate, the granularity of the delay is 1/2 bit. In this case, the least significant bit of the ISPD register is not used; the remaining 4 bits select the total delay in 1/2 bit increments, to a maximum of 7 1/2 bits. Also, the 0 bit delay reference point changes from the 3/4 bit position to the 1/2 bit position.

5.2 Fractional Bit Advancement on Output

See Section 18.0, Group Control Registers, for programming details.

This feature is used to advance the output data of groups with respect to the output frame boundary. Each group has its own bit advancement value which can be programmed in the Group Control Register0 - 31 (SCR0 - 31).

By default all output streams have zero bit advancement such that bit 7 is the first bit that appears after the output frame boundary (Assuming ST-BUS formatting). The output advancement is enabled by the Output Stream Bit Advancement (bits 21 - 20) of the Group Control Register0 - 31 (SCR0 - 31) as described in Section 18.0, Group Control Registers. The output delay can vary from 0 to 22.8 ns with a 7.6 ns increment. The exception to this is output streams programmed at 65 Mbps, in which case the increment is 3.8 ns with a total advancement of 11.4 ns.

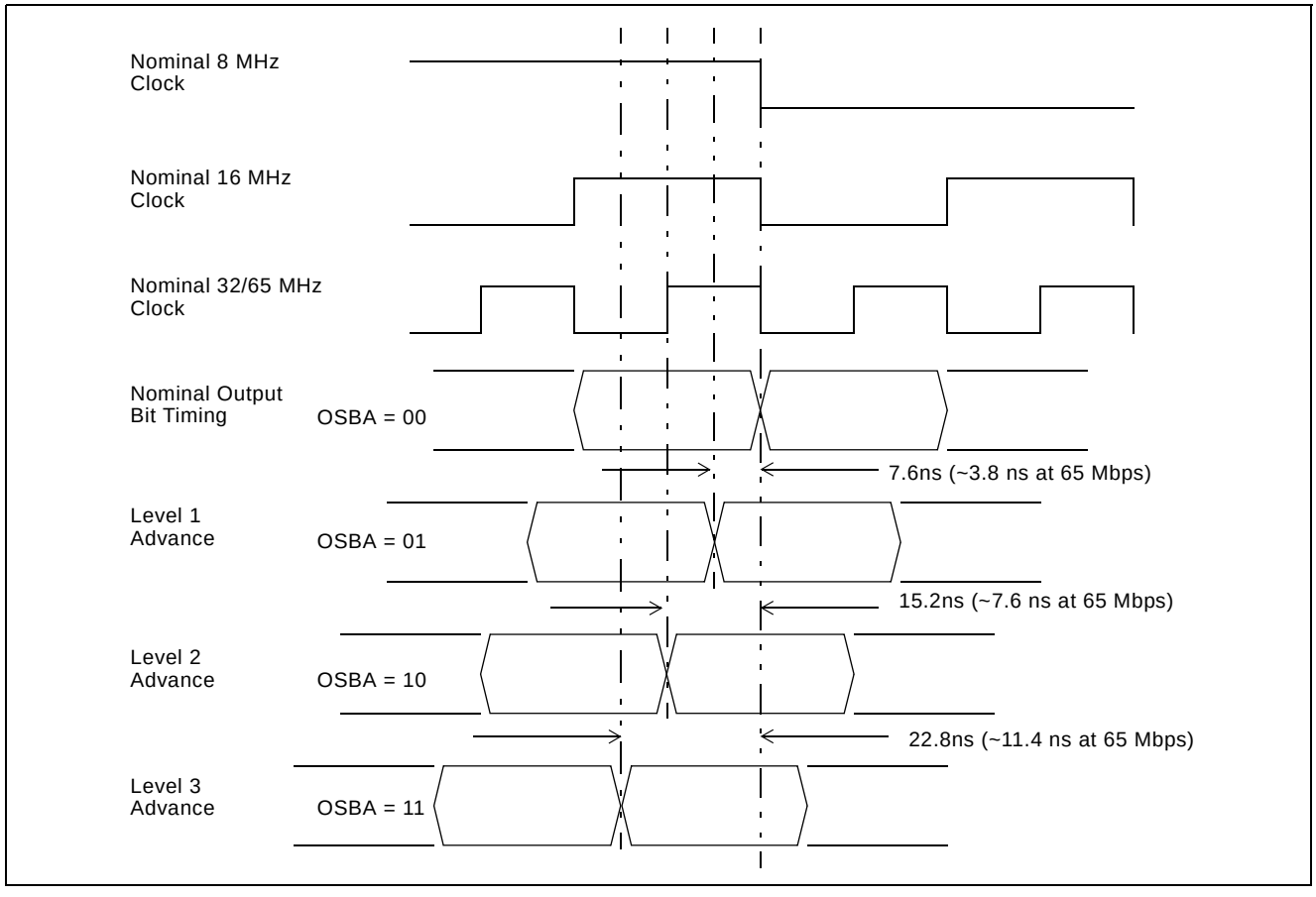


Figure 5 - Output Bit Advance Timing

This programming feature is provided to assist in designs where per stream routing delays are significant and different.

The OSBA bits, in the Group Control Registers, are used to set the bit-advance for each of the corresponding serial output streams. Figure 5 illustrates the effect of the OSBA settings on the output timing.

There are limitations when the ZL50075 are programmed to use $\overline{\text{CKi}}$2 - 0 as the output stream clock source:

- If the selected reference clock frequency is 65 MHz or 32 MHz, the granularity of the advance is reduced to 1/2 the clock period
- If the selected reference clock frequency is 16 MHz or 8 MHz, bit advancement is not available and the output streams are driven at the nominal times

6.0 Message Mode

In Message Mode (MSG), microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

For a given output channel, when the corresponding Per Channel Function (bits 31 - 29) in the Connection Memory Bits are set to Message Mode (010), the ZL50075 writes the Connection Address (bits 7 - 0) of the Connection Memory, in the outgoing timeslot. Refer to Section 14.1, Connection Memory Bit Functions, for programming details

To increase programming bandwidth, the ZL50075 has a separate addressable 32 bit memory location which provides direct access to the Connection Memory Least Significant Bytes (LSB), bits 7 - 0. Up to four consecutive message mode channels can by set with one Connection Memory LSB access. Refer to Section 15.0, Connection Memory LSB, for programming details.

6.1 Data Memory Read

All TDM input channels can be read via the microprocessor port. This feature is useful for receiving control and status information from external circuits or other TDM devices. Each 32 bit Data Memory access enables up to four consecutive input channels to be monitored. The Data Memory field is read only, any attempt to write to this address range will result in a bus error condition signalled back to the host processor. Refer to Section 16.0, Data Memory, for programming details.

The latency of data reads is up to 3 frames, depending on when the input timeslots are sampled.

6.2 Connection Memory Block Programming

See Section 18.3, Block Init Register, and Section 18.4, Block Init Enable Register, for programming details.

This feature allows for fast initialization of the connection memory after power up. When the block programming mode is enabled, the contents of Block Init Register are written to all Connection Memory Bits. This operation completes in one 125µs frame. During Connection Memory initialization, all TDM output streams are set to high impedance.

7.0 Data Delay Through the Switching Paths

See Section 14.1, Connection Memory Bit Functions, for programming details.

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data application, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by programming the Per Channel Function (bits 31 - 29) in the Connection Memory Bits. When these bits are set to 011, the channel is in variable delay mode. When they are set to 100, the channel is in constant delay mode.

7.1 Constant Delay Mode

In this mode the frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum delay of 1 frame + 1 channel if the last channel of a stream is switched to the first channel of a stream. The maximum delay is 1 channel short of 3 frames delay. This occurs when the first channel of a stream is switched to the last channel of a stream.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (n) and output channel number (m). The data throughput delay (T) is:

T = 2 frames + (n - m)

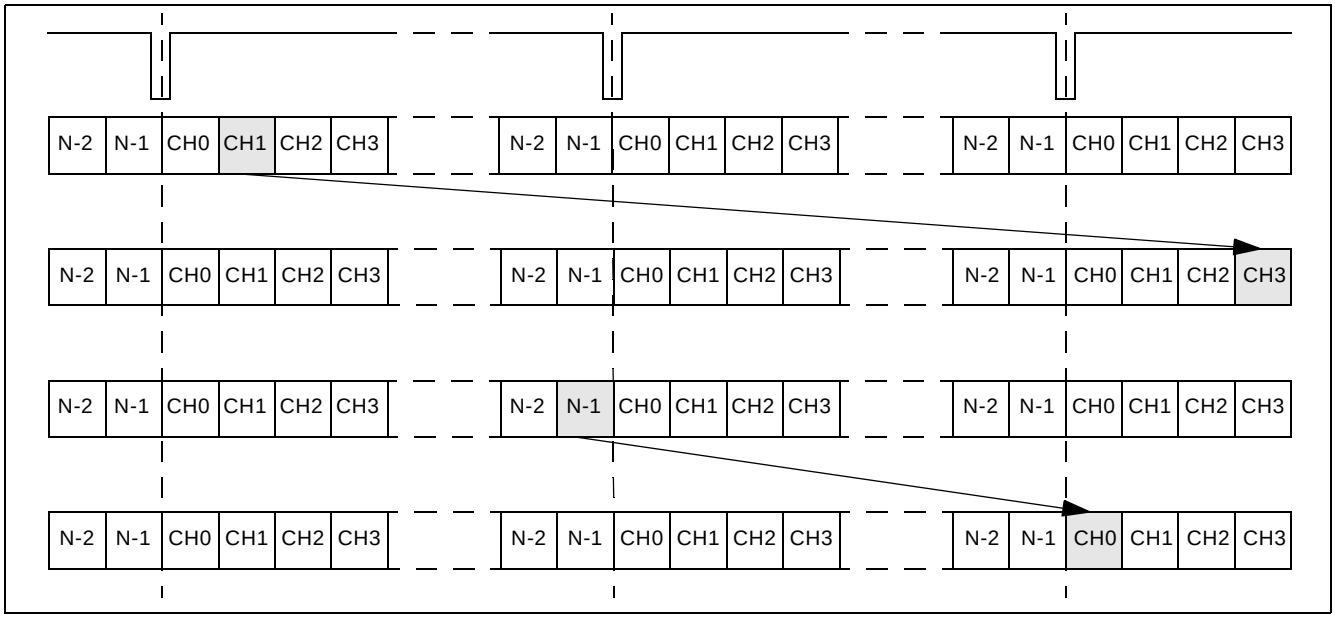


Figure 6 - Data Throughput Delay for Constant Delay

7.2 Variable Delay Mode

Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than data integrity. The delay through the switch can be as little as 3 channels to a maximum of 1 frame + 2 channels. Channels Available at Various Data Rate.

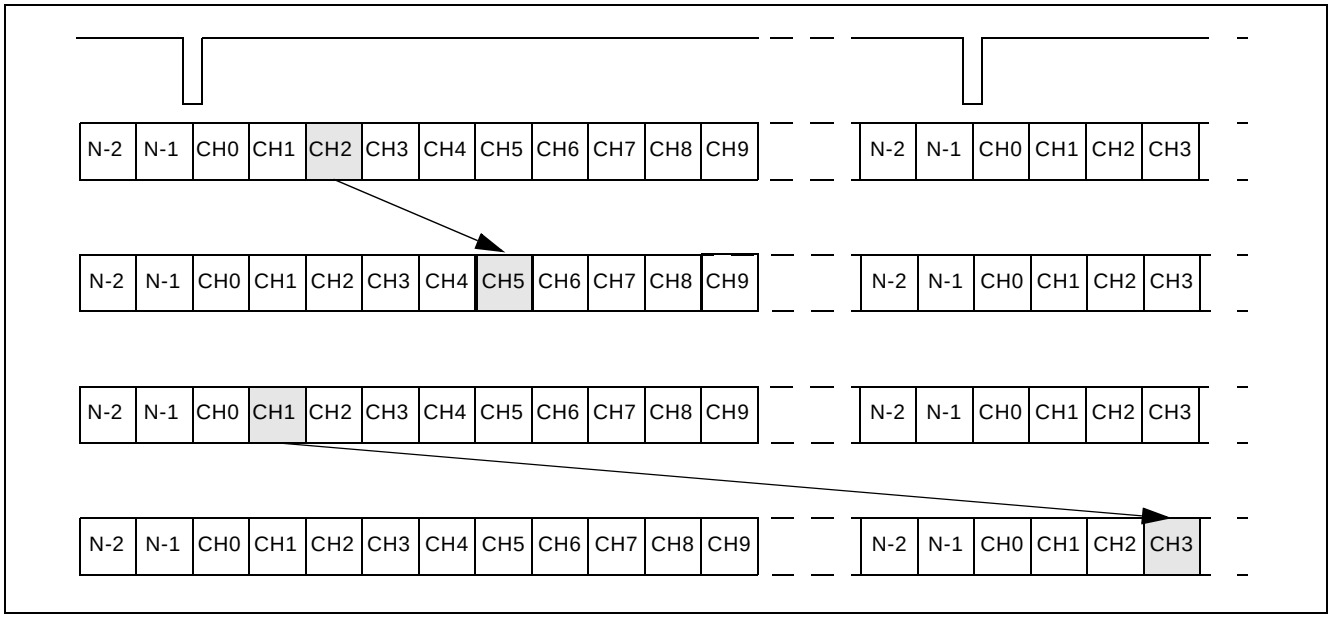


Figure 7 - Data Throughput Delay for Variable Delay

8.0 Per-Channel A-Law/μ-Law Translation

The ZL50075 provides per channel code translation to be used to adapt pulse code modulation (PCM) voice or data traffic between networks which use different encoding laws. Code translation is available in both Connection Mode and Message Mode.

In order to use this feature the Connection Memory Bits must be set. The $\overline{V}$/D (bit 28) defines if the traffic in the channel is voice or data. Setting the ICL1 - 0 (bits 27 - 26) programs the input coding law and the OCL1 - 0 (bits 25 - 24) programs the output coding law as shown in Table 4.

The different code options are shown in Table 4:

Input Coding (ICL1- 0)	Output Coding (OCL1 - 0)	Voice Coding ($\overline{V}$/D bit = 0)	Data Coding ($\overline{V}$/D bit = 1)
00	00	ITU-T G.711 A-Law	No code
01	01	ITU-T G.711 μ-Law	Alternate Bit Inversion (ABI)
10	10	A-Law without Alternate Bit Inversion (ABI)	Inverted Alternate Bit Inversion (ABI)
11	11	μ-Law without Magnitude Inversion (MI)	All bits inverted

Table 4 - Input and Output Voice and Data Coding

For voice coding options, the ITU-T G.711 A-Law and ITU-T G.711 μ-Law are the standard rules for encoding. The A-Law without Alternate Bit Inversion (ABI) is an alternative code that does not invert the even bits (6, 4, 2, 0). The μ-Law without Magnitude Inversion (MI) is an alternative code that does not perform Inversion of magnitude bits (6, 5, 4, 3, 2, 1, 0).

When performing data code options, no code does not invert the bits. The Alternate Bit Inversion (ABI) option inverts the even bits (6, 4, 2, 0) while the Inverted Alternate Bit Inversion (ABI) inverts the odd bits (7, 5, 3, 1). When all bits inverted is selected, all of the bits (7, 6, 5, 4, 3, 2, 1, 0) are inverted.

The input channel and output channel encoding law are configured independently. If the output channel coding is set to be different to the input channel, the ZL50075 performs translation between the two standards. If the input and output encoding laws are set to the same standard, no translation occurs.

9.0 Bit Error Rate Tester

The ZL50075 has one Bit Error Rate (BER) transmitter and one BER receiver for each pair of input and output streams, resulting in 64 transmitters connected to the output streams and 64 receivers associated with the input streams. Each transmitter can generate a BER sequence with a pattern of 2^{15}-1 Pseudo-Random Code (ITU O.151). Each transmitter can start at any location on the stream and will last for a minimum of 1 channel to a maximum of 1 frame time (125 μs). The BER transmitters are enabled by programming the Pseudo-random Bit Sequence (bit 31 - 29) to 101 in the Connection Memory Bits.

Multiple Connection Memory locations can be programmed for BER tests. These locations are not required to be consecutive. However, when read back, the BER locations must be received in the same order that they were transmitted. If the BER locations are not received in the same order, the BER test will produce errors.

The PRBS bit pattern is sequentially loaded into the output timeslots as shown in the following example, see Figure 8.

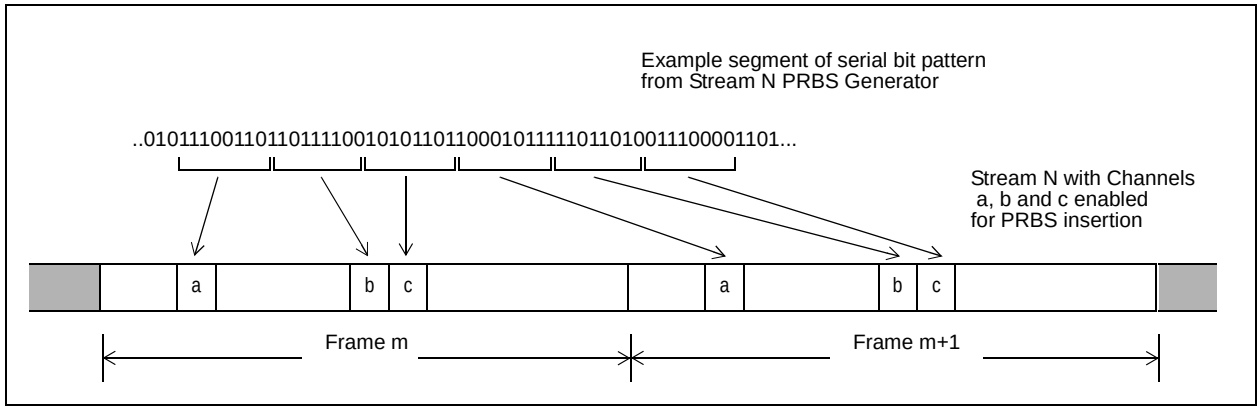


Figure 8 - Example PRBS Timeslot Insertion

Each PRBS detector can be configured to monitor for bit errors in one or more timeslots. The selection of timeslots is configured by the Input BER Enable Control Memory (IBERECM), see Section 17.1, for programming details, Each detector has an associated 16 bit error counter which is accessible via the microprocessor interface, see Section 17.2. The value of the counter represents the total number of errors detected on the corresponding input stream. Bit errors are accumulated until the counter is either reset by the microprocessor, or the counter reaches its maximum value, 65,535 (decimal). If more than 65,535 errors are detected, the counter will hold at the maximum value until reset.

Any number of timeslots may be configured for bit error rate testing; however the user must ensure the following for correct operation of the BER test function:

1. The number of timeslots enabled for PRBS detection on the input stream must equal the number of timeslots enabled for PRBS generation on the source output stream
2. The arrival order of timeslots at the PRBS detector must be the same as the order in which timeslots were transmitted by the PRBS generator. For example, in Figure 8 above, the timeslot order a,b,c must be maintained through the external path from source TDM output stream to destination TDM input stream.

10.0 Microprocessor Port

The ZL50075 has a generic 16-bit microprocessor port, used to provide access to the internal Data Memory (read access only), Connection Memory and the Control Registers. D15 on the bus maps to Bit 31 and Bit 15 of the internal 32 bit memory or register, D14 maps to Bit 30 and Bit 14, etc.

The IM pin is used to select between Motorola bus control and Intel bus control. If the IM input is low, then a Motorola control is selected. If the IM bit is high, then an Intel control is selected. Regardless of which bus configuration is selected, the bus cycle termination signals $\overline{\text{WAIT}}$ & $\overline{\text{DTA}}$ are both provided.

The byte enable signals, SIZ0-1, control which byte(s) on the 16-bit data bus are written to the internal memory, see Table 5.

Pin Name	Motorola Mode MC68000, MC68302 Equivalent Function IM = 0	Intel Mode i960 Equivalent Function IM = 1	Data Bus Bytes Enabled
SIZ1	$\overline{\text{UDS}}$	$\overline{\text{BE1}}$	D15-8
SIZ0	$\overline{\text{LDS}}$	$\overline{\text{BE0}}$	D7-0

Table 5 - Byte Enable Signals

The address bus, A18 - 1, provides byte addressing to the memory space. A0, is not used, and must be connected to defined logic level. Address bit A1 and the Data Transfer Size inputs, SIZ1 - 0, identify which bytes are being accessed.

In both Intel and Motorola modes, the A1 address input is used to identify the word alignment in internal memory as shown in Table 6.

A1	Memory Data Word Alignment
0	Bits 31:16
1	Bits 15:0

Table 6 - Memory Data Word Alignment

Data bus word alignments are shown in Table 7. An example of byte addressing is given in Table 8.

Microprocessor 16 bit Data Bus	SIZ1	SIZ0	A1	Internal 32-bit Memory or Register
D15 - 8	0	1	0	Bits 31:24
	0	1	1	Bits 15:8
D7 - 0	1	0	0	Bits 23:16
	1	0	1	Bits 7:0
D15 - 0	0	0	0	Bits 31:16
	0	0	1	Bits 15:0
	1	1	X[1]	No access

Table 7 - Data Bus Word Alignment

1. X - Don't Care

Address (Hex)	Register Description	Register Byte	A18 - 0 (binary)	SIZ1	SIZ0	Comments
40200 or 40201	Stream Control Register (Group 0)	Bits 23:16	100 0000 0010 0000 000X†	1	0	8 bit transfer
40282 or 40283	Input Clock Control Register	Bits 15:8	100 0000 0010 1000 001X†	0	1	8 bit transfer
40286 or 40287	Output Clock Control Register	Bits 15:0	100 0000 0010 1000 011X†	0	0	16 bit transfer
40284 or 40285	Output Clock Control Register	Bits 31:16	100 0000 0010 1000 010X†	0	0	16 bit transfer

Table 8 - Byte Address Examples

† - Don't Care. A0 is not used.

10.1 Bus Operation

10.1.1 Read Cycle

The operation of a read cycle is illustrated in Figure 9.

- The microprocessor asserts the R/$\overline{W}$ control signal high, to signal a read cycle. It also drives the address A, transfer size, SIZ1 - 0, and chip select logic drives the $\overline{CS}$ signal active low to select the ZL50075
- The microprocessor then drives the $\overline{DS}$ signal active low, to signal the start of the bus cycle. The $\overline{DS}$ signal is held low for the duration of the bus cycle
- $\overline{WAIT}$ is asserted active low
- The ZL50075 accesses the requested memory or register location(s), and places the requested data onto the data bus, D15 - 0. All data bus pins are driven, whether or not they are being used for the specific data transfer. Unused pins will present unknown data. If the address is to an unused area of the memory space, unknown data is presented on the data bus
- The ZL50075 then de-asserts $\overline{WAIT}$, and asserts either $\overline{DTA}$ or $\overline{BERR}$, depending on the validity of the data transfer
- When the microprocessor observes the active low state of the $\overline{DTA}$ or the $\overline{BERR}$ signal, it terminates the bus cycle by driving the $\overline{DS}$ pin inactive high
- When the ZL50075 sees the $\overline{DS}$ signal go inactive high, it removes the assertions on the $\overline{DTA}$ or $\overline{BERR}$ signals by driving them inactive high
- When the ZL50075 sees the $\overline{CS}$ signal go inactive high, it tri-states the data bus, D15 - 0 and the $\overline{DTA}$ and $\overline{BERR}$ signals. However, if $\overline{CS}$ goes inactive high before $\overline{DS}$ goes inactive high, the $\overline{DTA}$ and $\overline{BERR}$ signals are driven inactive high before they are tri-stated
- In Intel mode, $\overline{DTA}$ is always driven to signal the end of a bus cycle, regardless of $\overline{BERR}$

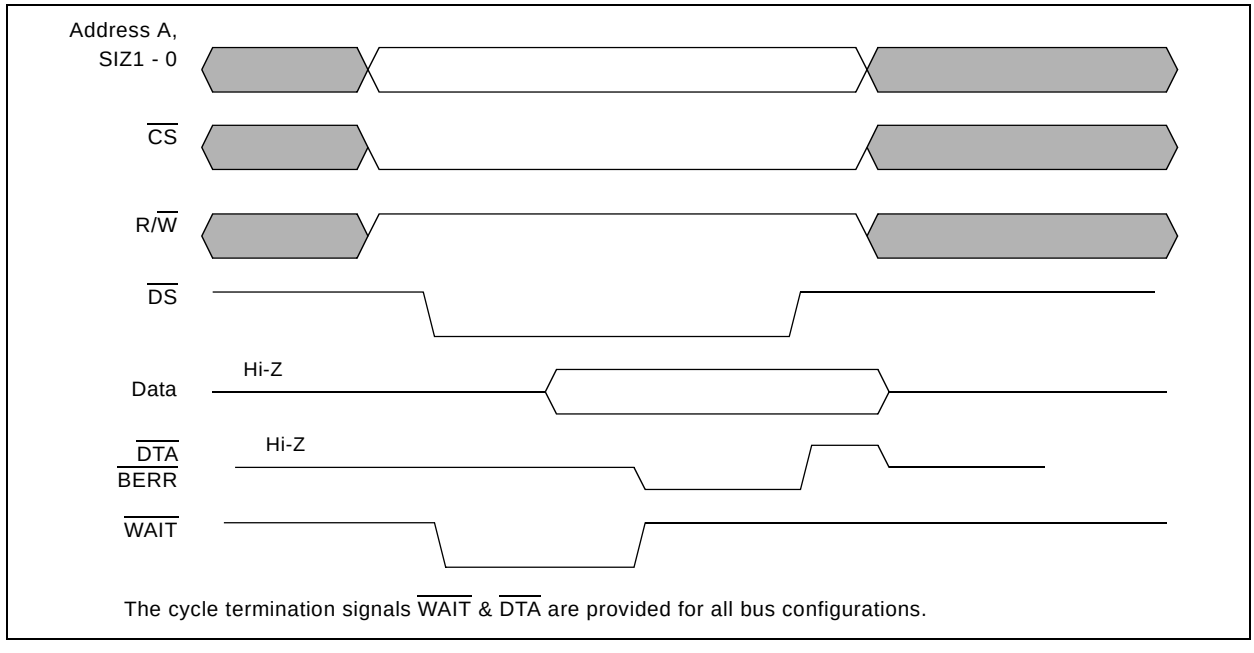


Figure 9 - Read Cycle Operation

10.1.2 Write Cycle

The operation of the write cycle is illustrated in Figure 10.

- The microprocessor asserts the R/$\overline{W}$ control signal low, to signal a write cycle. It also drives the address A, data transfer size, SIZ1 - 0, and chip select logic drives the $\overline{CS}$ signal active low to select the ZL50075
- The microprocessor then drives the data bus, D15 - 0 with the data to be written, and then drives the $\overline{DS}$ signal active low, to signal the start of the bus cycle. The $\overline{DS}$ signal is held low for the duration of the bus cycle
- $\overline{WAIT}$ is asserted active low
- The ZL50075 transfers the data presented on the data bus pins into the indicated memory or register location(s). If the address is to an unused area of the memory space, or to the data memory, no data is transferred. The microprocessor port cannot write to the Data Memory
- The ZL50075 then de-asserts $\overline{WAIT}$, and asserts either $\overline{DTA}$ or $\overline{BERR}$, depending on the validity of the data transfer
- When the microprocessor observes the active low state of the $\overline{DTA}$ or the $\overline{BERR}$ signal, it terminates the bus cycle by driving the $\overline{DS}$ pin inactive high
- When the ZL50075 sees the $\overline{DS}$ signal go inactive high, it removes the assertions on the $\overline{DTA}$ or $\overline{BERR}$ signals by driving them inactive high
- When the ZL50075 sees the $\overline{CS}$ signal go inactive high, it tri-states the $\overline{DTA}$ and $\overline{BERR}$ signals. However, if $\overline{CS}$ goes inactive high before $\overline{DS}$ goes inactive high, the $\overline{DTA}$ and $\overline{BERR}$ signals are driven inactive high before they are tri-stated
- In Intel mode, $\overline{DTA}$ is always driven to signal the end of a bus cycle, regardless of $\overline{BERR}$

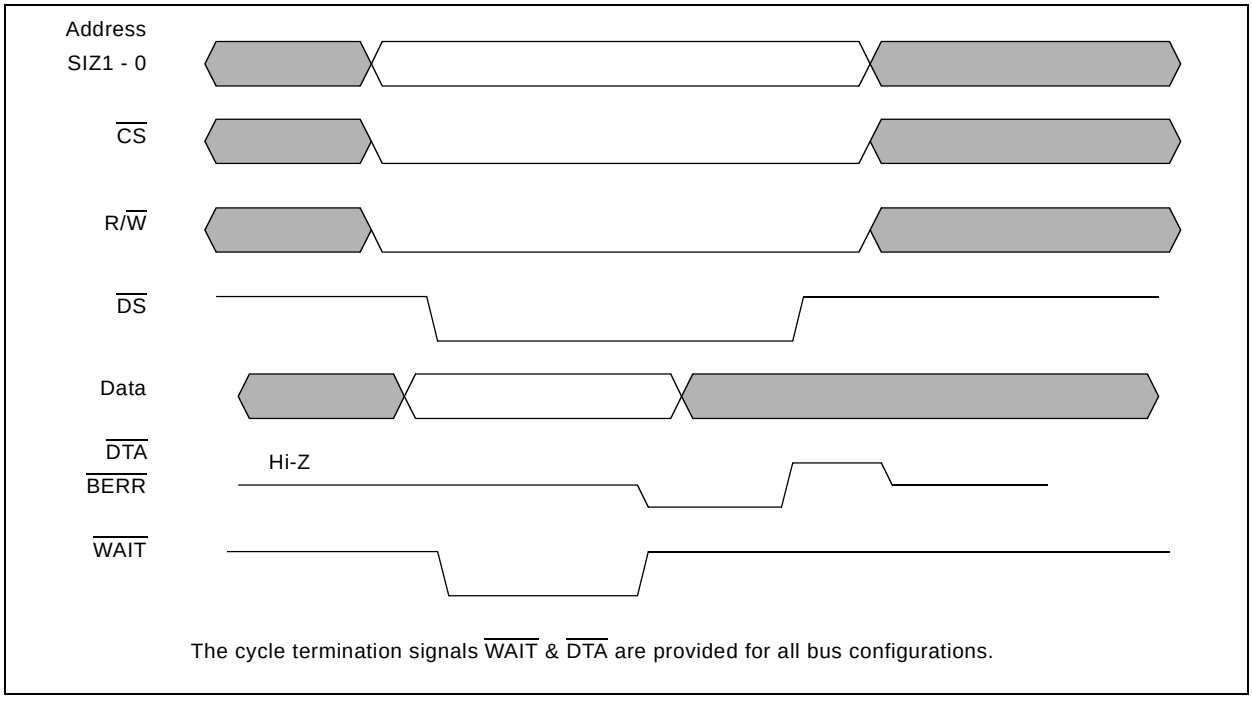


Figure 10 - Write Cycle Operation

11.0 Power-up and Initialization of the ZL50075

11.1 Device Reset and Initialization

The $\overline{\text{PWR}}$ pin is used to reset the ZL50075. When this pin is low, the following functions are performed:

- Asynchronously puts the microprocessor port in a reset state
- Tristates all of the output streams (SToA0 - 31, SToB0 - 31)
- Preloads all of the registers with their default values (refer to the individual registers for default values)
- Clears all internal counters

11.2 Power Supply Sequencing

The ZL50075 has two separate power supplies: V_{DD_IO} (3.3 V) and V_{DD_CORE} (1.8 V). The recommended power-up sequence is for V_{DD_IO} to be applied first, followed by the V_{DD_CORE} supply. V_{DD_CORE} should not lead V_{DD_IO} supply by more than 0.3 V. Both supplies may be powered-down simultaneously.

11.3 Initialization

Upon power up, the ZL50075 should be initialized as follows:

- Assert $\overline{\text{PWR}}$ to low immediately after power is applied
- Set the $\overline{\text{TRST}}$ pin low to disable the JTAG TAP controller
- Deassert the $\overline{\text{PWR}}$ pin.
- Apply the Master Clock Input ($\overline{\text{CKi}}$0) and Master Frame Pulse Input ($\overline{\text{FPi}}$0) to the values defined by the CK_SEL1 - 0 pins
- Set the ODE pin low to disable the output streams

Note: After the $\overline{\text{PWR}}$ reset is removed, and on the application of a suitable master clock input, it takes approximately 1ms for the internal initialization to complete

- Automatic block initialization of the Connection Memory to all zeros occurs, without microprocessor intervention
- All Group Control Registers are preset to 000C000C hex, corresponding to rates of 65 Mbps, no link inversions, no fractional output bit advancements, internal clock source, and no input sample point delays
- The Input Clock Control Register is preset to 0DB hex, corresponding to:
  - All clock inputs set to negative logic sense
  - All frame pulse inputs set to negative logic sense
  - All input frame pulses set to ST-BUS timing
- The Output Clock Control Register is pre-set to 060D1C3C hex, corresponding to:
  - All clock outputs set to negative logic sense
  - All frame pulse outputs set to negative logic sense
  - All output frame pulses set to ST-BUS timing
  - All output clock source selections to internal
  - Clock outputs, $\overline{\text{CKo}}$0 - 1 are preset to rates of 65 MHz and 32 MHz, respectively

Note: If the master clock input, $\overline{\text{CKi}}$0, is not available, the microprocessor port will assert $\overline{\text{BERR}}$ on all accesses and read cycles.

12.0 IEEE 1149.1 Test Access Port

The JTAG test port is implemented to meet the mandatory requirements of the IEEE 1149.1 (JTAG) standard. The operation of the boundary-scan circuity is controlled by an external Test Access Port (TAP) Controller.

The ZL50075 uses the public instructions defined in IEEE 1149.1, with the provision of a 16-bit Instruction Register, and three scannable Test Data Registers: Boundary Scan Register, Bypass Register and Device Identification Register.

12.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50075 test functions. The interface consists of 4 input and 1 output signal. as follows:

- **Test Clock (TCK)** - TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Select (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to V_{DD_IO} when it is not driven from an external source.
- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to V_{DD_IO} when it is not driven from an external source.
- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDo. The data out of the TDo is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDo driver is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)** - Resets the JTAG scan structure. This pin is internally pulled to V_{DD_IO} when it is not driven from an external source. When JTAG is not in use, this pin must be tied low for normal operation.

The TAP signals are only applied when the ZL50075 is required to be in test mode. When in normal, non-test mode, $\overline{\text{TRST}}$ must be connected low to disable the test logic. The remaining test pins may be left unconnected.

12.2 Instruction Register

The ZL50075 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG interface contains a 4 bit instruction register. Instructions are serially loaded into the instruction register from the TDi when the TAP controller is in its shifted-OR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDi and TDo during register scanning.

12.3 Test Data Register

As specified in the IEEE 1149.1 standard, the ZL50075 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50075 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDi to TDo.
- T**he Device Identification Register** - The JTAG device ID for the ZL50075 is $C39B14B_H$

Version	<31:28>	0000
Part Number	<27:12>	1100 0011 1001 1011
Manufacturer ID	<11:1>	0001 0100 101
LSB	<0>	1

12.4 Boundary Scan Description Language (BSDL)

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149.1 test interface.

13.0 Memory Map of ZL50075

The memory map for the ZL50075 is given in Table 9.

Address (Hex)	Description
00000 - 1FFFF	Connection Memory
20000 - 27FFF	Connection Memory LSB
28000 - 2FFFF	Data Memory: Read only; Bus error on write ($\overline{\text{BERR}}$)
30000 - 37FFF	Input BER Enable Control Memory
38000 - 3FFFF	Invalid Address. Access causes Bus error ($\overline{\text{BERR}}$)
40000 - 400FF	BER Counters
40100 - 401FF	Data Memory: Read only; Bus error on write ($\overline{\text{BERR}}$)
40200 - 4027F	Group Control Registers
40280 - 40283	Input Clock Control Register
40284 - 40287	Output Clock Control Register
40288 - 4028B	Block Init Register
4028C - 4028F	Block Init Enable
40290- 7FFFF	Invalid Address. Access causes Bus error ($\overline{\text{BERR}}$)

Table 9 - Memory Map

14.0 Connection Memory

Address range 00000 - 1FFFF hex.

On power-up, all Connection Memory locations are initialized automatically to 00000000 hex, using the Block Initialization feature, see Section 18.3 and Section 18.4.

The 32 bit Connection Memory has 32,768 locations. Each 32 bit long-word is used to program the desired source data and any other per-channel characteristics of one output time-slot.

The memory map for the Connection Memory is sub-divided into 32 blocks, each corresponding to one of the possible 32 output stream group numbers. The address ranges for these blocks are illustrated in Table 10.

Output Group	Start Address (Hex)	Address Range (Hex)	Output Group	Start Address (Hex)	Address Range (Hex)
0	000000	000000 - 000FFF	16	010000	010000 - 010FFF
1	001000	001000 - 001FFF	17	011000	011000 - 011FFF
2	002000	002000 - 002FFF	18	012000	012000 - 012FFF
3	003000	003000 - 003FFF	19	013000	013000 - 013FFF
4	004000	004000 - 004FFF	20	014000	014000 - 014FFF
5	005000	005000 - 005FFF	21	015000	015000 - 015FFF
6	006000	006000 - 006FFF	22	016000	016000 - 016FFF
7	007000	007000 - 007FFF	23	017000	017000 - 017FFF
8	008000	008000 - 008FFF	24	018000	018000 - 018FFF
9	009000	009000 - 009FFF	25	019000	019000 - 019FFF
10	00A000	00A000 - 00AFFF	26	01A000	01A000 - 01AFFF
11	00B000	00B000 - 00BFFF	27	01B000	01B000 - 01BFFF
12	00C000	00C000 - 00CFFF	28	01C000	01C000 - 01CFFF
13	00D000	00D000 - 00DFFF	29	01D000	01D000 - 01DFFF
14	00E000	00E000 - 00EFFF	30	01E000	01E000 - 01EFFF
15	00F000	00F000 - 00FFFF	31	01F000	01F000 - 01FFFF

Table 10 - Connection Memory Stream Control Mapping

The control of each output stream group, SToA*n* and SToB*n*, depends on the programmed bit rate. The address offset range for each group is illustrated in Table 11.

Output Group Data Rate	Timeslot Range	Output Stream	Stream Address Offset Range (Hex)
65 Mbps	0 - 1023	SToA*n*	00000 - 00FFF
		SToB*n*	N/A
32 Mbps	0 - 511	SToA*n*	00000 - 007FF
		SToB*n*	00800 - 00FFF
16 Mbps	0 - 255	SToA*n*	00000 - 003FF
		SToB*n*	00400 - 007FF
	N/A	$\overline{\text{BERR}}$	00800 - 00FFF
8 Mbps	0 - 127	SToA*n*	00000 - 001FF
		SToB*n*	00200 - 003FF
	N/A	$\overline{\text{BERR}}$	00400 - 00FFF

Table 11 - Output Control at Various Output Rates

The address range for a particular stream is given by adding the group start address, as indicated in Table 11, to the appropriate stream offset range, as indicated in Table 12. For example, the Connection Memory address range for SToB12 operating at 32 Mbps, is 00C800-00CFFF.

Control of each channel timeslot within each stream, offset timeslot number, timeslot address offset, range of 4 addresses is shown in the table below.

Timeslot		Address Offset hex
SToA*n*	**SToB*n***	
0	0	000
1	1	004
2	2	008
-	-	-
510	510	7F8
511	511	7FC
512		800
513		804
-		-
1021		FF4
1022		FF8
1023		FFC

Table 12 - Stream Offset Range

14.1 Connection Memory Bit Functions

The bit functions of the connection memory are illustrated in Table 13.

External Read/Write Address: 000000_H
Reset Value: 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCF 2	PCF 1	PCF 0	$\overline{V}$/D	ICL 1	ICL 0	OCL 1	OCL 0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	GR 4	GR 3	GR 2	GR 1	GR 0	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1 ST1	CH 0 ST0

Bit	Name	Description
31 - 29	PCF2 - 0	**Per Channel Function** PCF2 - 0 / Function / Description 000 / OT / Output is tri-stated 001 / FH / Output drives high always 010 / MSG / Output is in message mode 011 / VAR / Connection is in variable delay mode 100 / CD / Connection is in constant delay mode 101 / PRBS / PRBS Generator 110 / OT / Output is tri-stated 111 / OT / Output is tri-stated
28	$\overline{V}$/D	**Voice/Data Control** When this bit is low, the corresponding channel is for voice. When this bit is high, the corresponding channel is for data.
27 - 26	ICL1 - 0	**Input Coding Law** ICL1 - 0 / Input Coding Law: For Voice ($\overline{V}$/D bit = 0) / For Data ($\overline{V}$/D bit = 1) 00 / CCITT.ITU A-Law / No Code 01 / CCITT.ITU μ-Law / ABI 10 / A-Law w/o ABI / Inverted ABI 11 / μ-Law w/o Mag. Inv / All Bits Inverted

Table 13 - Connection Memory Bits (CMB)

External Read/Write Address: 000000_H
Reset Value: 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCF 2	PCF 1	PCF 0	$\overline{V}$/D	ICL 1	ICL 0	OCL 1	OCL 0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	GR 4	GR 3	GR 2	GR 1	GR 0	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1 ST1	CH 0 ST0

Bit	Name	Description
25 - 24	OCL1 - 0	**Output Coding Law** OCL1 - 0 / Output Coding Law: For Voice ($\overline{V}$/D bit = 0) / For Data ($\overline{V}$/D bit = 1) 00 / CCITT.ITU A-Law / No Code 01 / CCITT.ITU μ-Law / ABI 10 / A-Law w/o ABI / Inverted ABI 11 / μ-Law w/o Mag. Inv / All Bits Inverted
23 - 15	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
14 - 10	GR4 - 0	**Group Selection.** These bits define the input/source serial group number (31 - 0).
9 - 0	CH9 - 0	**Channel Selection.** These bits define the input/source channel number, depending on the data rate. For 65.536 Mbps bits 9 - 0 are used to access the 1024 channels. For 32.768 Mbps bits 9 - 1 are used to access the 512 channels. Bit 0 is used to select stream ‘A’ (0) or stream ‘B’ (1). For 16.869 Mbps bits 9 - 2 are used to access the 256 channels. Bit 1 MUST be set to 0. Bit 0 is used to select stream ‘A’ (0) or stream ‘B’ (1). For 8.192 Mbps bits 9 - 3 are used to access the 128 channels. Bit 2 - 1 MUST be set to 0. Bits 0 is used to select stream ‘A’ (0) or stream ‘B’ (1).

Table 13 - Connection Memory Bits (CMB) (continued)

15.0 Connection Memory LSB

The Connection Memory Least Significant Byte field is provided to give a convenient alternative way to modify the output data for a stream in message mode. In this memory address range, all of the connection memory least significant bytes (bits 7 - 0) are available for read/write in consecutive address locations. This feature is provided for programming convenience. It can allow higher programming bandwidth on message mode streams. For example, one longword access to this memory space can read or set the message bytes in four consecutive connection memory locations. Access to this memory space is big-endian, with the most significant bytes on the data bus accessing the lower address of the connection memory. Addressing into each of the streams is illustrated in Table 14.

Output Group	Start Address (Hex)	Address Range (Hex)	Output Group	Start Address (Hex)	Address Range (Hex)
0	020000	020000 - 0203FF	16	024000	024000 - 0243FF
1	020400	020400 - 0207FF	17	024400	024400 - 0247FF
2	020800	020800 - 020BFF	18	024800	024800 - 024BFF
3	020C00	020C00 - 020FFF	19	024C00	024C00 - 024FFF
4	021000	021000 - 0213FF	20	025000	025000 - 0253FF
5	021400	021400 - 0217FF	21	025400	025400 - 0257FF
6	021800	021800 - 021BFF	22	025800	025800 - 025BFF
7	021C00	021C00 - 021FFF	23	025C00	025C00 - 025FFF
8	022000	022000 - 0223FF	24	026000	026000 - 0263FF
9	022400	022400 - 0227FF	25	026400	026400 - 0267FF
10	022800	022800 - 022BFF	26	026800	026800 - 026BFF
11	022C00	022C00 - 022FFF	27	026C00	026C00 - 026FFF
12	023000	023000 - 0233FF	28	027000	027000 - 0273FF
13	023400	023400 - 0237FF	29	027400	027400 - 0277FF
14	023800	023800 - 023BFF	30	027800	027800 - 027BFF
15	023C00	023C00 - 023FFF	31	027C00	027C00 - 027FFF

Table 14 - Connection Memory LSB Stream Control Mapping

Output Group Data Rate	Timeslot Range	Output Stream	Stream Address Offset Range (Hex)
65 Mbps	0 - 1023	STo*An*	00000 - 003FF
		STo*Bn*	N/A
32 Mbps	0 - 511	STo*An*	00000 - 001FF
		STo*Bn*	00200 - 003FF
16 Mbps	0 - 255	STo*An*	00000 - 000FF
		STo*Bn*	00100 - 001FF
	N/A	$\overline{\text{BERR}}$	00200 - 003FF
8 Mbps	0 - 127	STo*An*	00000 - 0007F
		STo*Bn*	00080 - 000FF
	N/A	$\overline{\text{BERR}}$	00100 - 003FF

Table 15 - Connection Memory LSB Output Group Control

Within each stream group, the control of each of the actual output groups depends on the output rate programmed into the Group Control Registers. The address offsets to these control areas for each of the four output groups are illustrated in Table 15.

16.0 Data Memory

The data memory field is a read only address range used to monitor the data being received by the input streams. Addressing into each of the streams is illustrated in Table 16.

Input Group	Start Address (Hex)	Address Range (Hex)	Input Group	Start Address (Hex)	Address Range (Hex)
0	028000	028000 - 0283FF	16	02C000	02C000 - 02C3FF
1	028400	028400 - 0287FF	17	02C400	02C400 - 02C7FF
2	028800	028800 - 028BFF	18	02C800	02C800 - 02CBFF
3	028C00	028C00 - 028FFF	19	02CC00	02CC00 - 02CFFF
4	029000	029000 - 0293FF	20	02D000	02D000 - 02D3FF
5	029400	029400 - 0297FF	21	02D400	02D400 - 02D7FF
6	029800	029800 - 029BFF	22	02D800	02D800 - 02DBFF
7	029C00	029C00 - 029FFF	23	02DC00	02DC00 - 02DFFF
8	02A000	02A000 - 02A3FF	24	02E000	02E000 - 02E3FF
9	02A400	02A400 - 02A7FF	25	02E400	02E400 - 02E7FF
10	02A800	02A800 - 02ABFF	26	02E800	02E800 - 02EBFF
11	02AC00	02AC00 - 02AFFF	27	02EC00	02EC00 - 02EFFF
12	02B000	02B000 - 02B3FF	28	02F000	02F000 - 02F3FF
13	02B400	02B400 - 02B7FF	29	02F400	02F400 - 02F7FF
14	02B800	02B800 - 02BBFF	30	02F800	02F800 - 02FBFF
15	02BC00	02BC00 - 02BFFF	31	02FC00	02FC00 - 02FFFF

Table 16 - Data Memory Stream Control Mapping

Within each stream group, the mapping of each of the actual input streams, STiA and STiB, depends on the input rate programmed into the Group Control Registers. The address offsets to these data areas for each of the input groups is illustrated in Table 17.

Input Group Data Rate	Time-slot Range	Input Streams	Address Offset Range (Hex)
65 Mbps	0 - 1023	STiA*n*	00000 - 003FF
		STiB*n*	N/A
32 Mbps	0 - 511	STiA*n*	00000 - 001FF
		STiB*n*	00200 - 003FF
16 Mbps	0 - 255	STiA*n*	00000 - 000FF
		STiB*n*	00100 - 001FF
	N/A	$\overline{\text{BERR}}$	00200 - 003FF
8 Mbps	0 - 127	STiA*n*	00000 - 0007F
		STiB*n*	00080 - 000FF
	N/A	$\overline{\text{BERR}}$	00100 - 003FF

Table 17 - Data Memory Stream Access

The address ranges for the data memory portion corresponding to each of the actual input groups, STiA and STiB, for any particular input stream number is calculated by adding the Start Address for the particular stream, as indicated in Table 16, to the appropriate Address Offset Range, as indicated in Table 17. The time-slots map linearly into the appropriate address offset range. (i.e. timeslots 0, 1, 2, ... map into addresses 00000, 00001, 00002, ...)

The entire data memory is a read only structure. Any write attempts will result in a bus error. **$\overline{\text{BERR}}$** is driven active low to terminate the bus cycle.

17.0 BER Control Memory and Error Counters

17.1 Input BER Enable Control Memory

The BER Enable Control Memory (IBERECM) is a read/write memory block. Each memory location is used to control the BER counter of one incoming timeslot. Addressing into each of the streams is illustrated in Table 18.

Input Group	Start Address (Hex)	Address Range (Hex)	Input Group	Start Address (Hex)	Address Range (Hex)
0	030000	030000 - 0303FF	16	034000	034000 - 0343FF
1	030400	030400 - 0307FF	17	034400	034400 - 0347FF
2	030800	030800 - 030BFF	18	034800	034800 - 034BFF
3	030C00	030C00 - 030FFF	19	034C00	034C00 - 034FFF
4	031000	031000 - 0313FF	20	035000	035000 - 0353FF
5	031400	031400 - 0317FF	21	035400	035400 - 0357FF
6	031800	031800 - 031BFF	22	035800	035800 - 035BFF
7	031C00	031C00 - 031FFF	23	035C00	035C00 - 035FFF

Table 18 - BER Stream Control Mapping

Input Group	Start Address (Hex)	Address Range (Hex)	Input Group	Start Address (Hex)	Address Range (Hex)
8	032000	032000 - 0323FF	24	036000	036000 - 0363FF
9	032400	032400 - 0327FF	25	036400	036400 - 0367FF
10	032800	032800 - 032BFF	26	036800	036800 - 036BFF
11	032C00	032C00 - 032FFF	27	036C00	036C00 - 036FFF
12	033000	033000 - 0333FF	28	037000	037000 - 0373FF
13	033400	033400 - 0337FF	29	037400	037400 - 0377FF
14	033800	033800 - 033BFF	30	037800	037800 - 037BFF
15	033C00	033C00 - 033FFF	31	037C00	037C00 - 037FFF

Table 18 - BER Stream Control Mapping (continued)

Each byte location of the BER Enable Memory contains one read/write BER counter enable (BCE) bit, mapped into the D0 location. If the BCE bit is set, then the BER counter for the corresponding stream and timeslot is enabled for the duration of that timeslot. If the BCE bit is cleared the counter is disabled.

Input Group Data Rate	Time-slot Range	Output Streams	Address Offset Range (Hex)
65 Mbps	0 - 1023	SToA*n*	00000 - 003FF
		SToB*n*	N/A
32 Mbps	0 - 511	SToA*n*	00000 - 001FF
		SToB*n*	00200 - 003FF
16 Mbps	0 - 255	SToA*n*	00000 - 000FF
		SToB*n*	00100 - 001FF
	N/A	$\overline{\text{BERR}}$	00200 - 003FF
8 Mbps	0 - 127	SToA*n*	00000 - 0007F
		SToB*n*	00080 - 000FF
	N/A	$\overline{\text{BERR}}$	00100 - 003FF

Table 19 - BER Enable Memory Group Access

17.2 BER Counters

There are a total of 64 Bit Error Counters, corresponding to the 64 serial input streams. Each count value is 32 bits wide, but only the least significant 16 bits are used. The most significant 16 bits of the bit error counters will always read back zero. A write operation to any byte of the counter, including the 16 most significant bits, will clear that counter.

Each bit error counter contains the number of single bit errors detected on the corresponding stream, since the counter was last cleared. If the number of bit errors detected exceeds 65535 (decimal), the counter will hold that value until it is cleared.

BER Stream	Start Address (Hex)	Address Range (Hex)
0	040000	040000 - 040003
1	040004	040004 - 040007
2	040008	040008 - 04000B
3	04000C	04000C - 04000F
. .	. .	. .
60	0400F0	0400F0 - 0400F3
61	0400F4	0400F4 - 0400F7
62	0400F8	0400F8 - 0400FB
63	0400FC	0400FC - 0400FF

Table 20 - BER Enable Memory Stream Access

18.0 Group Control Registers

The ZL50075 addresses the issues of a simple programming model and automatic stream configuration, by defining a basic switching bit rate of 65.536 Mbps, and by grouping the I/O streams depending on the rate they are programmed.

The Group Control Registers are provided for setting the operating characteristics of the TDM input and output streams. All of the Group Control Registers are mapped long-word aligned on 32 bit boundaries in the memory space. Each of the 32 registers is used to control one stream. The mapping of the Group Control Registers to the I/O stream numbers is illustrated in Table 21. The bit functions of each of the Group Control Registers are illustrated in Table 22.

TDM Group	Group Control Register Address (Hex)
0	40200 - 40203
1	40204 - 40207
2	40208 - 4020B
3	4020C - 4020F
: :	: :
29	40274 - 40277
30	40278 - 4027B
31	4027C - 4027F

Table 21 - Group Control Register Addressing

External Read/Write Address: 40200_H - $4027F_H$
Reset Value: $000C000C_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	OSI	OSBA 1	OSBA 0	OSBR 1	OSBR 0	OSSCR 1	OSSCR 0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	ISI	ISPD 4	ISPD 3	ISPD 2	ISPD1	ISPD0	ISBR 1	ISBR 0	ISSRC 1	ISSRC 0

Bit	Name	Description
31 - 23	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
22	OSI	**Output Stream Inversion.** For normal operation, this bit is set low. To invert the output stream, set this bit high.
21 - 20	OSBA1 - 0	**Output Stream Bit Advancement** OSBA1 - 0 / Non-65 Mbps / 65 Mbps 00 / 0ns / 0 ns 01 / 7.6ns / 3.8 ns 10 / 15.2ns / 7.6 ns 11 / 22.8ns / 11.4 ns
19 - 18	OSBR1 - 0	**Output Stream Bit Rate** OSBR1 - 0 / Bit Rates Per Group (STo A / STo B) 00 / 8.192 Mbps / 8.192 Mbps 01 / 16.384 Mbps / 16.384 Mbps 10 / 32.768 Mbps / 32.768 Mbps 11 / 65.536 Mbps / Not Used Unused streams are tri-stated.
17 - 16	OSSRC1 - 0	**Output Stream Clock Source Select** OSSRC1 - 0 / Output Timing Source 00 / Internal System Clock 01 / $\overline{CKi}0$ and $\overline{FPi}0$ 10 / $\overline{CKi}1$ and $\overline{FPi}1$ 11 / $\overline{CKi}2$ and $\overline{FPi}2$
15 - 10	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
9	ISI	**Input Stream Inversion** For normal operation, this bit is set low. To invert the output stream, set this bit high.

Table 22 - Group Control Register

External Read/Write Address: 40200_H - $4027F_H$
Reset Value: $000C000C_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	OSI	OSBA 1	OSBA 0	OSBR 1	OSBR 0	OSSCR 1	OSSCR 0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	ISI	ISPD 4	ISPD 3	ISPD 2	ISPD1	ISPD0	ISBR 1	ISBR 0	ISSRC 1	ISSRC 0

Bit	Name	Description
8 - 4	ISPD4 - 0	**Input Sampling Point Delay** Default Sampling Point is 3/4. Adjust according to Figure 4 on page 15.
3 - 2	ISBR1 - 0	**Input Stream Bit Rate** ISBR1 - 0 / Bit Rates Per Group: STiA / STiB 00: 8.192 Mbps / 8.192 Mbps 01: 16.384 Mbps / 16.384 Mbps 10: 32.768 Mbps / 32.768 Mbps 11: 65.536 Mbps / Not Used Unused streams must be connected to ground.
1 - 0	ISSRC1 - 0	**Input Stream Clock Source Select** 00: Internal System Clock 01: $\overline{CKi}0$ and $\overline{FPi}0$ 10: $\overline{CKi}1$ and $\overline{FPi}1$ 11: $\overline{CKi}2$ and $\overline{FPi}2$

Table 22 - Group Control Register (continued)

The Group Control Register is a static control register. Changes to bit settings may disrupt data flow on the selected port for a maximum of 2 frames.

18.1 Input Clock Control Register

The Input Clock Control Register is used to select the logic sense of the input clock.

External Read/Write Address: 40280_H
Reset Value: $0DB_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	GCISEL0	FPIPOL0	CKIPOL0

Bit	Name	Description
31 - 3	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
2	GCISEL0	**GCI-Bus Selection** When this bit is low, $\overline{FPi0}$ is set for ST-BUS mode. When this bit is high, $\overline{FPi0}$ is set for GCI-Bus mode.
1	FPIPOL2	**Frame Pulse Polarity Selection** When this bit is low, $\overline{FPi0}$ is set for the positive clock edge. When this bit is high, $\overline{FPi0}$ is set for negative.
0	CKIPOL2	**Clock Polarity Selection** When this bit is low, $\overline{CKi0}$ is set for the positive clock edge. When this bit is high, $\overline{CKi0}$ is set for negative.

Table 23 - Input Clock Control Register

18.2 Output Clock Control Register

The Output Clock Control Register is used to select the desired source, frequency, and logic sense of the output clocks. The bit functions of the Output Clock Control Register are illustrated in Table 24.

External Read/Write Address: 40284_H
Reset Value: $060D1C3C_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	GCOSEL1	FPOPOL1	CKOPOL1	CKO1RATE1	CKO1RATE0	CKO1SRC1	CKO1SRC0	GCOSEL0	FPOPOL0	CKOPOL0	CKO0RATE1	CKO0RATE0	CKO0SRC1	CKO0SRC0

Bit	Name	Description
31 - 28	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
27 - 14	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to 01100000110100.

Table 24 - Output Clock Control Register

External Read/Write Address: 40284_H
Reset Value: $060D1C3C_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	GCOSEL1	FPOPOL1	CKOPOL1	CKO1RATE1	CKO1RATE0	CKO1SRC1	CKO1SRC0	GCOSEL0	FPOPOL0	CKOPOL0	CKO0RATE1	CKO0RATE0	CKO0SRC1	CKO0SRC0

Bit	Name	Description
13	GCOSEL 1	**GCI-Bus Selection** When this bit is low, $\overline{FPo1}$ is set for ST-BUS mode. When this bit is high, $\overline{FPo1}$ is set for GCI-Bus mode.
12	FPOPOL 1	**Frame Pulse Polarity Selection** When this bit is low, $\overline{FPo1}$ is set for the positive clock edge. When this bit is high, $\overline{FPo1}$ is set for the negative clock edge.
11	CKOPOL 1	**Clock Polarity Selection** When this bit is low, $\overline{CKo1}$ is set for the positive clock edge. When this bit is high, $\overline{CKo1}$ is set for the negative clock edge.
10 - 9	CKO1RATE1 - 0	**Output Clock Rate for $\overline{CKo1}$ and $\overline{FPo1}$** The output clock rate can not exceed the selected input clock rate. All rates are available when the internal system clock is selected. CKO1RATE1 - 0 / $\overline{CKo1}$ / $\overline{FPo1}$ 00 / 8.192 MHz / 120 ns 01 / 16.384 MHz / 60 ns 10 / 32.768 MHz / 30 ns 11 / 65.536 MHz / 15 ns
8 - 7	CKO1SRC1 - 0	**Output Clock Source for $\overline{CKo1}$ and $\overline{FPo1}$** CKO1SRC1 - 0 / Output Timing Source 00 / Internal System Clock 01 / $\overline{CKi0}$ and $\overline{FPi0}$ 10 / $\overline{CKi1}$ and $\overline{FPi1}$ 11 / $\overline{CKi2}$ and $\overline{FPi2}$
6	GCOSEL 0	**GCI-Bus Selection** When this bit is low, $\overline{FPo0}$ is set for ST-BUS mode. When this bit is high, $\overline{FPo0}$ is set for GCI-Bus mode.
5	FPOPOL 0	**Frame Pulse Polarity Selection** When this bit is low, $\overline{FPo0}$ is set for the positive clock edge. When this bit is high, $\overline{FPo0}$ is set for the negative clock edge.

Table 24 - Output Clock Control Register (continued)

External Read/Write Address: 40284_H
Reset Value: $060D1C3C_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	GCOSEL1	FPOPOL1	CKOPOL1	CKO1RATE1	CKO1RATE0	CKO1SRC1	CKO1SRC0	GCOSEL0	FPOPOL0	CKOPOL0	CKO0RATE1	CKO0RATE0	CKO0SRC1	CKO0SRC0

Bit	Name	Description
4	CKOPOL0	**Clock Polarity Selection** When this bit is low, $\overline{CKo0}$ is set for the positive clock edge. When this bit is high, $\overline{CKo0}$ is set for the negative clock edge.
3 - 2	CKO0RATE1 - 0	**Output Clock Rate for $\overline{CKo0}$ and $\overline{FPo0}$**
1 - 0	CKO0SRC1 - 0	**Output Clock Source for $\overline{CKo0}$ and $\overline{FPo0}$**

CKO0RATE1 - 0	$\overline{CKo0}$	$\overline{FPo0}$
00	8.192 MHz	120ns
01	16.384 MHz	60ns
10	32.768 MHz	30ns
11	65.536 MHz	15ns

CKO0SRC1 - 0	Output Timing Source
00	Internal System Clock
01	$\overline{CKi0}$ and $\overline{FPi0}$
10	$\overline{CKi1}$ and $\overline{FPi1}$
11	$\overline{CKi2}$ and $\overline{FPi2}$

Table 24 - Output Clock Control Register (continued)

18.3 Block Init Register

The Block Init Register is a 32 bit read/write register at address 040288 - $04028B_H$.

The Block Init Register is used during block initialization of the connection memory. A block initialization automatically occurs at power-up. However, it is possible to perform a block initialization at any time. During Block Initialization, the value of the Block Init Register is copied to all connection memory locations in an operation that runs in about 120µs. If the Block Init Register is modified during a block initialization, the new value used is ignored.

18.4 Block Init Enable Register

The Block Init Enable Register is a 32 bit read/write register at address 04028C - $04028F_H$.

The Block Init Enable Register is used to initiate a block initialization of the connection memory. A block initialization automatically occurs at power-up. Since the Block Init Register is cleared at power-up this automatic block initialization will write all zeros to all Connection Memory Bits. However, it is possible to perform a block initialization at any time. To begin a block initialization, the hex value 31415926 must be written to the Block Init Enable Register. If a block initialization is signaled while one is in progress, the signal is ignored, and the currently active block initialization is allowed to complete.

The value read back from the Block Init Enable Register is different than the value written. It represents both the block initialization status, and the power-up reset initialization status. The meaning of the initialization status bits is illustrated in Table 25. The bits 31 - 2 always read back 0.

Bit	Name	Description
0	Block Init Status	0 if Block initialization is completed; 1 if Block initialization is in progress
1	Reset Init Status	0 if Reset initialization is completed 1 if Reset initialization is in progress

Table 25 - Block and Power-up Initialization Status Bits

Any access to the connection memory or the data memory during a block initialization or a reset initialization will result in a bus error, $\overline{BERR}$. All TDM outputs are tri-stated during any block initialization.

Absolute Maximum Ratings[1] - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ[2]	Max	Unit
1	Chip I/O Supply Voltage	V_{DD_IO}	-0.5		5.0	V
2	Chip Core Supply Voltage	V_{DD_CORE}	-0.5		5.0	V
3	Input Voltage (non-5 V tolerant inputs)	V_{I_3V}	-0.5		V_{DD_IO} + 0.5	V
4	Input Voltage (5 V tolerant inputs)	V_{I_5V}	-0.5		7.0	V
5	Continuous Current at digital outputs	I_o			15	mA
6	Package power dissipation	P_D			2.1	W
7	Storage temperature	T_S	- 55		+125	°C

Note 1: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Note 2: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ[1]	Max	Unit
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply Core	V_{DD_CORE}	1.71	1.8	1.89	V
3	Positive Supply I/O	V_{DD_IO}	3.0	3.3	3.6	V
4	Input Voltage (non-5 V tolerant inputs)	V_{I_3V}	0		V_{DD_IO}	V
5	Input Voltage (5 V tolerant inputs)	V_{I_5V}	0		5.5	

Note 1: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Typ[1]	Max	Unit	Test Conditions
1	Core Supply Current[2]	I_{DD_CORE}			500	mA	
2	I/O Supply Current	I_{DD_IO}			62	mA	Outputs Unloaded
3	Leakage Current	I_{DDQ}		105		uA	
4	Dynamic Power Dissipation	P_{DD}			1.2	W	Outputs Unloaded
5	Input High Voltage	V_{IH}	2.0			V	
6	Input Low Voltage	V_{IL}			0.8	V	
7	Input Leakage-input pins[3]	I_{IL}			5	µA	$0 \leq < V_I \leq V_{DD\_IO}$
8	Input Leakage-bidirectional pins	I_{BL}			5	uA	$0 \leq < V_I \leq V_{DD\_IO}$
9	Pull-up Current	I_{PU}		-33		µA	Input at 0V
10	Pull-down Current	I_{PD}		33		µA	Input at V_{DD_IO}
11	Input Pin Capacitance	C_I		3		pF	
12	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 8mA
13	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8mA

Note 1: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 2: StoA = 65 Mbps with random patterns. CKo0 = 65 MHz, CKo1 = 32 MHz.

Note 3: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (Vin).

AC Electrical Characteristics[1] - Timing Parameter Measurement Voltage Levels - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Level	Unit	Test Conditions
1	CMOS Threshold	V_{CT}	0.5 V_{DD_IO}	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	0.7 V_{DD_IO}	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	0.3 V_{DD_IO}	V	

1. Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics[1] - $\overline{\text{FPi}}$ and $\overline{\text{CKi}}$ Timing

No.	Characteristic (Figure 11)	Sym	Min	Typ[2]	Max	Units	Notes
1	$\overline{\text{FPi}}$ Input Frame Pulse Setup Time	t_{FPIS}	3			ns	
2	$\overline{\text{FPi}}$ Input Frame Pulse Hold Time	t_{FPIH}	2			ns	
3	$\overline{\text{CKi}}$ Input Clock Period (average value, does not consider the effects of jitter)	t_{CKIP}	15	15.26	15.5	ns	65.536 MHz
			30	30.5	31	ns	32.768 MHz
			60	61	62	ns	16.384 MHz
			120	122	124	ns	8.192 MHz
4	$\overline{\text{CKi}}$ Input Clock High Time	t_{CKIH}	4			ns	
5	$\overline{\text{CKi}}$ Input Clock Low Time	t_{CKIL}	4			ns	
6	$\overline{\text{CKi}}$ Input Clock Rise/Fall Time	t_{rCKI}, t_{fCKI}	0		6	ns	
7	$\overline{\text{CKi}}$ Input Clock Cycle to Cycle Variation	t_{CVC}			2	ns p-p	Standard rating[3]. STi at 65 Mbps
					4	ns p-p	Standard rating[3]. STi at 32 Mbps
					10	ns p-p	Standard rating[3]. STi at 16 Mbps
					20	ns p-p	Standard rating[3]. STi at 8 Mbps
					20% of t_{CKIP}	p-p	Extended rating. With alternate clock source[4] or high $\overline{\text{CKi0}}$ rate[5]

Note 1: Characteristics are over recommended operating conditions unless otherwise stated.

Note 2: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 3: When using internal APLL clock source and the $\overline{\text{CKi0}}$ frequency is less than or equal to the data rate.

Note 4: When using input clock source $\overline{\text{CKi}}$2-0 instead of the internal APLL clock source.

Note 5: When using internal APLL clock source and the $\overline{\text{CKi0}}$ frequency is higher than or equal to twice the data rate.

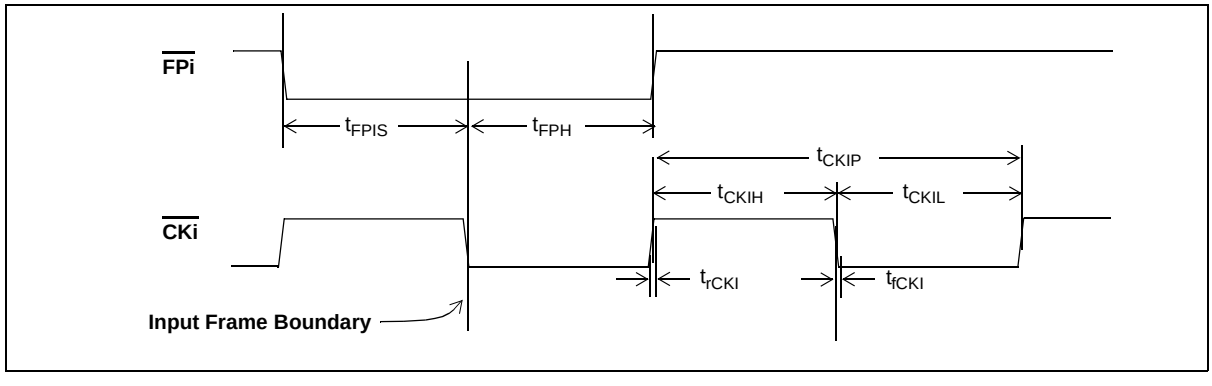


Figure 11 - Frame Pulse Input and Clock Input

AC Electrical Characteristics[1] - $\overline{\text{FPi}}$ and $\overline{\text{CKi}}$ Skew

No.	Characteristic (Figure 12)	Sym	Min	Typ[2]	Max	Units	Notes
1	$\overline{\text{CKi0}}$ to $\overline{\text{CKi1}}$, $\overline{2}$ Skew	t_{CKSK}	-30		+30	ns	C_L 50 pF Assume no jitter on input clocks

Note 1: Characteristics are over recommended operating conditions unless otherwise stated.

Note 2: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

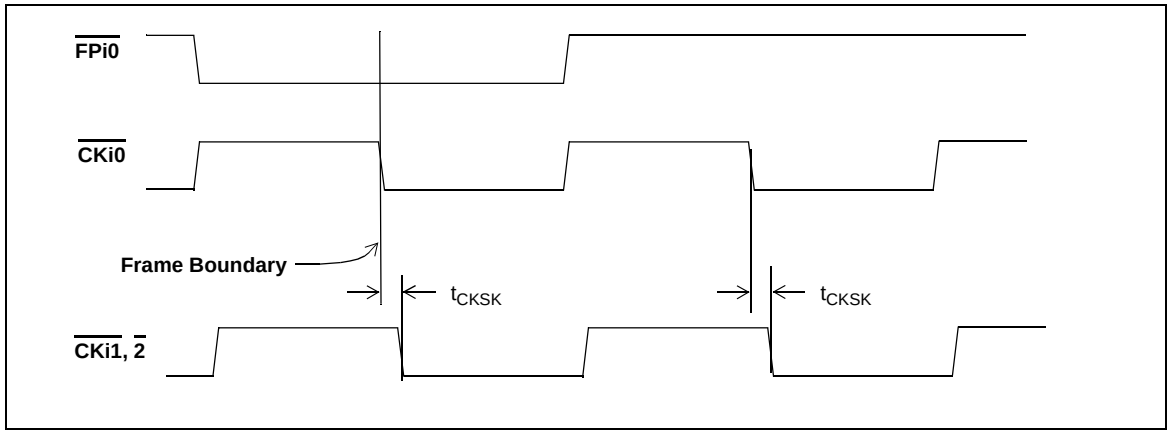


Figure 12 - Frame Skew Timing Diagram

AC Electrical Characteristics[1] - Serial Data Timing[2] to $\overline{CKi}$

No.	Characteristic (Figure 13)	Sym	Min	Typ[3]	Max	Units	Notes[4]
1	$\overline{CKi}$ to $\overline{CKo}$ Propagation Delay	t_{CKD}	3		12	ns	$\overline{CKo}$ clock source = $\overline{CKi}$
			3		12	ns	$\overline{CKo}$ Clock source = Internal 131 MHz APLL output
2	STi to posedge $\overline{CKi}$ setup	t_{SIPS}	0			ns	
3	STi to posedge $\overline{CKi}$ hold	t_{SIPH}	7.5			ns	
4	STi to negedge $\overline{CKi}$ setup	t_{SINS}	0			ns	
5	STi to negedge $\overline{CKi}$ hold	t_{SINH}	7.5			ns	
6	Posedge $\overline{CKi}$ to Output Data Valid	t_{SIPV}	3		12.5	ns	STo A[5]
			3		13	ns	STo B[5]
7	Negedge $\overline{CKi}$ to Output Data Valid	t_{SINV}	3		14	ns	STo A[5]
			3		16	ns	STo B[5]
8	Posedge $\overline{CKi}$ to Output Data tri-state	t_{SIPZ}			14	ns	STo A[5]
					15	ns	STo B[5]
9	Negedge $\overline{CKi}$ to Output Data tri-state	t_{SINZ}			14	ns	STo A[5]
					15	ns	STo B[5]
10	ODE to Output Data tri-state	t_{SOZ}			10	ns	STo A C_L = 30 pF, R_L = 1K[5]
					11	ns	STo B C_L = 30 pF, R_L = 1K[5]
11	ODE to Output Data Enable	t_{SOE}	4.5		15	ns	STo A[5]
			6		20	ns	STo B[5]

Note 1: Characteristics are over recommended operating conditions unless other wise stated.

Note 2: Data Capture points vary with respect to $\overline{CKi}$ edge depending on clock rates & fractional delay settings.

Note 3: All of these specifications refer to ST-BUS inputs and outputs with clock source set to $\overline{CKi}$.

Note 4: Loads on all serial outputs set to 30 pF.

Note 5: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

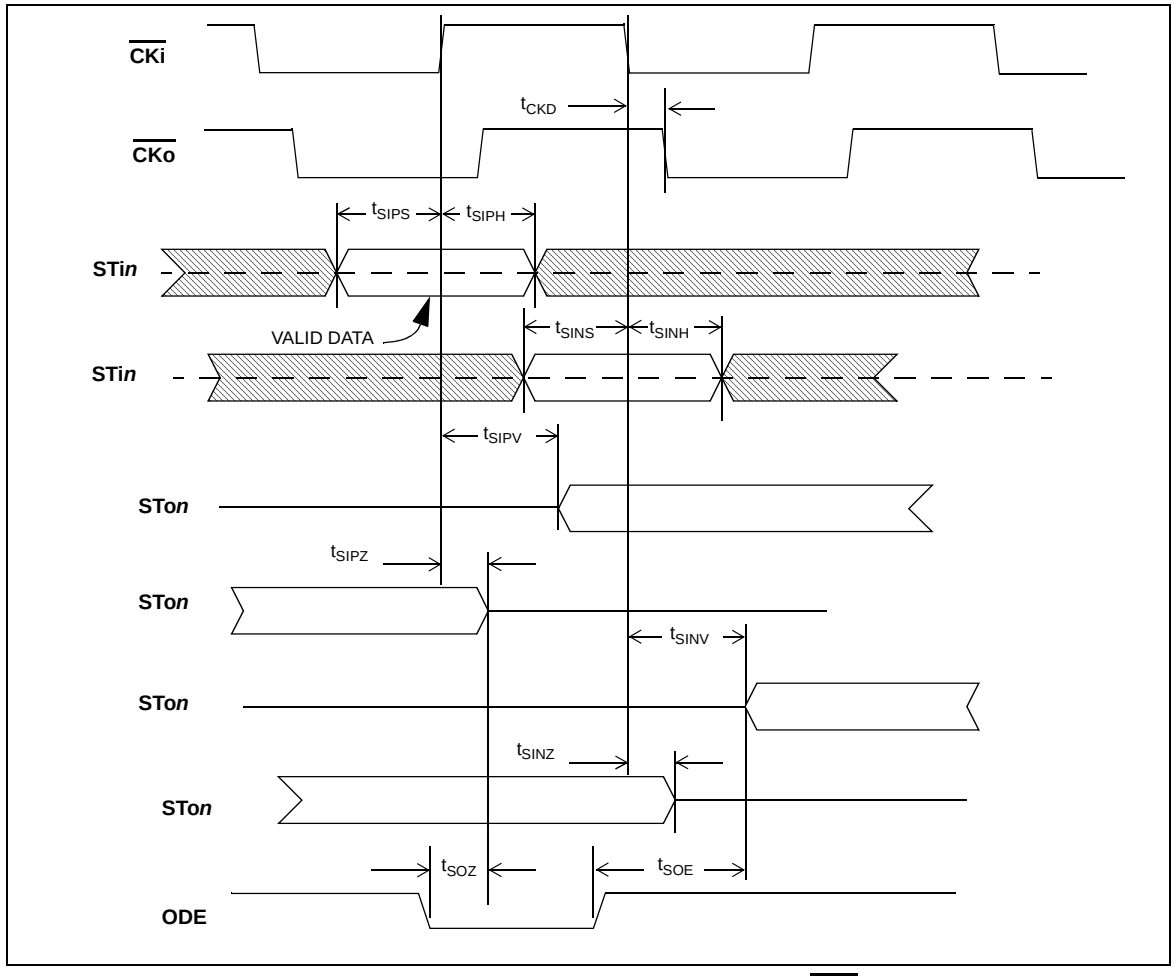


Figure 13 - Serial Data Timing to $\overline{CKi}$

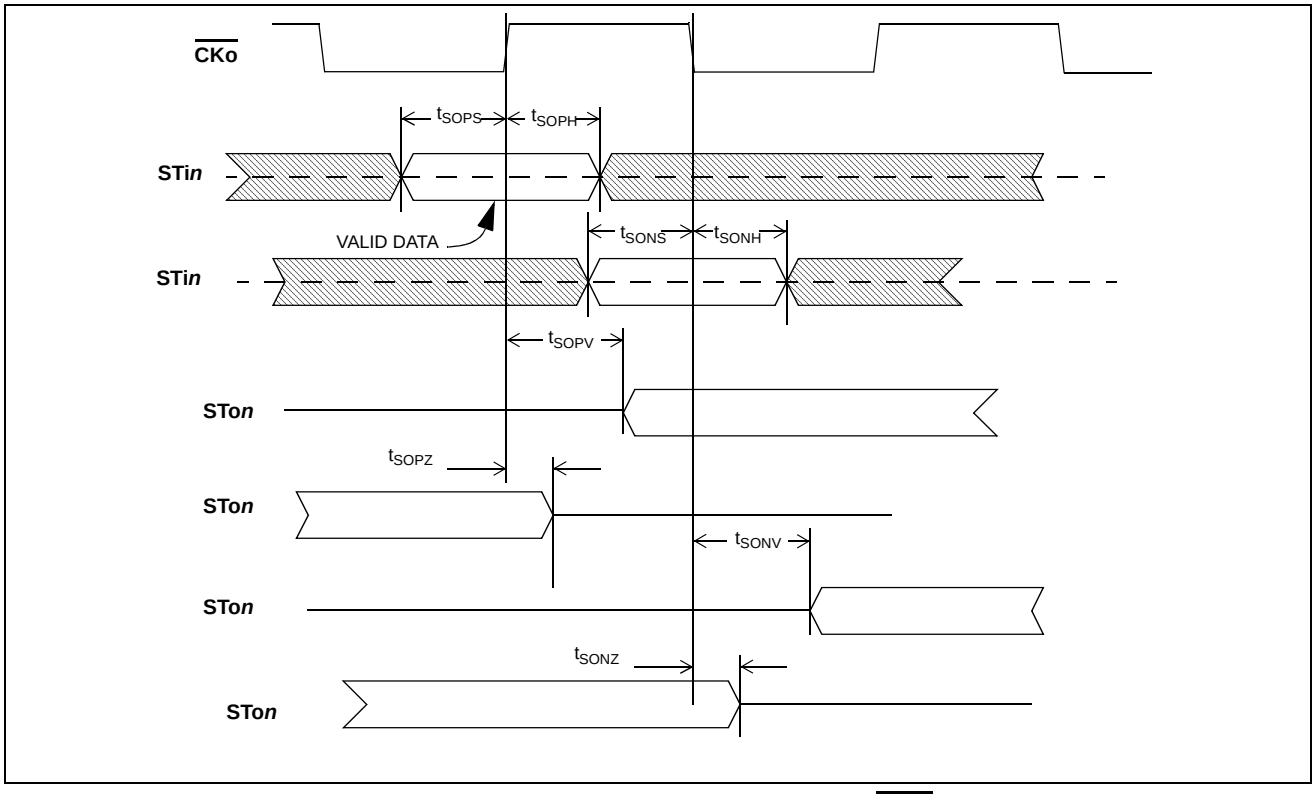


Figure 14 - Serial Data Timing to $\overline{\text{CKo}}$

AC Electrical Characteristics - Serial Data Timing[1] to $\overline{\text{CKo}}$[2]

No.	Characteristic (Figure 14)	Sym	Min	Typ[3]	Max	Units	Notes[4]
1	STi to posedge $\overline{\text{CKo}}$ setup	t_{SOPS}	7.5			ns	
2	STi to posedge $\overline{\text{CKo}}$ hold	t_{SOPH}	0			ns	
3	STi to negedge $\overline{\text{CKo}}$ setup	t_{SONS}	7.5			ns	
4	STi to negedge $\overline{\text{CKo}}$ hold	t_{SONH}	0			ns	
5	Posedge $\overline{\text{CKo}}$ to Output Data Valid	t_{SOPV}	1		5	ns	STo A[4]
			1		5	ns	STo B[4]
6	Negedge $\overline{\text{CKo}}$ to Output Data Valid	t_{SONV}	1		5	ns	STo A[4]
			1		5	ns	STo B[4]
7	Posedge $\overline{\text{CKo}}$ to Output Data tri-state	t_{SOPZ}			9	ns	STo A[4]
					11	ns	STo B[4]
8	Negedge $\overline{\text{CKo}}$ to Output Data tri-state	t_{SONZ}			9	ns	STo A[4]
					11	ns	STo B[4]

Note 1: Data Capture points vary with respect to $\overline{\text{CKo}}$ edge depending on clock rates & fractional delay settings.

Note 2: $\overline{\text{CKo}}$ output set to internal clock source.

Note 3: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

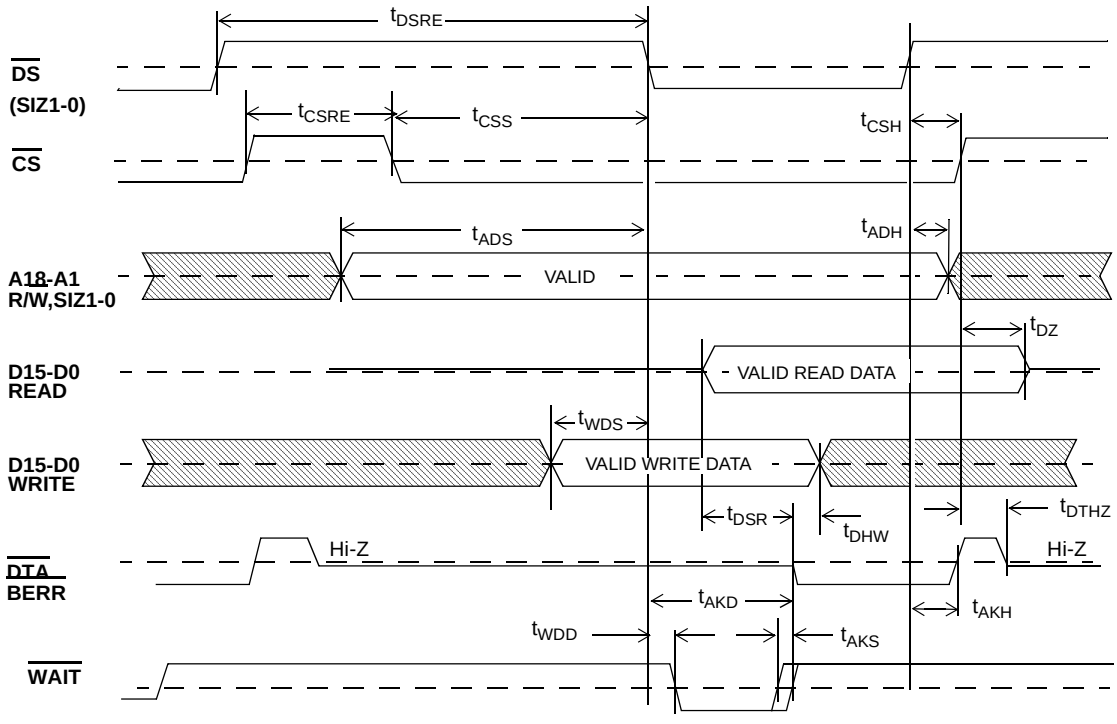
Note 4: Loads on all serial outputs set to 30 pF.

AC Electrical Characteristics - Microprocessor Bus Interface

No	Characteristics (Figure 15, & Figure 16)	Sym	Min	Typ[1]	Max	Units	Notes
1	$\overline{DS}$ Recovery	t_{DSRE}	5			ns	
2	$\overline{CS}$ Recovery	t_{CSRE}	0			ns	
3	$\overline{CS}$ asserted setup to $\overline{DS}$ asserted	t_{CSS}	0			ns	
4	Address, SIZ1-0, R/$\overline{W}$ setup to $\overline{DS}$ asserted	t_{ADS}	0			ns	
5	$\overline{CS}$ hold from $\overline{DS}$ deasserted	t_{CSH}	0			ns	
6	Address, SIZ0-1, R/$\overline{W}$ hold from $\overline{DS}$ deasserted	t_{ADH}	0			ns	
7	Data valid to $\overline{DTA}$ asserted on read	t_{DSR}	0			ns	C_L = 50 pF, R_L = 1k[2]
8	$\overline{CS}$ deasserted to Data tri-stated on read	t_{DZ}			5	ns	C_L = 50 pF, R_L = 1k[2]
9	Data setup to $\overline{DS}$ asserted on write	t_{WDS}	0			ns	
10	Data hold from $\overline{DTA}$ asserted on write	t_{DHW}	0			ns	
11	$\overline{DS}$ asserted to $\overline{WAIT}$ Asserted	t_{WDD}			9	ns	C_L = 50 pF, R_L = 1k[2]
12	$\overline{WAIT}$ deasserted to $\overline{DTA}$/$\overline{BERR}$ asserted skew	t_{AKS}			10	ns	C_L = 50 pF, R_L = 1k[2]
13	$\overline{DS}$ asserted to $\overline{DTA}$ Asserted	t_{AKD}	35		155	ns	Connection Memory
			50		75	ns	All other registers
14	$\overline{DS}$ deasserted to $\overline{DTA}$ Deasserted	t_{AKH}			7	ns	C_L = 30 pF, R_L = 1K[2]
15	$\overline{CS}$ deasserted to $\overline{DTA}$ tri-stated	t_{DTHZ}			13	ns	C_L = 30 pF, R_L = 1K[2]
16	$\overline{BE}$ or $\overline{UDS}$/$\overline{LDS}$ skew	t_{DSK}			20	ns	
17	$\overline{BE}$ or $\overline{UDS}$/$\overline{LDS}$ to $\overline{DS}$ set-up	t_{BEDS}	0				

Note 1: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 2: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.



Note: Motorola MC68000 and Intel i960 or similar processors are depicted in this diagram.

Figure 15 - Microprocessor Bus Interface Timing

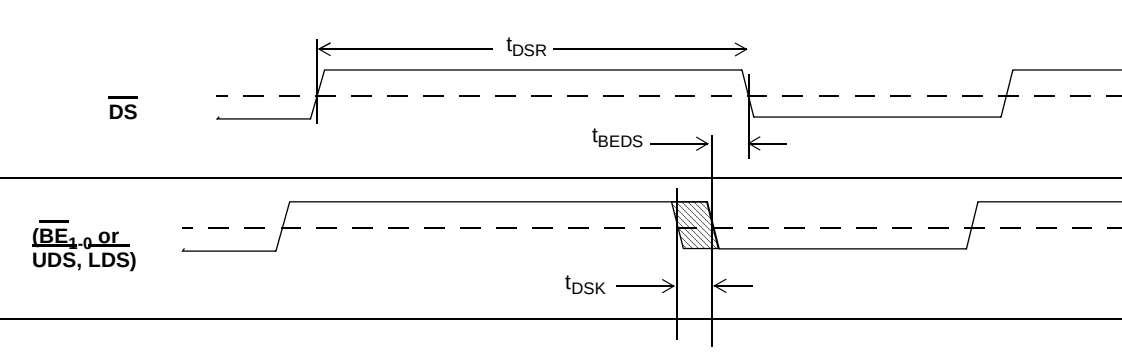


Figure 16 - Intel Mode Timing

AC Electrical Characteristics[1] - IEEE 1149.1 Test Port and $\overline{\text{PWR}}$ Pin Timing

No.	Characteristic (Figure 17)	Sym	Min	Typ[2]	Max	Units	Notes
1	TCK Clock Period	t_{TCKP}	100			ns	
2	TCK Clock Frequency	t_{TCKF}			10	MHz	
3	TCK Clock Pulse Width High	t_{TCKH}	20			ns	
4	TCK Clock Pulse Width Low	t_{TCKL}	20			ns	
5	TMS Set-up Time	t_{TMSS}	10			ns	
6	TMS Hold Time	t_{TMSH}	10			ns	
7	TDi Input Set-up Time	t_{TDIS}	20			ns	
8	TDi Input Hold Time	t_{TDIH}	60			ns	
9	TDo Output Delay	t_{TDOD}			20	ns	C_L = 30 pF
10	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	20			ns	
11	$\overline{\text{PWR}}$ pulse width	t_{TPWR}	20			ns	

Note 1: Characteristics are over recommended operating conditions unless otherwise stated.

Note 2: Typical figures are at 25°C, V_{DD_CORE} at 1.8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

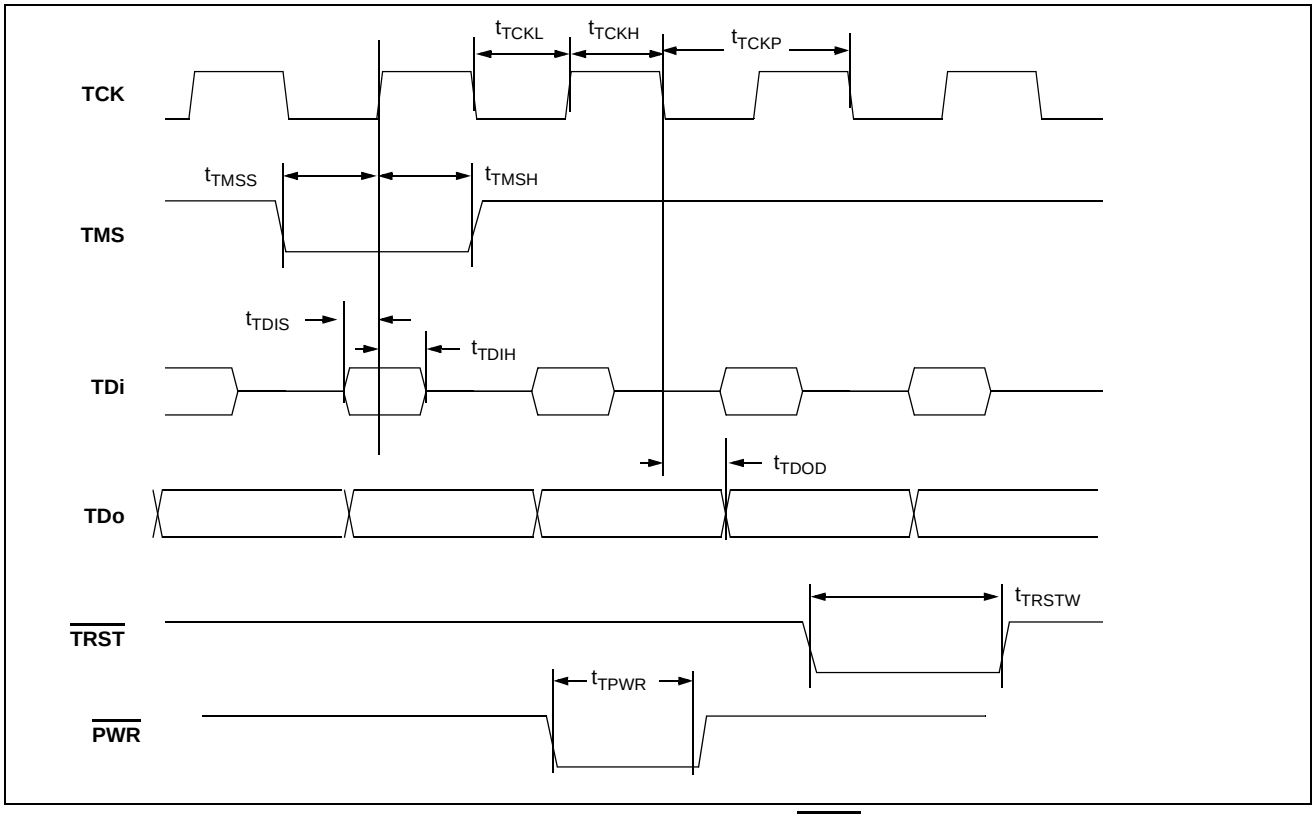
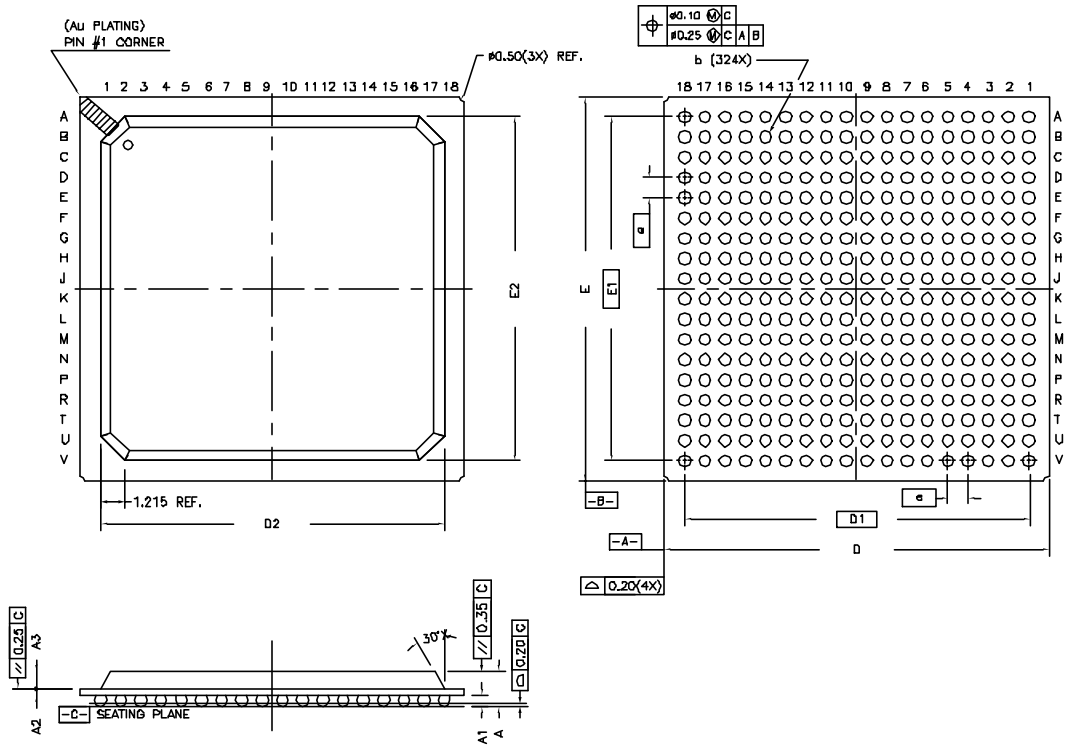


Figure 17 - IEEE 1149.1 Test Port & $\overline{\text{PWR}}$ Reset Timing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.71	1.90
A1	0.40	0.50	0.60
A2		0.36 REF.	
A3		0.85 Ref.	
b	0.50	0.60	0.70
D	18.80	19.00	19.20
D1		17.00 Ref.	
D2	16.80	17.00	17.20
E	18.80	19.00	19.20
E1		17.00 Ref.	
E2	16.80	17.00	17.20
e		1.00 Ref.	

Confirms to JEDEC MS-034
AAG-1 iss. A

NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. NOT TO SCALE.
6. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALISED MARKING, BUT MUST BE LOCATED WITHIN ZONE INDICATED.

ISSUE	1			
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APPRD.				

ZARLINK SEMICONDUCTOR

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Previous package codes

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