Low–Voltage 1:10 Differential ECL/PECL/HSTL Clock Driver

MC100EP111

See Upgrade Product – MC100ES6111

**LOW–VOLTAGE
1:10 DIFFERENTIAL
ECL/PECL/HSTL
CLOCK DRIVER**

FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A

The MC100EP111 is a low skew 1–to–10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single–ended if the V_{BB} output is used. HSTL inputs can be used when the EP111 is operating under PECL conditions. The selected signal is fanned out to 10 identical differential outputs.

- 100ps Part–to–Part Skew typical
- 35ps Output–to–Output Skew typical
- Differential Design
- V_{BB} Output
- Low Voltage V_{EE} Range of –2.25 to –3.8V for ECL
- Low Voltage V_{CC} Range of +2.25 to +3.8V for PECL and HSTL
- 75kΩ Input Pulldown Resistors
- ECL/PECL Outputs

The EP111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100EP111 may be driven single–endedly utilizing the V_{BB} bias output with the $\overline{CLK0}$ input. If a single–ended signal is to be used, the V_{BB} pin should be connected to the $\overline{CLK0}$ input and bypassed to ground via a 0.01 μF capacitor. The V_{BB} output can only source/sink 0.2mA; therefore, it should be used as a switching reference for the MC100EP111 only. Part–to–Part Skew specifications are not guaranteed when driving the MC100EP111 single–endedly.

Rev 1

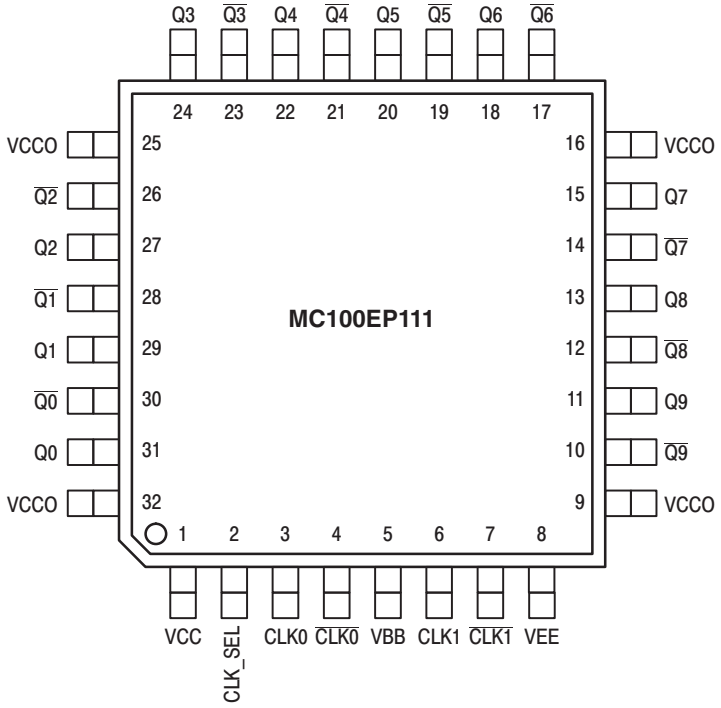

Figure 1. 32–Lead TQFP Pinout
(Top View)

PIN NAMES

Pins	Function
CLK0, $\overline{\text{CLK0}}$	Differential ECL/PECL Input Pair
CLK1, $\overline{\text{CLK1}}$	Differential HSTL Input Pair
Q0:9, $\overline{\text{Q0:9}}$	Differential PECL Outputs
CLK_SEL	Active Clock Select Input
VBB	V_{BB} Output

FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

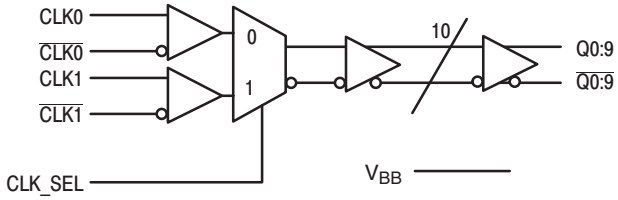

Figure 2. Logic Symbol

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

7

DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

		–40°C			25°C			70°C				
Symbol	**Characteristic**	**Min**	**typ**	**Max**	**Min**	**typ**	**Max**	**Min**	**typ**	**Max**	**Unit**	**Condition**
IEE	Internal supply current	45		85	60		95	65		105	mA	Absolute value of current
ICC	Output and Internal supply current	270		360	290		380	300		380	mA	All outputs terminated 50Ω to VCC–2.0V
IIN	Input current			150			150			150	µA	Includes pullup/ pulldown resisters
VBB	Internally generated bias voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V	for VEE= –3.0 to –3.8 volts
VBB	Internally generated bias voltage	–1.38		–1.16	–1.38		–1.16	–1.38		–1.16	V	for VEE= –2.25 to –2.75 volts
VIH	Input HIGH voltage (CLK_SEL)	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V	
VIL	Input LOW voltage (CLK_SEL)	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V	
VPP	Input amplitude (CLK0,CLK0)	0.5		1.3	0.5		1.3	0.5		1.3	V	Difference of input ≈ VIH – VIL[1]
VCMR	Common mode voltage (CLK0,CLK0)	VEE+1.0		–0.3	VEE+1.0		–0.3	VEE+1.0		–0.3	V	Cross point of input ≈ average (VIH,VIL)
VOH	Output HIGH voltage	–1.30		–0.95				–1.20		–0.90		IOH = –30 mA
VOL	Output LOW voltage	–1.85		–1.40				–1.90		–1.50		IOL = –5 mA
VOUTpp	Differential output swing	350						500			mV	

DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

		–40°C			25°C			70°C				
Symbol	**Characteristic**	**Min**	**typ**	**Max**	**Min**	**typ**	**Max**	**Min**	**typ**	**Max**	**Unit**	**Condition**
IEE	Internal supply current	45		85	60		95	65		105	mA	Absolute value of current
ICC	Output and Internal supply current	270		360	290		380	300		380	mA	All outputs terminated 50Ω to VCC–2.0V
IIN	Input current			150			150			150	µA	Includes pullup/ pulldown resisters
VBB	Internally generated bias voltage	VCC–1.38		VCC–1.26	VCC–1.38		VCC–1.26	VCC–1.38		VCC–1.26	V	for VCC= 3.0 to 3.8 volts
VBB	Internally generated bias voltage	VCC–1.38		VCC–1.16	VCC–1.38		VCC–1.16	VCC–1.38		VCC–1.16	V	for VCC= 2.25 to 2.75 volts
VIH	Input HIGH voltage (CLK_SEL)	VCC–1.165		VCC–0.880	VCC–1.165		VCC–0.880	VCC–1.165		VCC–0.880	V	
VIL	Input LOW voltage (CLK_SEL)	VCC–1.810		VCC–1.475	VCC–1.810		VCC–1.475	VCC–1.810		VCC–1.475	V	
VPP	Input amplitude (CLK0,CLK0)	0.5		1.3	0.5		1.3	0.5		1.3	V	Difference of input ≈ VIH – VIL[1]
VCMR	Common mode voltage (CLK0,CLK0)	1		VCC–0.3	1		VCC–0.3	1		VCC–0.3	V	Cross point of input ≈ average (VIH,VIL)
Vdif	Differential input voltage (CLK1,CLK1)	0.4		1.9	0.4		1.9	0.4		1.9	V	Difference of input ≈ VIH – VIL
Vx	Input crossover voltage (CLK1,CLK1)	0.68		0.9	0.68		0.9	0.68		0.9	V	Cross point of input ≈ average (VIH,VIL)

DC CHARACTERISTICS
Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

VOH	Output HIGH voltage	VCC–1.30	VCC–0.95		VCC–1.20	VCC–0.90		IOH = –30 mA
VOL	Output LOW voltage	VCC–1.85	VCC–1.40		VCC–1.90	VCC–1.50		IOL = –5 mA
VOUTpp	Differential output swing	350			500		mV	
Note 1.	VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 100 mV.							

AC CHARACTERISTICS – PECL Input
Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts –OR–
VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

		–40°C			25°C			70°C				
Symbol	**Characteristic**	**Min**	**typ**	**Max**	**Min**	**typ**	**Max**	**Min**	**typ**	**Max**	**Unit**	**Condition**
Tpd	Differential propagation delay											Nominal (single input condition VPP = 0.650V, VCMR = VCC–0.800V
	CLK0,$\overline{CLK0}$ to all Q0,$\overline{Q0}$ thru Q9,$\overline{Q9}$	350		500	380		530	450		600	ps	Note 2
Tsk(part)	Part to part skew			150			150			150	ps	Note 2
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Tpd	Differential propagation delay CLK0,$\overline{CLK0}$ to all Q0,$\overline{Q0}$ thru Q9,$\overline{Q9}$	280		600	300		620	370		700	ps	Note 2
Tsk(part)	Part to part skew			320			320			330	ps	Note 2
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Fmax	Maximum frequency			1500			1500			1500	MHz	Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	All outputs terminated 500Ω to VCC–2.0V

7

AC CHARACTERISTICS – HSTL Input
Vsupply : VCC=VCC0 = 2.25 to 3.8 volts, VEE = 0.0 volts

Symbol	Characteristic	–40°C Min	–40°C typ	–40°C Max	25°C Min	25°C typ	25°C Max	70°C Min	70°C typ	70°C Max	Unit	Condition
Tpd	Differential propagation delay											Nominal (single input condition Vdif = 1.000V, Vx = VEE+0.750V
	CLK1,$\overline{CLK1}$ to all Q0,$\overline{Q0}$ thru Q9,$\overline{Q9}$	380		530	420		570	500		650	ps	Note 2
Tsk(part)	Part to part skew			150			150			150	ps	Note 2
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Tpd	Differential propagation delay											All input conditions (full input range)
	CLK1,$\overline{CLK1}$ to all Q0,$\overline{Q0}$ thru Q9,$\overline{Q9}$	300		600	350		650	430		750	ps	Note 2
Tsk(part)	Part to part skew			300			300			320	ps	Note 2
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Fmax	Maximum frequency			250			250			250	MHz	Functional to 250 MHz Timing specifications apply up to 250 MHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	All outputs terminated 500Ω to VCC–2.0V
Note 2.	For operation with 2.5 volt supply, the output termination is 50Ω to VEE. For operation at 3.3 volt supply, the output termination is 50Ω to VCC–2v.											