

1.0 Features

- Three PLLs with deep reference, feedback, and post dividers to provide precision clock frequencies
- Multiple outputs provide several clocking options
- Suspend feature shuts down a selection of PLLs and outputs for power conservation
- Outputs may be tristated for board testing
- S0 and S1 frequency select inputs modify output frequencies for design flexibility
- Glitch-free slewing of CLK_CPU output enables downstream PLLs to remain locked
- 5V to 3.3V operation
- Accepts 5 to 30MHz crystals
- Custom frequency patterns, pinouts, and packages are available. Contact your local AMI Sales Representative for more information.

2.0 Description

The FS6322 is a ROM-based CMOS clock generator IC designed to minimize cost and component count in a variety of electronic systems.

Three low-jitter phase-locked loops (PLLs) drive up to five low-skew clock outputs to provide a high degree of flexibility. A buffered copy of the reference clock is also available. The device is packaged in a 16-pin SOIC to minimize board space.

Figure 1: Pin Configuration

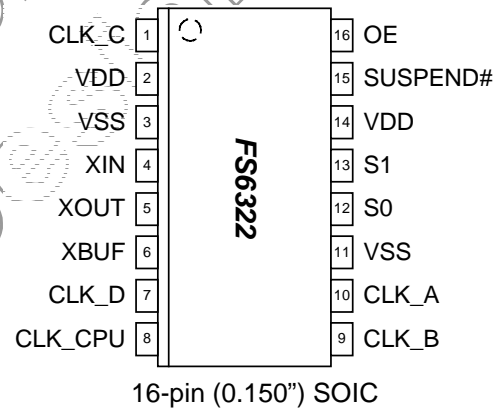
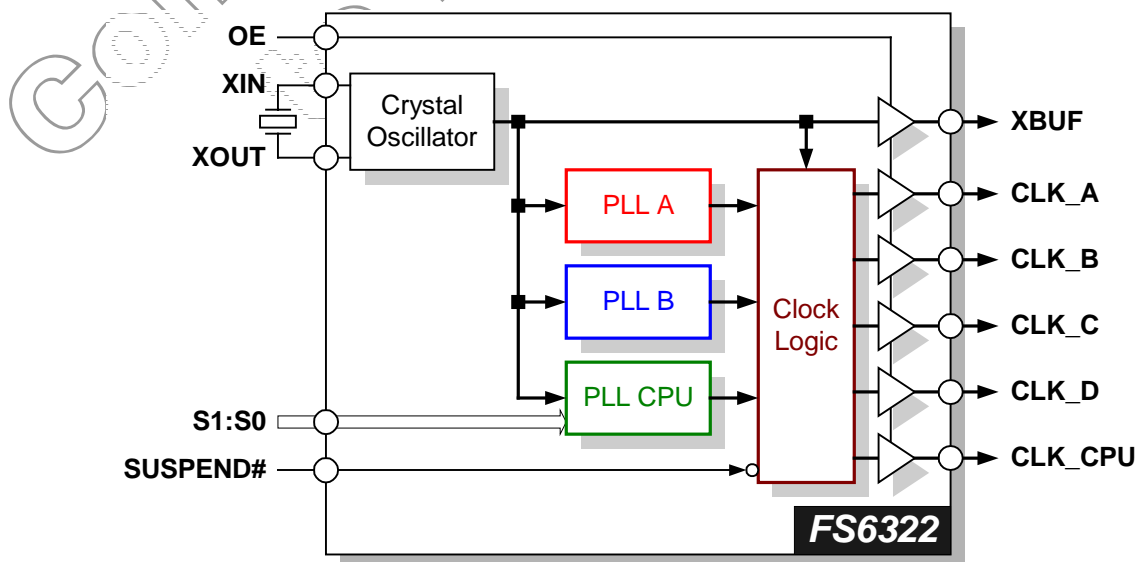


Figure 2: Block Diagram



FS6322-02

Three-PLL Clock Generator IC



Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	DO	CLK_C	C clock output
2	P	VDD	Power supply (5V to 3.3V)
3	P	VSS	Ground
4	AI	XIN	Crystal oscillator feedback
5	AO	XOUT	Crystal oscillator drive
6	DO	XBUF	Buffered crystal oscillator frequency output
7	DO	CLK_D	D clock output
8	DO	CLK_CPU	CPU PLL output with controlled frequency slew rate
9	DO	CLK_A	A clock output
10	DO	CLK_B	B clock output
11	P	VSS	Ground
12	DI	S0	Frequency select control input for the CLK_CPU output
13	DI	S1	Frequency select control input for the CLK_CPU output
14	P	VDD	Power supply (5V to 3.3V)
15	DI	SUSPEND#	Active-low control input powers-down selected PLLs and outputs
16	DI	OE	Output enable input; logic-high enables outputs; logic-low tristates outputs (high impedance)

**Table 2: Frequency Table
FS6322-02: 3.3 volt device
(all frequencies in MHz)**

SUSPEND#	S1	S0	FREF	CLK_A (pin 10)	CLK_B (pin 9)	CLK_C (pin 1)	CLK_D (pin 7)	XBUF (pin 6)	CLK_CPU (pin 8)
0	0	0	14.31818	25.00000	OFF	OFF	OFF	OFF	OFF
0	0	1	14.31818	20.00000	48.00000	66.00000	24.57598	14.31818	14.31818
0	1	0	DO NOT USE						
0	1	1	DO NOT USE						
1	0	0	14.31818	25.00000	40.00000	40.00000	40.00000	14.31818	24.57598
1	0	1	14.31818	20.00000	48.00000	83.00071	24.57598	14.31818	14.31818
1	1	0	DO NOT USE						
1	1	1	DO NOT USE						

3.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc ($V_{SS} = \text{ground}$)	V_{DD}	$V_{SS}-0.5$	7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	-50	50	mA
Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	$5V \pm 10\%$	4.5	5	5.5	V
		$3.3V \pm 10\%$	3	3.3	3.6	
Ambient Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XIN}		5		30	MHz
Output Load Capacitance	C_L				15	pF

FS6322-02

Three-PLL Clock Generator IC



4.0 Package Information

Table 5: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
θ	0°	8°	0°	8°

Diagram illustrating the mechanical dimensions of the 16-pin SOIC package. The drawing shows the top view, a side view, and a detailed view of the lead profile. Key dimensions include: A (package height), A1 (lead height), A2 (lead height to seating plane), B (lead width), C (lead thickness), D (package width), E (lead pitch), H (total height), h (lead thickness), L (lead length), and θ (lead angle). The package is labeled 'AMI AMERICAN MICROSYSTEMS, INC.' and '16'. A note specifies 'ALL RADII: 0.005" TO 0.01"'. The base and seating planes are also indicated.

Table 6: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 16-pin 0.150" SOIC	θ_{JA}	Air flow = 0 m/s	95	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

5.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11825-101	FS6322-02	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel

Contact Factory Prior to New Designs

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