

75Ω Driver IC for HD Monolithic IC MM1797 Series

Outline

This IC is a video driver IC that realizes the frequency characteristics necessary for analog high definition signals. It deletes S video signals (Y/C) from the video signals to be output to maintain only the composite signals (CVBS) and the component signals (PY/Pb/Pr).

This feature helps its package to be miniaturized and the mounting area to be reduced. As a video output driver, this IC is best suited to a BD/DVD player.

Features

- Built-in LPF whose passband is 30 MHz for 1080i or 720p/XGA HD video signals.
- Rank A : Use of a new SAG correction circuit (patent pending) and reduction in the output coupling capacitance.
Rank C : Use of a positive power supply and a negative power supply to eliminate the output coupling capacitance.
Rank D/E : Use of a simple output circuit without "C" and elimination of output coupling capacitance.
- Any additional electrostatic protection circuit is not required since the video output terminal has passed the ESD aerial discharge test (conforming to IEC610000-4-2).

		A-rank	C-rank	D-rank	E-rank
Input Signal		CVBS, Y, Pb, Pr (4ch)			
Output Signal		CVBS, Y, Pb, Pr (4ch)			
Supply Voltage		+5V single	+3.3V, -5V dual	+3V or +3.3V single	
Output Circuit		New sag correction circuit 220μF, 2.2μF	Out capacitor - less		
SD/HD LPF Select		○ H, M, L	○ H, L	× LPF HD Hold	
Mute		All channel		PY, Pb, Pr	
L P F	CVBS (High : pass BW, Low : stop BW)	6.75MHz 27MHz	6.75MHz 47.25MHz	6.75MHz 27MHz	
	Y/Pb/Pr - SD (High : pass BW, Low : stop BW)	13.5MHz 54MHz			
	Y/Pb/Pr - HD (High : pass BW, Low : stop BW)	30MHz 74MHz	30MHz 112MHz	27MHz 74MHz	30MHz 148MHz
Package		TSOP-16B (0.65mm pitch)			
Note		If the 75Ω termination on the TV side is AC termination, the signal may not be output.			

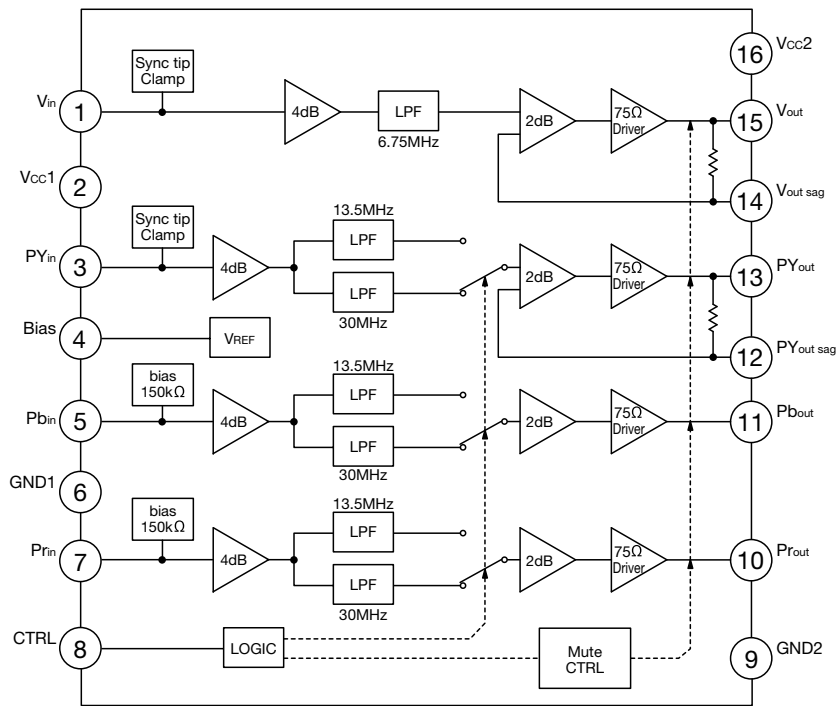
Packages

TSOP-16B

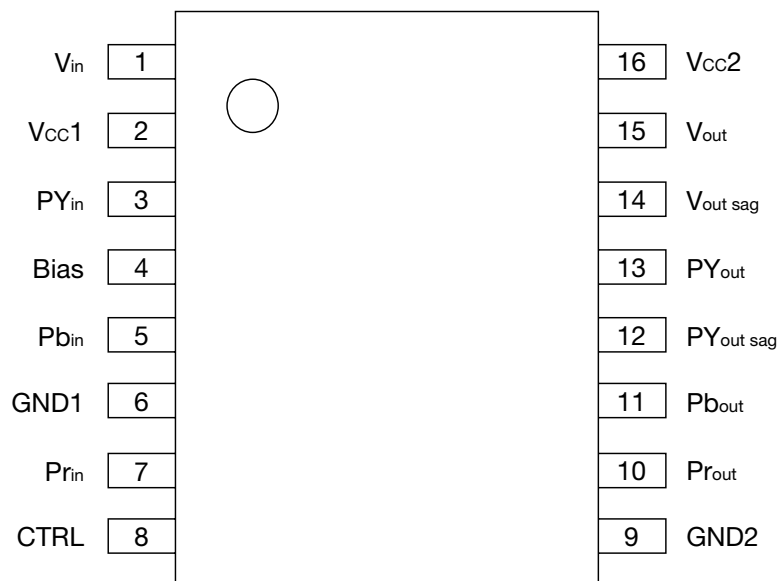
Applications

- BD/DVD Players
- Set Top Boxes

Block Diagram



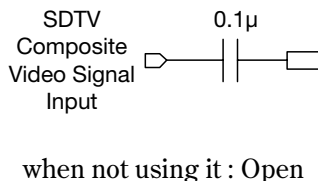
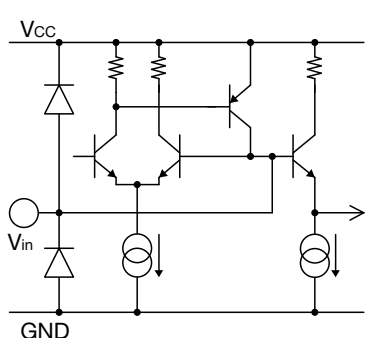
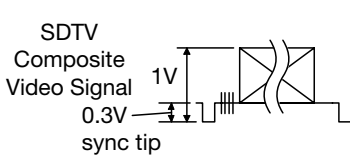
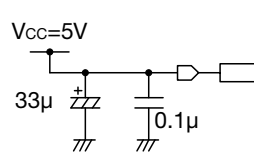
Pin Assignment

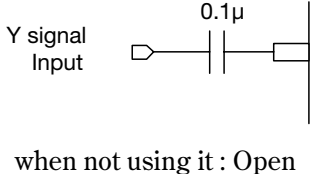
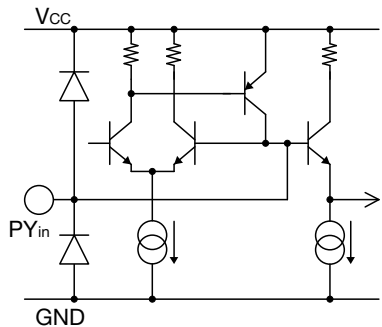
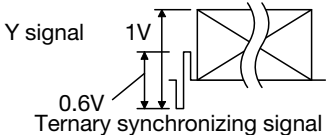
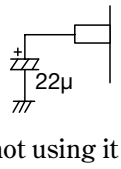
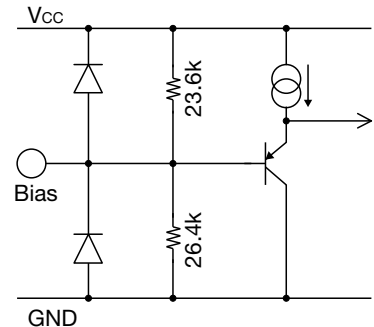


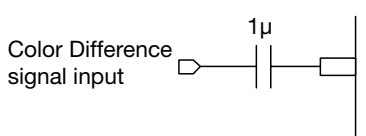
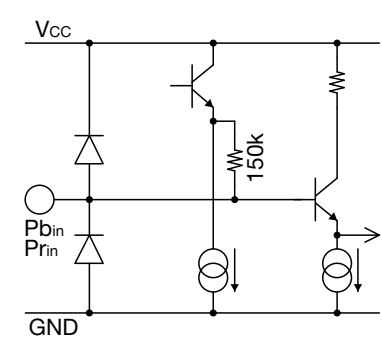
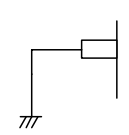
TSOP-16B
(TOP VIEW)

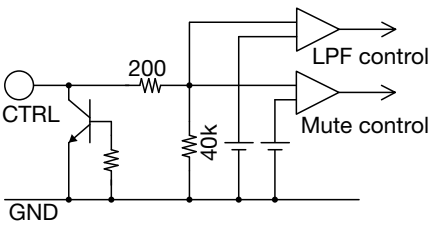
1	V _{in}	9	GND2
2	V _{cc} 1	10	P _r _{out}
3	P _Y _{in}	11	P _b _{out}
4	Bias	12	P _Y _{out sag}
5	P _b _{in}	13	P _Y _{out}
6	GND1	14	V _{out sag}
7	P _r _{in}	15	V _{out}
8	CTRL	16	V _{cc} 2


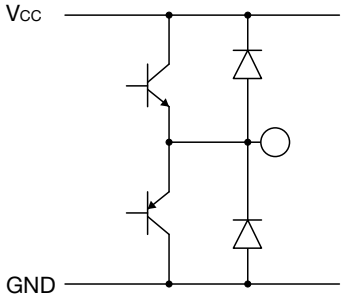

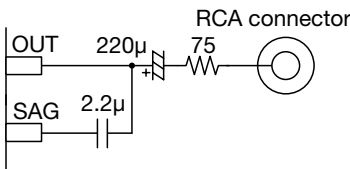
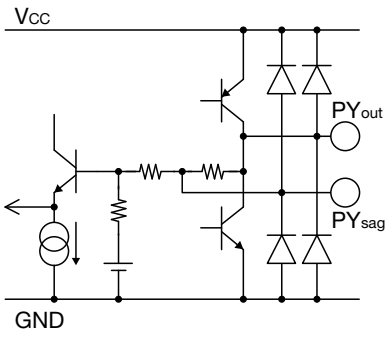
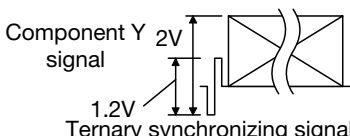
Pin Description

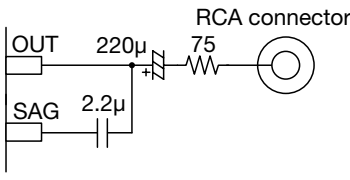
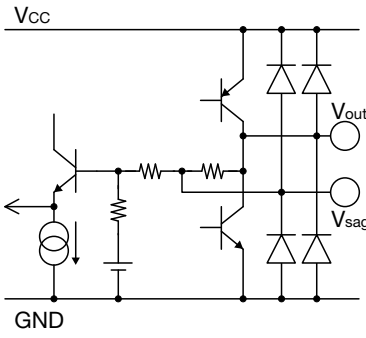
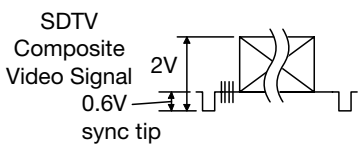
Pin No.	Pin name	Pin description	
1	V _{in}	Function	
		Composite Video Signal Input Pin to input composite video signals Clamp input pin Pin voltage : 1.3V (typ.)	
		External circuit	Internal equivalent circuit
		 <p>when not using it : Open</p>	
		Input signal	
			
2 16	V _{cc1} V _{cc2}	Function	
		Voltage Supply Pin to apply a positive supply voltage. Apply 5V. Pin2 and Pin16 are not shorted inside the IC. V _{cc2} is connected to an output stage circuit, and V _{cc1} is connected to a circuit other than an output stage circuit. Note : Please arrange power supply bypass capacitor near the terminal.	
		External circuit	Internal equivalent circuit
		 <p>when not using it : Open</p>	
		Input signal	
		DC Voltage : 4.5V to 5.5V	

Pin No.	Pin name	Pin description	
3	PY _{in}	Function	
		Y Signal Input (for HD) Pin to input Y signals. Clamp input pin. Pin voltage : 1.3V (typ.)	
		External circuit	Internal equivalent circuit
		 <p>Y signal Input</p> <p>0.1µ</p> <p>when not using it : Open</p>	 <p>VCC</p> <p>GND</p> <p>PY_{in}</p>
Input signal			
		 <p>Y signal</p> <p>1V</p> <p>0.6V</p> <p>Ternary synchronizing signal</p>	
4	Bias	Function	
		bias All the reference voltages used inside the IC are produced according to the resistance divider of this pin. Pin to stabilize reference voltages, and reduce both power supply ripple and crosstalk by decreasing impedance with an external 22µF.	
		External circuit	Internal equivalent circuit
		 <p>22µ</p> <p>when not using it : Open</p>	 <p>VCC</p> <p>GND</p> <p>Bias</p> <p>23.6k</p> <p>26.4k</p>
Input signal			

Pin No.	Pin name	Pin description	
5 7	Pb _{in} Pr _{in}	Function	
		Color Difference Signal Input (for HD) Pin to input color difference signals. Bias input pin. Pin voltage : 2.6V (typ.) Input impedance : 150kΩ (typ.)	
		External circuit	Internal equivalent circuit
		 <p>Color Difference signal input</p> <p>when not using it : Open</p>	
		Input signal	
		Function	
6 9	GND1 GND2	Ground Ground pin.	
		External circuit	Internal equivalent circuit
			
		Input signal	

Pin No.	Pin name	Pin description	
8	CTRL	Function	
		<p>LPF select Mute control</p> <p>LPF band selection and all output mute ON/OFF of PY/Pb/Pr can be selected according to the voltage applied to this pin.</p> <p>L level applied ... Mute ON M level applied ... Mute OFF, LPF passband 13.5MHz selected H level applied ... Mute OFF, LPF passband 30MHz selected</p> <p>L level input voltage : max.0.4V M level input voltage : min.1.4V max.3.0V H level input voltage : min.3.5V max.5.0V</p> <p>Input impedance : 40kΩ (typ.)</p>	
		External circuit	Internal equivalent circuit
		<p>H Level (3.4V~5.0V) CTRL</p> <p>M Level (1.4V~3.4V) →</p> <p>L Level (0V~1.4V)</p>	
Input signal			

Pin No.	Pin name	Pin description	
10 11	Pb _{out} Pr _{out}	Function	
		<p>Color Difference Signal Pb/Pr Output Pin to output color difference signals. Bias output pin.</p> <p>Pin voltage : 2.70V (typ.) Output Dynamic Range : 2.8Vp-p (typ.)</p> <p>Keep the wire as short as possible between each video output pin and 75Ω.</p>	
		External circuit	
		Internal equivalent circuit	
			
		Input signal	
		<p>Color Difference Signal</p>  <p>Ternary synchronizing signal</p>	
12 13	PY _{out sag} PY _{out}	Function	
		<p>Component Y Signal Output Pin to output component Y signals. Clamp output pin.</p> <p>Pin voltage : SAG terminal is not used 0.9V (typ.) SAG terminal is used 0.4V (typ.)</p> <p>Output Dynamic Range : 2.8Vp-p (typ.)</p> <p>Keep the wire as short as possible between each video output pin and 75Ω.</p>	
		External circuit	
		Internal equivalent circuit	
			
		Input signal	
		<p>Component Y signal</p>  <p>Ternary synchronizing signal</p>	

Pin No.	Pin name	Pin description	
Function			
<p>Composite Video Signal Output Pin to output composite video signals. Clamp output pin.</p> <p>Pin Voltage : SAG terminal is not used 0.9V (typ.) SAG terminal is used 0.4V (typ.)</p> <p>Output Dynamic Range : 2.8Vp-p (typ.)</p> <p>Keep the wire as short as possible between each video output pin and 75Ω.</p>			
		External circuit	Internal equivalent circuit
<p>14 15</p>	<p>$V_{out\ sag}$ V_{out}</p>		
	Input signal		
			

Absolute Maximum Ratings (Except where noted otherwise Ta=25°C)

Parameter	Symbol	Ratings	Units
Storage temperature	T _{stg_s}	-55~+150	°C
Operating temperature	T _{opr_s}	-40~+85	°C
Supply voltage	V _{CC max_s}	6	V
Junction Temperature	T _{jmax.}	150	°C
Power dissipation (Note1)	P _{d_s}	1.0	W

Note1 : When mounting on the board made of the glass epoxy. (40×40×1.6mm)

Recommended Operating Conditions

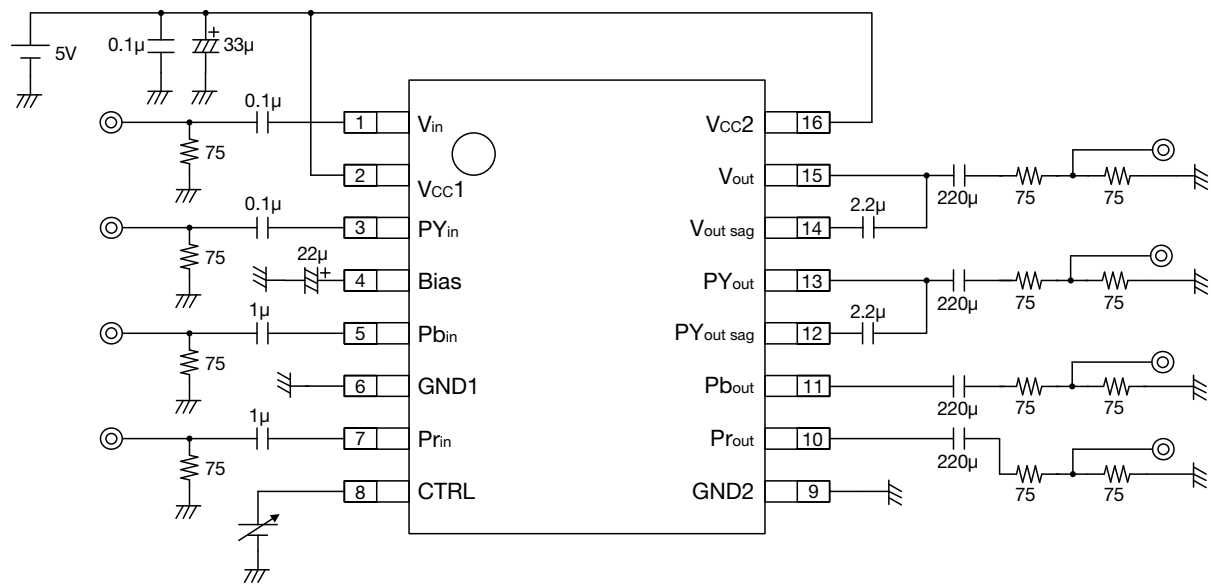
Parameter	Symbol	Ratings	Units
Operating temperature	T _{opr_s}	-40~+85	°C
Operating voltage	V _{ccop_s}	4.5~5.5	V

Electrical Characteristics (Except where noted otherwise Ta=25°C, V_{cc1}, V_{cc2}=5V)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units	
Supply current 1	I _{cc1}	No signal	35	50	65	mA	
Supply current 2	I _{cc2}	No signal Mute ON	1.8	2.5	3.2	mA	
Terminal voltage	Composite video input	V _{vin}	1.1	1.3	1.5	V	
	Luminance input	V _{PYin}	1.1	1.3	1.5	V	
	Component input	V _{Pbin, Prin}	2.3	2.6	2.9	V	
	Composite video output 1	V _{Vout1}	14pin-15pin short-circuited		0.90		V
	Composite video output 2	V _{Vout2}	Sag terminal used		0.40		V
	Luminance output 1	V _{Vout1}	12pin-13pin short-circuited		0.90		V
	Luminance output 2	V _{Vout2}	Sag terminal used		0.40		V
	Component output	V _{Pbout, Prout}			2.70		V

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Output dynamic range	DR _V	SIN wave : 100kHz, THD=1.0%	2.6	2.8		V
	DR _{PY, Pb, Pr}	SIN wave : 100kHz, THD=1.0%	2.6	2.8		V
Control terminal input voltage	H	V _{thH}	3.5		5.0	V
	M	V _{thM}	1.4		3.0	V
	L	V _{thL}			0.4	V
Control terminal input current	H	I _H V _H =5V			190	μA
	M	I _M V _M =3V			115	μA
	L	I _L V _L =0.4V			15	μA
Input impedance	Z _{Pbin,Prin}		100	150	200	kΩ
Voltage gain	GV	SIN wave : 1V, f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic (V)	f1	SIN wave : 1V, 6.75MHz/100kHz	-1	0	1	dB
	f2	SIN wave : 1V, 27MHz/100kHz		-33	-27	dB
Frequency characteristic (PY, Pb, Pr-SD)	f3	SIN wave : 1V, 13.5MHz/100kHz	-1	0	1	dB
	f4	SIN wave : 1V, 54MHz/100kHz		-33	-27	dB
Frequency characteristic (PY-HD)	f5	SIN wave : 1V, 30MHz/100kHz	-1	0	1	dB
	f6	SIN wave : 1V, 74MHz/100kHz		-33	-27	dB
Frequency characteristic (Pb, Pr-HD)	f7	SIN wave : 1V, 15MHz/100kHz	-1	0	1	dB
	f8	SIN wave : 1V, 30MHz/100kHz	-3.0	-1.0	1.0	dB
	f9	SIN wave : 1V, 74MHz/100kHz		-33	-27	dB
Group delay (V)	t1	at 100kHz		45	80	ns
Group delay (PY, Pb, Pr)	t2	at 100kHz		25	50	ns
Group delay deviation 1 (V)	Δt1	to 3.58MHz		4	10	ns
		to 4.43MHz		6	10	ns
		to 6MHz		12	20	ns
Group delay deviation 2 (PY, Pb, Pr)	Δt2	to 4MHz		1	10	ns
		to 24MHz		6	15	ns
Between channel Group delay deviation 1	Δt1 _{ch}	Between PY and Pb (Pr) at 4MHz		1	10	ns
Differential gain	DG	Staircase signal 1V		0.5	2.0	%
Differential phase	DP	Staircase signal 1V		0.5	2.0	°
Crosstalk 1	CT1	f=4.43MHz, 1V		-60	-55	dB
Crosstalk 2	CT2	f=20MHz, 1V		-45	-40	dB
S/N 1	SN1	BW : 100k ~ 6MHz		-80		dB
S/N 2	SN2	BW : 100k ~ 6MHz at SD select		-80		dB
S/N 3	SN3	BW : 100k ~ 30MHz at HD select		-66		dB

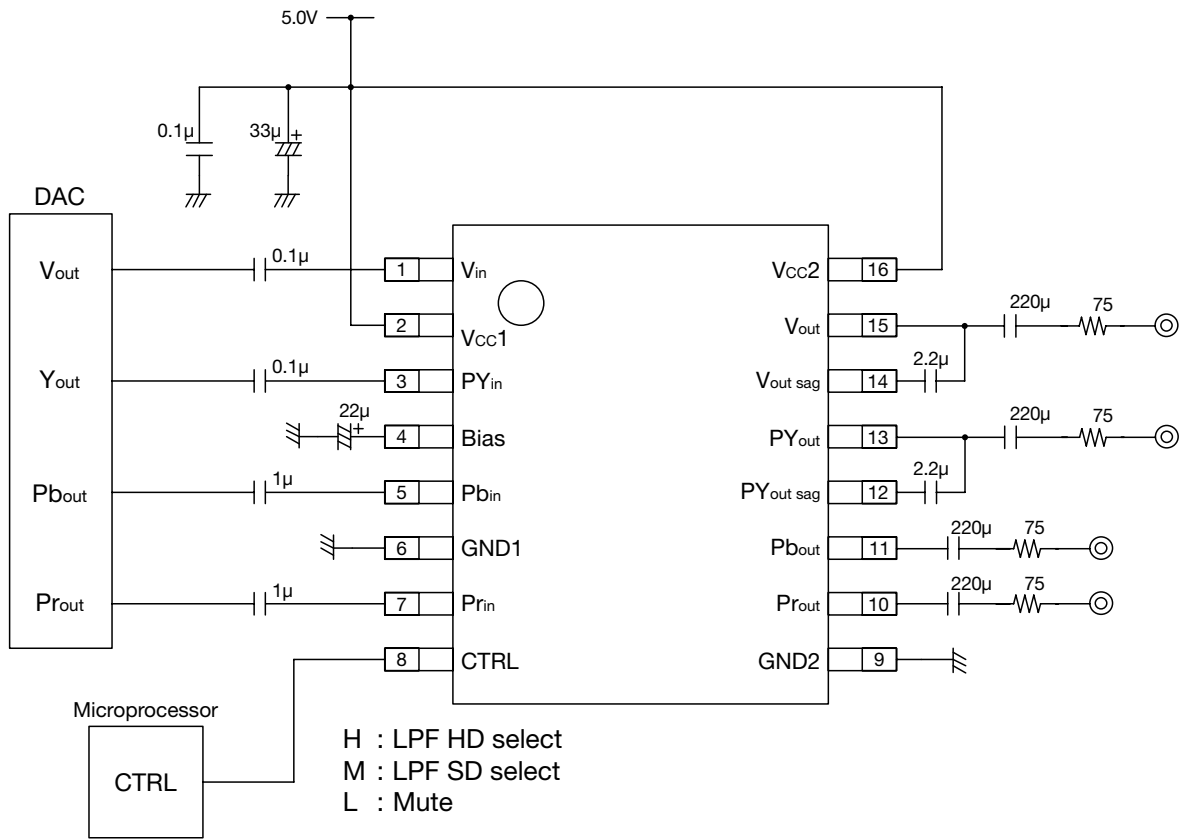
Measuring Circuit



Switch Control Table

CTRL-Pin	Mute	SD/HD select
H (3.5V~ 5.0V)	OFF	HD
M (1.4V~ 3.0V)	OFF	SD
L (0V~ 0.4V)	ON	
OPEN	ON	

Application Circuit



Note : Please arrange power supply bypass capacitor near the V_{CC} terminal (pin).

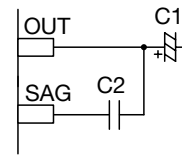
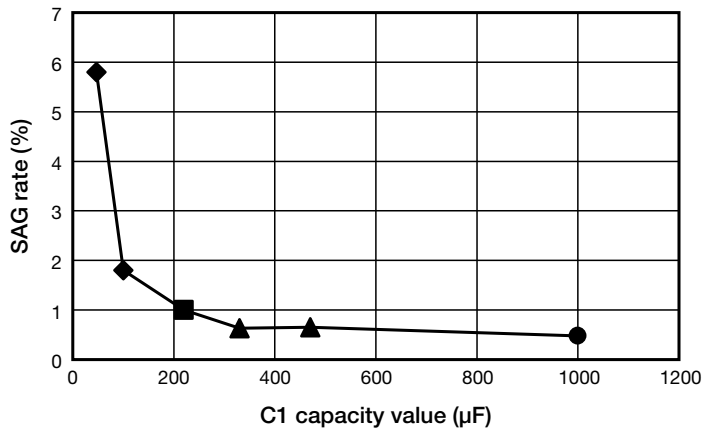
Note : Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

Note : Keep the wire as short as possible between each video output pin and 75Ω.

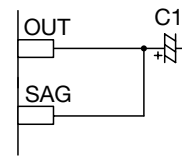
Note : Please use it after it confirms it enough by the installing set when you use applied circuit.

Supplemental 1 : SAG terminal

Please design the capacitor that connects it with the terminal SAG referring to the figure below.



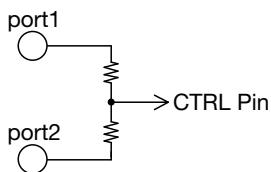
- ◆ : C2=1μF
- : C2=2μF
- ▲ : C2=4μF
- : SAG terminal is not used



Supplemental 2 : CTRL terminal

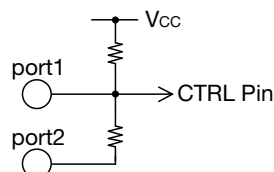
Please refer to figure shown below when you use microprocessor without three value output.

For CMOS output



port1	port2	CTRL
H	H	H
H	L	M
L	H	M
L	L	L

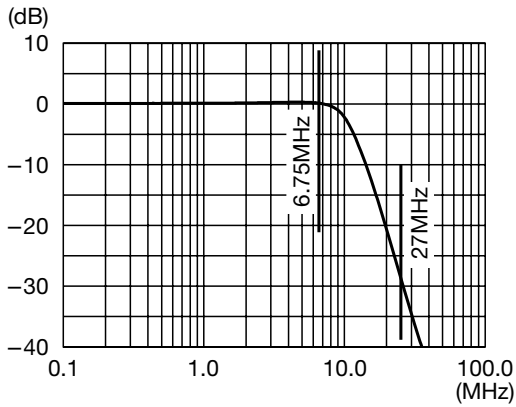
For NMOS open drain output



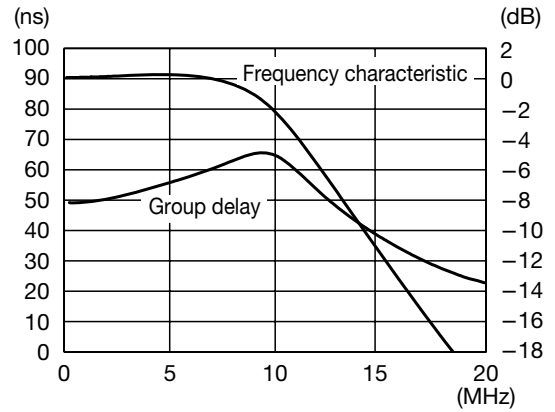
port1	port2	CTRL
H	H	H
H	L	M
L	H	L
L	L	L

Characteristics

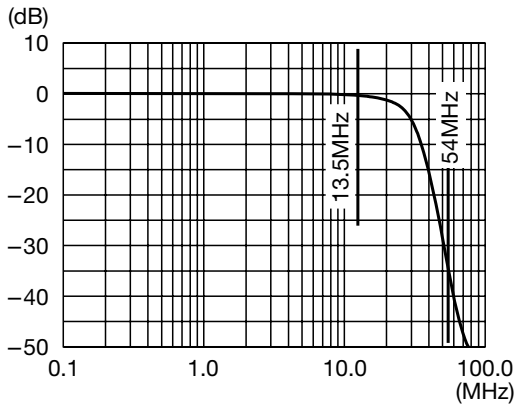
Frequency characteristic
(V_{out})



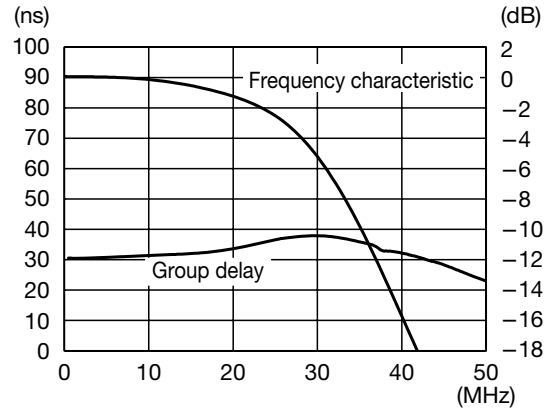
Group delay
(V_{out})



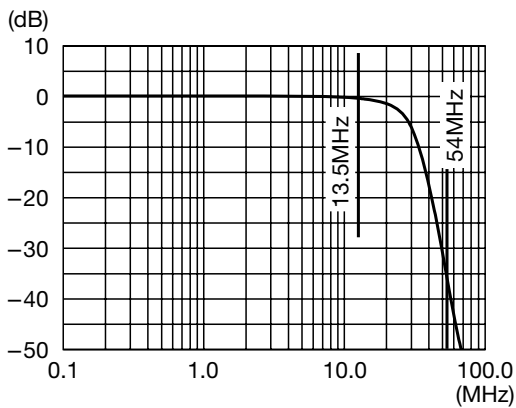
Frequency characteristic
(PY_{out} at SD select)



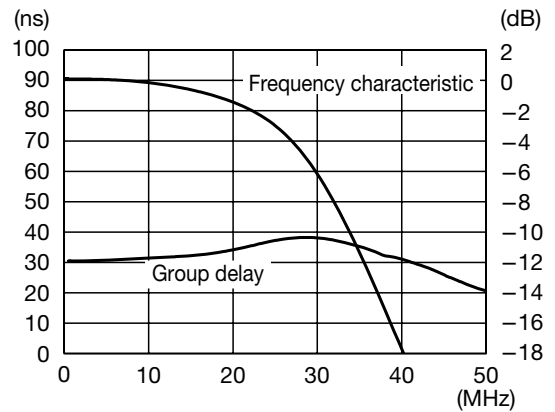
Group delay
(PY_{out} at SD select)



Frequency characteristic
(Pb_{out}/Pr_{out} at SD select)

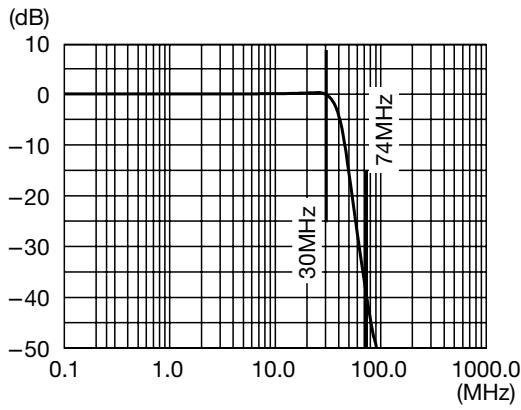


Group delay
(Pb_{out}/Pr_{out} at SD select)

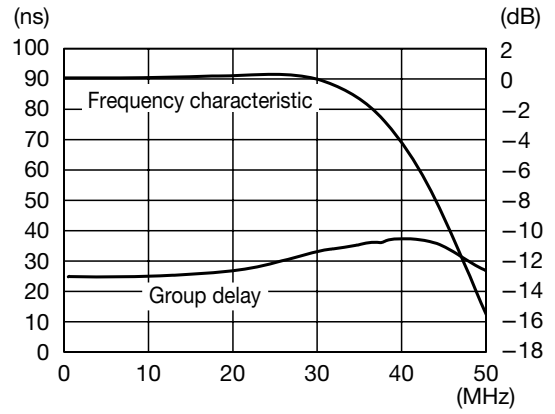


Note : The measurement point of all data is a middle point of 75Ω.

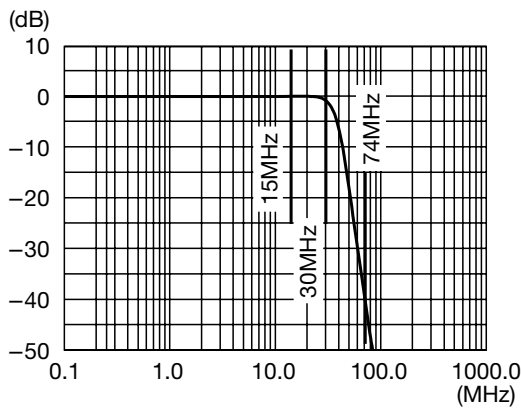
Frequency characteristic
(PY_{out} at HD select)



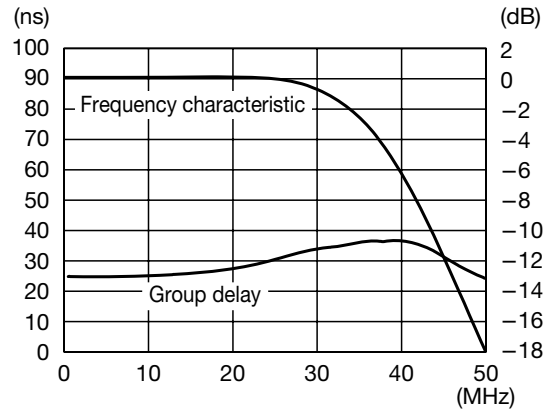
Group delay
(PY_{out} at HD select)



Frequency characteristic
(Pb_{out}/Pr_{out} at HD select)



Group delay
(Pb_{out}/Pr_{out} at HD select)



Note : The measurement point of all data is a middle point of 75Ω.