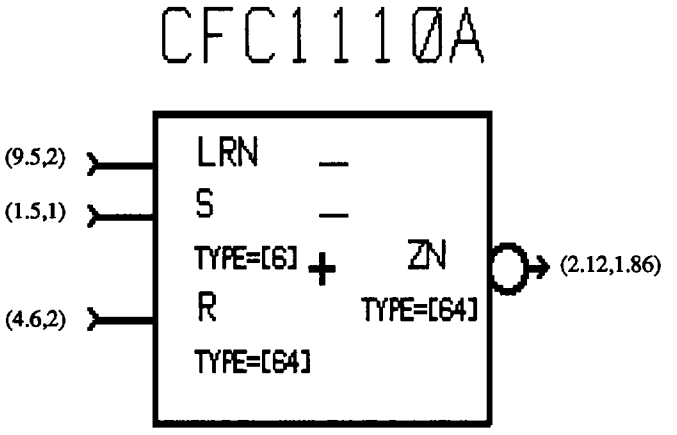
GENERAL DESCRIPTION: 64-BIT, ARITHMETIC, LEFT & RIGHT SHIFT WITH 0 FILL.

CFC1110A performs a 64-bit arithmetic shift. The LRN line controls shift direction to left if LRN=1, and right if LRN=0. Select signals S[5:0] set the number of bits to be shifted. Shift positions are filled with '0'. All outputs are out-of-phase with the inputs.

PIN CONNECTION DIAGRAM:



FEATURES:

- Shift left and right
- Backfilled with '0'

EQUIVALENT USED GATES: 957 GATES
(for rough area estimates)

THIS MEGAFUNCTION CONSISTS OF :
957 soft-coded gates.

POWER: NOT AVAILABLE.

FAULT COVERAGE(%): 100%

PIN DESCRIPTION:

LRN	SHIFT DIRECTION CONTROL LINE
S5:0	ENCODED SELECT LINES
R63:0	DATA INPUTS
ZN63:0	DATA OUTPUTS

AC CHARACTERISTICS:
(Nominal case, output loading is 2, delay predicted by LPACE)

PATH	10K DELAY TYP. ns	100K DELAY TYP. ns
R(I) TO OUTPUT ZN(I)	7.9	6.4
S(I) TO OUTPUT ZN(I)	10.1	8.1
LRN TO OUTPUT ZN(I)	9.9	7.8