SCD # QM5338
Source Control Drawing

Manufacturing Specification P/N **FT22V10(L)-XX/XXX**

Date-11.12.04	iss-1	Rev-	Changes-Orig	Name-MLSalmon
Date-	iss-	Rev-	Changes-	Name-
Date-	iss-	Rev-	Changes-	Name-
Date-	iss-	Rev-	Changes-	Name-
Date-	iss-	Rev-	Changes-	Name-
Date-	iss-	Rev-	Changes-	Name-

1 **INTRODUCTION/PURPOSE**

This document specifies the manufacturing, procurement details and screening requirements.
In brief the part is: EPLD
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2 **REFERENCE DOCUMENTS**

Test Method and procedures for Microcircuits	MIL-STD-883 (latest issue)	Department of Defence Washington DC 20363-5100, USA
General Specs for Hybrids Sort, incoming and outgoing Inspection procedures	MIL-PRF-38534	

3 **SOURCE OF PARTS**

This section provides an overview of the companies involved in the manufacture, screening and supply of the part. Original procurement of parts shall be from the address specified in section 3.3.

3.1 **Original Part Manufacturer**

The original die are/were produced by : Atmel

Manufacturer: Atmel
Address:

USA

The donor part number is: AT22V10W

3.2 **Assy /Manu,/Screening Company**

The above parts are then assembled and screened by:
Classified Disclosure under NDA or disclosed as:

3.3 **UK Supplier**

The assembled/screened parts shall be procured from:

Force Technologies Ltd
Ashley Court,
Henley,
Marlborough,
Wilts, UK
SN8 3RH

Tel: +44(0)1264 731200
Fax: +44(0)1264 731444

The Force Technologies part number(Ordering Code) is: **FT22V10(L)-speed/pkg/temp (/LF) QM5338**

4.0 **Manufacture**

(Manufacturing processes, assembly, Screen and test equipment listings available for inspection upon request.
Part Number breakdown

FT22V10(L)-15/20/25/pkg/temp +optional (/LF) Pb free

D	=	0.3” Dil 24 Pin Windowed	C	=	Comm
G	=	0.3” Dil 24 Pin Non-Windowed	I	=	Ind
N	=	28 pad LCC Non-Windowed	M	=	Mil temp
L	=	28 pad LCC Windowed	MB		Mil-Std-883

4.1 **SCREENING**

The AT22V10(L)-XX XMB shall be screened as specified in the table below.

All batches of parts shall be supplied with a Certificate of Conformity. The certificate of conformity shall reference the screening specified below.

Screening	**Method**	**Req.t**	**Note**
Visual Inspection	Incoming and Outgoing Inspection Procedures	100%	1
Internal Visual (Pre-Cap)	2010 Cond B (applicable to packaging parts)	100%	
Destructive tests		Optional	
Temperature cycling	1010, test condition C	100%	
Constant acceleration	2001, test condition E (min) Y1 orientation only	100%	
Seal a. Fine b. Gross	1014	100%	
Visual inspection		100%	
Interim Electrical		Optional	
Burn-in test	1015, 160 hours at 125°C minimum	100%	
Percentage defective allowable (PDA) calculation	5 percent	All lots	2
Final electrical test A) Static Tests 1)25oC (Subgroup1) 2)Max. & Min. rated opp. temp (Subgroup 2&3) B) Dynamic Test or Switching Test 25oC(Subgroup 4 or 9) C)Functional Test 25oC (Subgroup 7)	In accordance with applicable device specification.	100%	3
External Visual	2009	100%	
Radiation latch-up	1020	Optional	
Group B	5005	Optional	
Group C	5005	Optional	
Group D	5005	Optional	

Notes:
1/ For Pre-assembled product
2/ Manufactured batches shall have Lots tests carried out in accordance with Mil-Std-883
3/ Part No. **AT22V10(L)-XX XMB** Data sheet included on .PDF copy

Manufacturing

Test	**Method**
Wire Bond	2011
Die Shear	2019
Marking	2015

Additional manufacturing notes.

Features

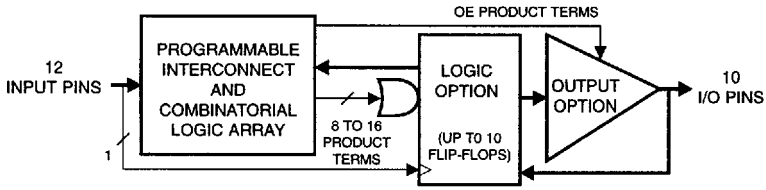
- **High Speed Programmable Logic Device**
  - **15 ns Max Propagation Delay**
  - **5 V ±10% Operation**
- **Low Power CMOS Operation**

Speed	"L"	-15,-20	All
Temp	Com./Mil.	Com./Mil.	Others
Icc(mA)	12/15	90/100	55

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages**

High Speed UV Erasable Programmable Logic Device

Logic Diagram



Description

The AT22V10 and AT22V10L are CMOS high performance EPROM-based Programmable Logic Devices (PLDs). Speeds down to 15 ns and power dissipation as low as 12 mA are offered. All speed ranges are specified over the full 5 V ±10% range. All pins offer a low ±10 µA leakage.

The AT22V10L provides the optimum low power CMOS PLD solution, with low DC power (8 mA typical) and full CMOS output levels. The AT22V10L significantly reduces total system power and enhances system reliability.

Full CMOS output levels help reduce power in many other system components.

The AT22V10 and AT22V10L incorporate a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

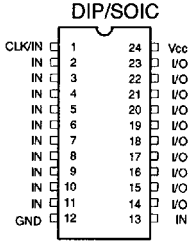
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

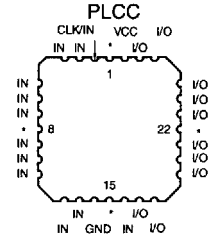
Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



PLCC



0023C

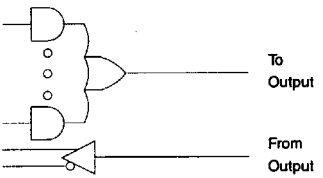
Absolute Maximum Ratings*

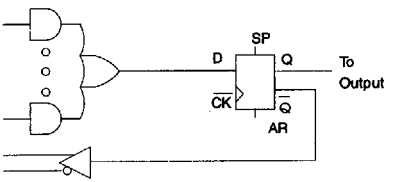
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

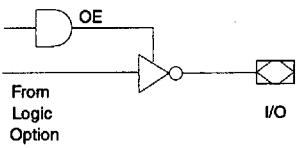
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

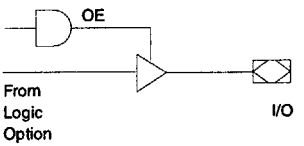
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22V10/L -15, -20, -25	Industrial AT22V10/L -15, -20, -25	Military AT22V10/L -15, -20, -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND, Outputs Open	AT22V10-15,-20	Com.			90	mA
				Ind., Mil.			100	mA
			AT22V10-25,-35[2]				55	mA
			AT22V10L[2]	Com.		1.7	12	mA
				Ind., Mil.		2.0	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	AT22V10L[2]	Com.		2.0		mA/MHz
				Ind., Mil.		2.0		mA/MHz
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

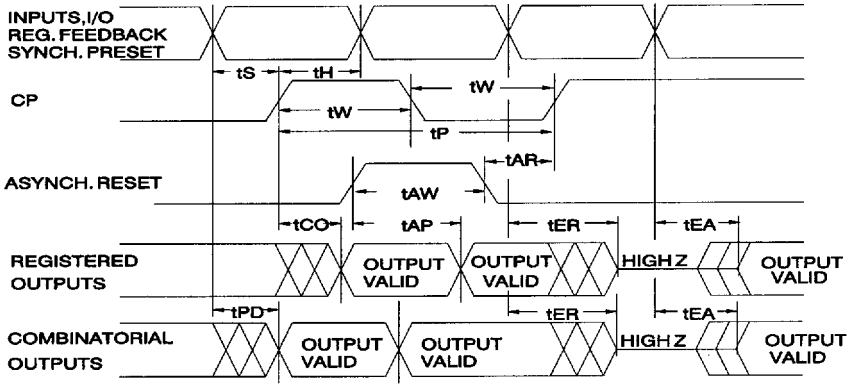
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See I_{CC} vs. Frequency curves in the back of this data sheet.

A.C. Characteristics, Commercial and Industrial

		AT22V10-15			AT22V10/L-20			AT22V10/L-25			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25	ns
t_{EA}	Input to Output Enable		10	15			20		15	25	ns
t_{ER}	Input to Output Disable		10	15			20		15	25	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	ns
t_{CO}	Clock to Output	0	7	10	0	8	12	0	10	15	ns
t_S	Input or Feedback Setup Time	10	8		12	8		15	12		ns
t_H	Hold Time	0			0			0			ns
t_P	Clock Period	12			20			24			ns
t_W	Clock Width	6			10			12			ns
F_{MAX}	External Feedback 1/(t_S+t_{CO})			50.0			41.6			33.3	MHz
	Internal Feedback 1/(t_S + t_{CF})			80.0			50.0			40.0	MHz
	No Feedback 1/(t_P)			83.3			50.0			41.6	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	15	8		20	12		25	15		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25	ns

A.C. Waveforms [1]

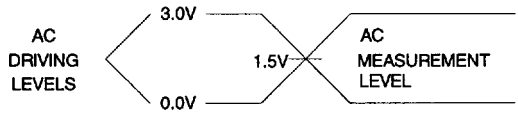


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics, Military

Symbol	Parameter	AT22V10-15			AT22V10/L-20			AT22V10/L-25			AT22V10/L-30			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	30	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	30	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	15	0	10	15	0	12	20	ns
t_{SF}	Feedback Setup Time	10	8		12	10		15	12		18	15		ns
t_S	Input Setup Time	10	8		17	14		18	15		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			31.2			30.3			25.0	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$			80.0			50.0			40.0			30.0	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

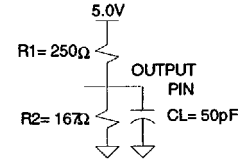
Input Test Waveforms and Measurement Levels



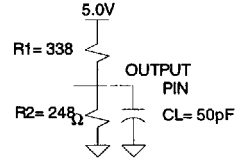
tR, tF < 5 ns (10% to 90%)

Output Test Loads:

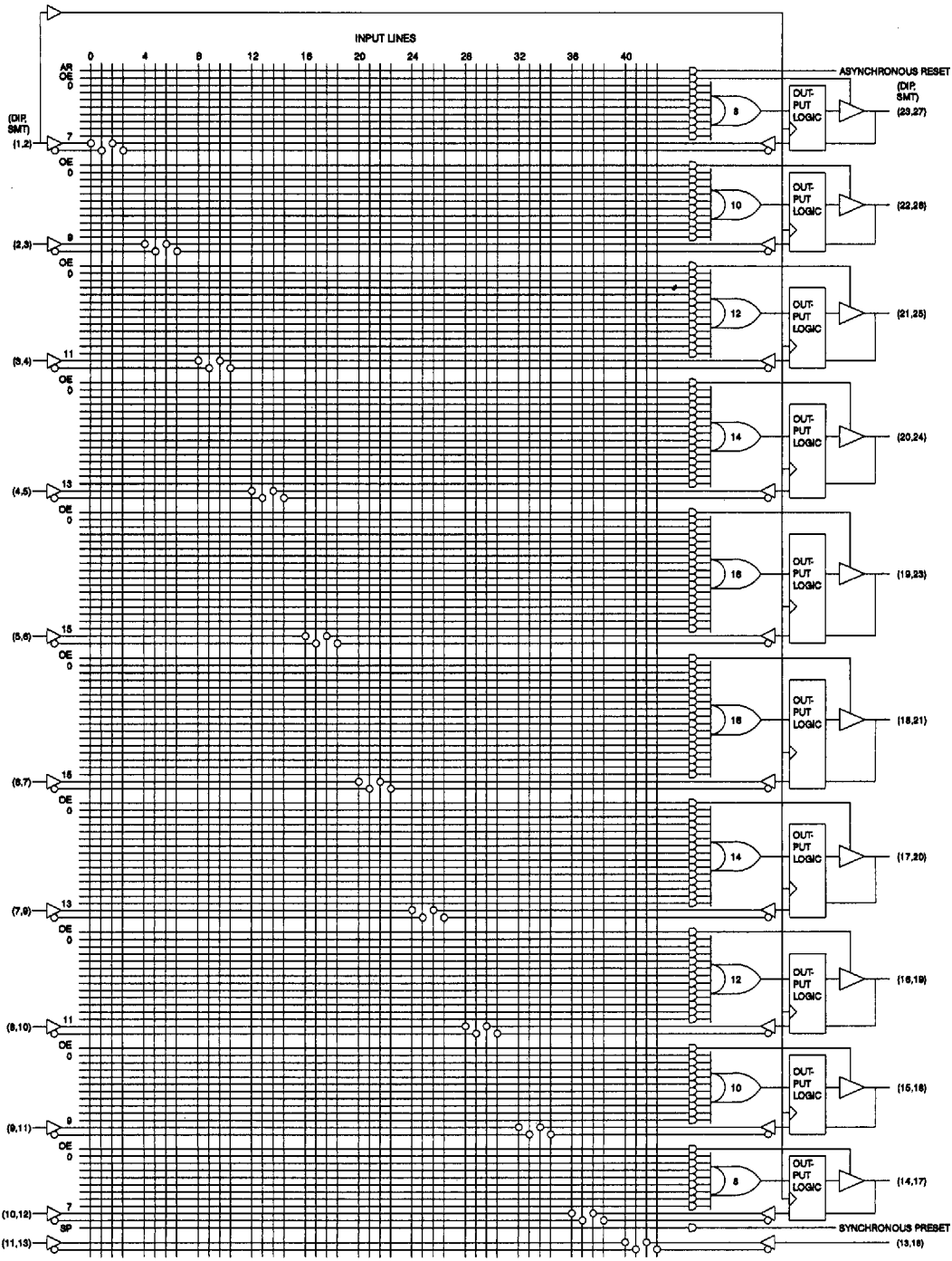
Commercial



Military



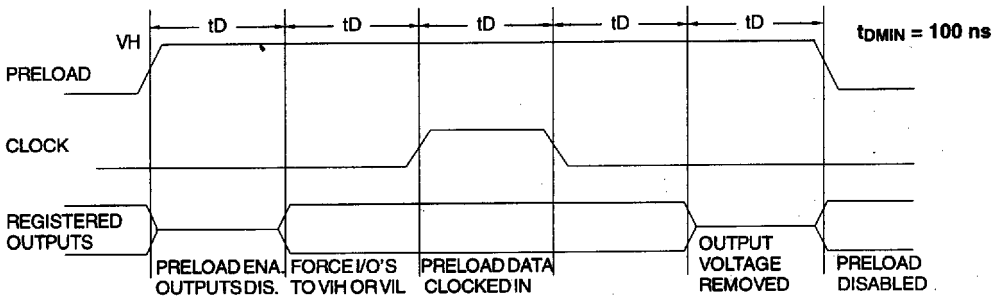
Functional Logic Diagram AT22V10/L



Preload of Registered Outputs

The registers in the AT22V10 and AT22V10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5-V to 13-V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during preload cycle	Register state after cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

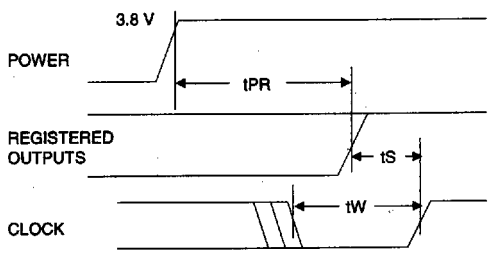
The registers in the AT22V10 and AT22V10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

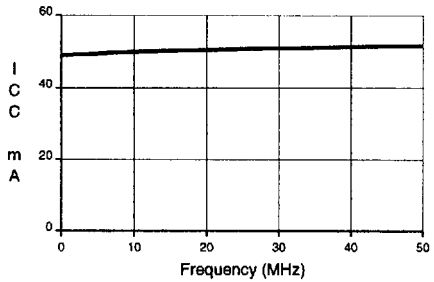
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10 or AT22V10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

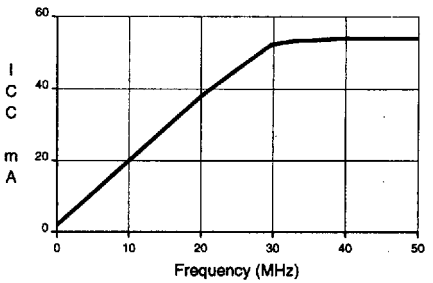
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10 (TA = 25C, VCC = 5V)

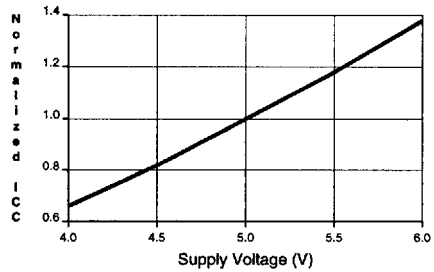


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10L (TA = 25C, VCC = 5V)

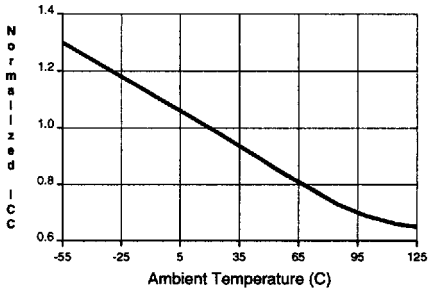


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



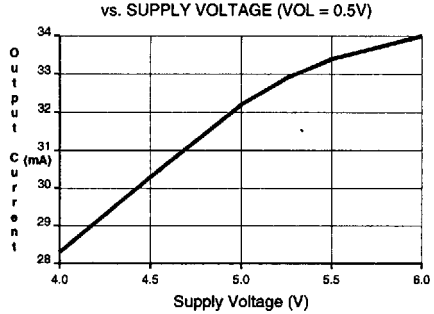
NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz



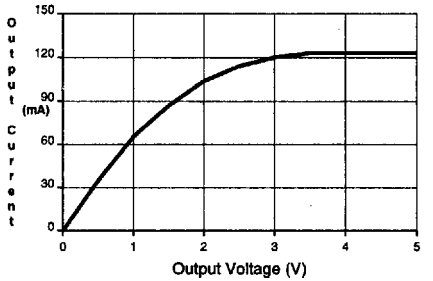
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



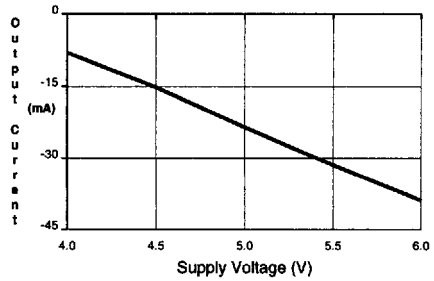
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



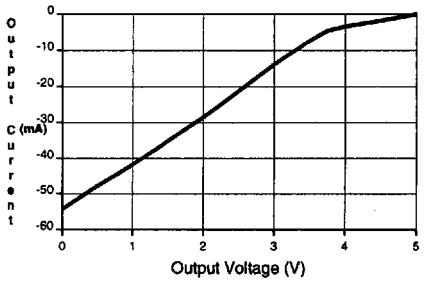
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

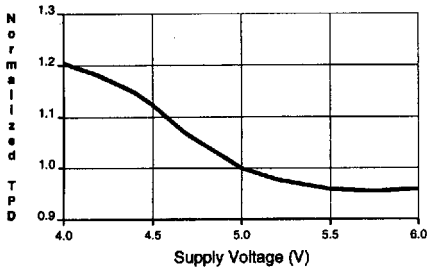


OUTPUT SOURCE CURRENT

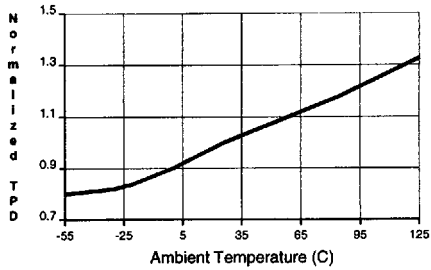
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



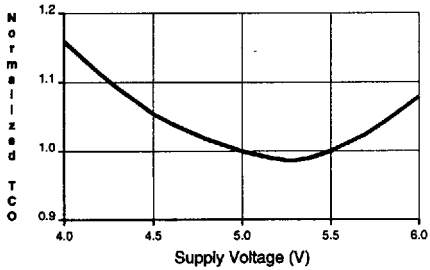
NORMALIZED TPD vs. SUPPLY VOLTAGE



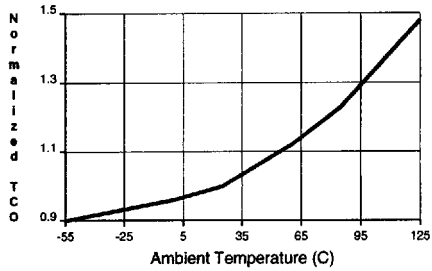
NORMALIZED TPD vs. TEMPERATURE



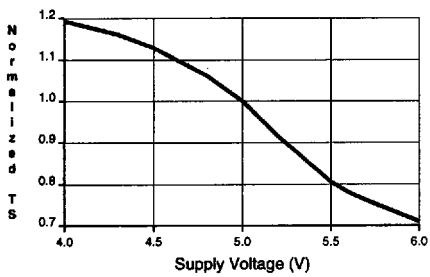
NORMALIZED TCO vs. SUPPLY VOLTAGE



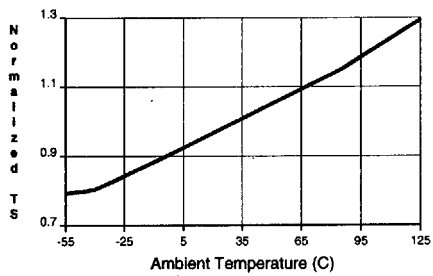
NORMALIZED TCO vs. TEMPERATURE



NORMALIZED TS vs. SUPPLY VOLTAGE

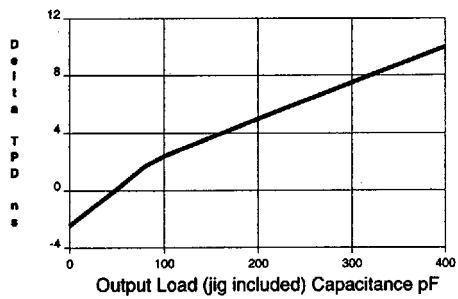


NORMALIZED TS vs. TEMPERATURE



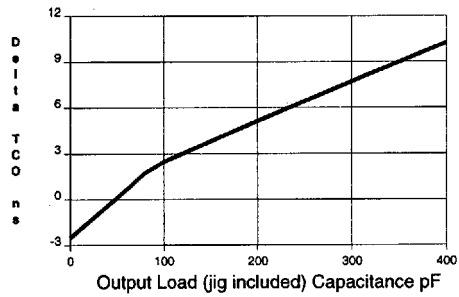
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	10	AT22V10-15DC AT22V10-15GC AT22V10-15JC AT22V10-15PC AT22V10-15SC	24DW3 24D3 28J 24P3 24S	Military/883C Commercial (0°C to 70°C)
			AT22V10-15DI AT22V10-15GI AT22V10-15JI AT22V10-15PI AT22V10-15SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22V10-15DM AT22V10-15GM AT22V10-15LM AT22V10-15NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10-15DM/883 AT22V10-15GM/883 AT22V10-15LM/883 AT22V10-15NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10-25DC AT22V10-25GC AT22V10-25JC AT22V10-25PC AT22V10-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10-25DI AT22V10-25GI AT22V10-25JI AT22V10-25PI AT22V10-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
25	18	15	AT22V10-25DM AT22V10-25GM AT22V10-25LM AT22V10-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10-25DM/883 AT22V10-25GM/883 AT22V10-25LM/883 AT22V10-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-87539 01 LA 5962-87539 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	10	5962-87539 05 LA 5962-87539 05 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	10	5962-88670 05 LA 5962-88670 05 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88670 01 LA 5962-88670 01 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	12	15	AT22V10L-20DC AT22V10L-20GC AT22V10L-20JC AT22V10L-20PC AT22V10L-20SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10L-20DI AT22V10L-20GI AT22V10L-20JI AT22V10L-20PI AT22V10L-20SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
20	17	15	AT22V10L-20DM AT22V10L-20GM AT22V10L-20LM AT22V10L-20NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10L-20DM/883 AT22V10L-20GM/883 AT22V10L-20LM/883 AT22V10L-20NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10L-25DC AT22V10L-25GC AT22V10L-25JC AT22V10L-25PC AT22V10L-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10L-25DI AT22V10L-25GI AT22V10L-25JI AT22V10L-25PI AT22V10L-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
25	18	15	AT22V10L-25DM AT22V10L-25GM AT22V10L-25LM AT22V10L-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10L-25DM/883 AT22V10L-25GM/883 AT22V10L-25LM/883 AT22V10L-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-88724 04 LA 5962-88724 04 3X	24DW3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88724 01 LA 5962-88724 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-89755 04 LA 5962-89755 04 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-89755 01 LA 5962-89755 01 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

5 **CERTIFICATE OF CONFORMITY**

All batches of parts shall be supplied with certificates of conformity. The certificate of conformity shall reference the test certificate.

5.1 **FT Cof C**

Screening specified in section 4 of this document.
Force Technologies part number.

6 **PACKAGE DESCRIPTION**

Package: as ordered
Pin-out: As Atmel data sheet
Finish: Hot Tined dip Mil-Prf-38534 Appendix E or Pb free(LF).

6.1 **MARKING**

Part number (will exclude die manufacturer if space limited)
Date Code-As tested
Batch Code-As assembled
FT Logo

7 **TRACEABILITY (IF APPLICABLE)**

Traceability shall be provided by the date code printed on the top/bottom side of each device.
ISO9002 traceability procedures to apply using batch codes

8 **COMPONENT SELECTION**

8.1 **General**

No component or component supplier shall be changed without the express written consent of the customer(s), following the submission of evidence to justify that the replacement component will meet all required parameters, including radiation immunity.

8.2 Nuclear Hardness (Not applicable)

8.3 The baseline component:

Original Manufacturer:	Manu:Atmel
Part number:	P/N:AT22V10W

The vendor shall determine that the die size, mask and if possible the manufacturing process has not changed since the manufacture of the baseline component. This shall be done prior to acceptance of any order by the vendor. If such a change has occurred, written notification shall be given to the customer the changes and possible alternatives. The vendor shall take no further action until a way forward has been agreed with the customer.

8.4 **Obsolescence**

Upon acceptance of an order the vendor becomes responsible for all component obsolescence until completion of that order. The vendor will inform customer of any PCN.

Ashley Crt, Henley,
Marlborough, Wilts, SN8 3RH
Tel: +44(0)1264 731200
Fax:+44(0)1264 731444
E-mail
info@forcetechnologies.co.uk
tech@forcetechnologies.co.uk
sales@forcetechnologies.co.uk
www.forcetechnologies.co.uk