

DATA SHEET

74F280B

9-bit odd/even parity generator/checker

Product specification

1996 Mar 12

IC15 Data Handbook

9-bit odd/even parity generator/checker

74F280B

FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in Low and High states)
- Buffered inputs — one normalized load
- Word length easily expanded by cascading
- Industrial temperature range available (−40°C to +85°C)

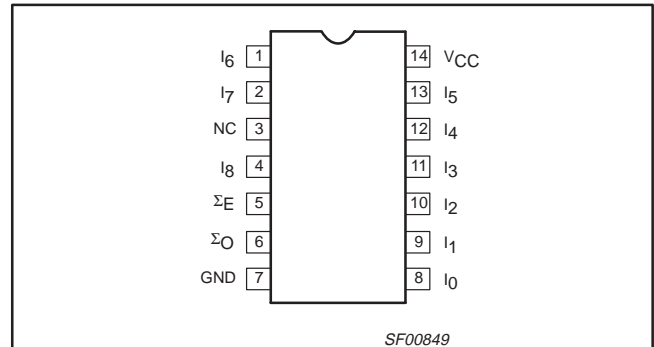
DESCRIPTION

The 74F280B is a 9-bit Parity Generator or Checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even (Σ_E) and Odd (Σ_O) parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even (Σ_E) parity output is High when an even number of Data inputs ($I_0 - I_8$) are High. The Odd (Σ_O) parity output is High when an odd number of Data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even (Σ_E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20ns.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280B	5.5ns	26mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C \text{ to } +70^\circ C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^\circ C \text{ to } +85^\circ C$	PKG. DWG. #
14-pin plastic DIP	N74F280BN	I74F280BN	SOT27-1
14-pin plastic SO	N74F280BD	I74F280BD	SOT108-1

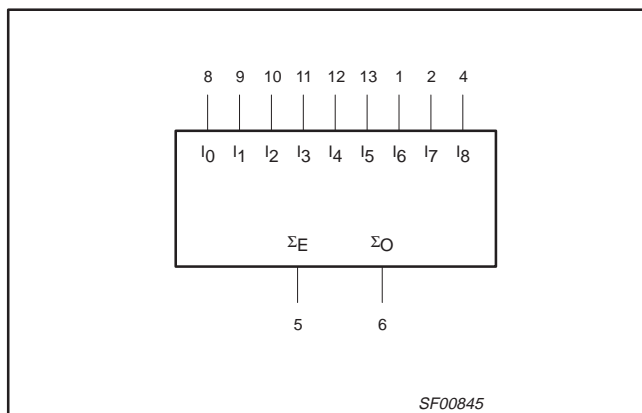
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_0 - I_8$	Data inputs	1.0/0.033	20µA/20µA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

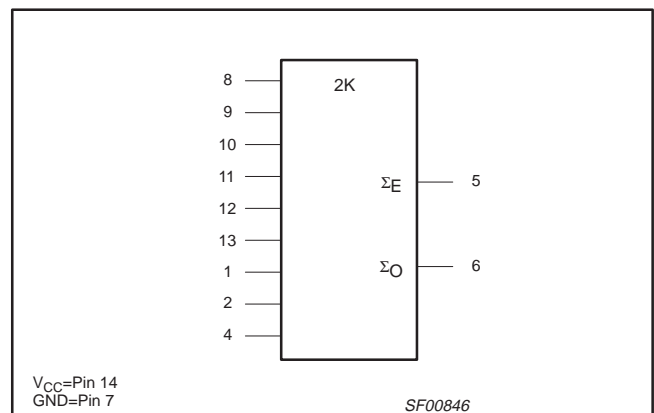
NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



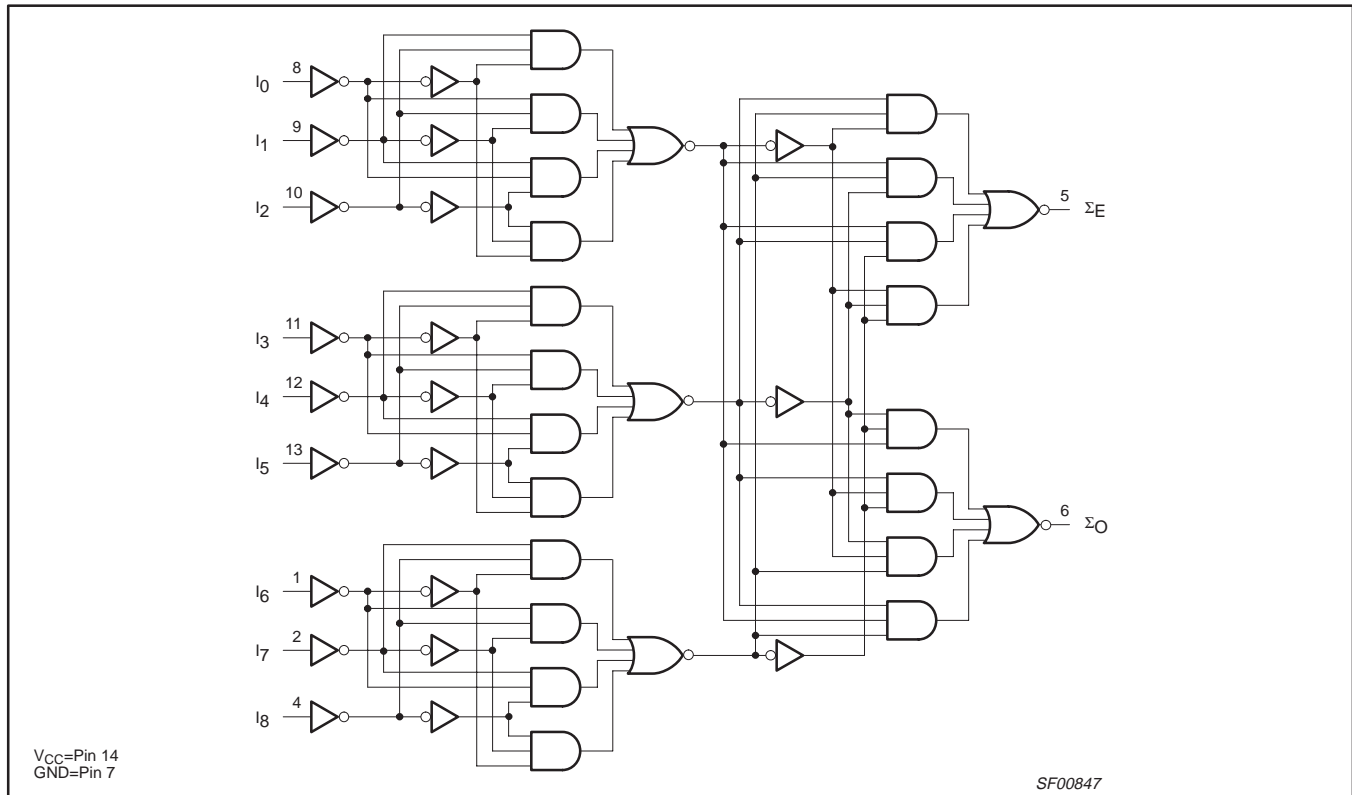
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
	Σ_E	Σ_O
Number of High Data Inputs ($I_0 - I_8$)		
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{stg}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0	70	°C
		Industrial range	-40	85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.4	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.35	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = 0.0V, V_I = 7.0V$			100	μA
I_{IH}	High-level input current	Commercial range	$V_{CC} = \text{MAX}, V_I = 2.7V$		20	μA
		Industrial range			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-20	μA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-60	-150	mA
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$		26	35	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

9-bit odd/even parity generator/checker

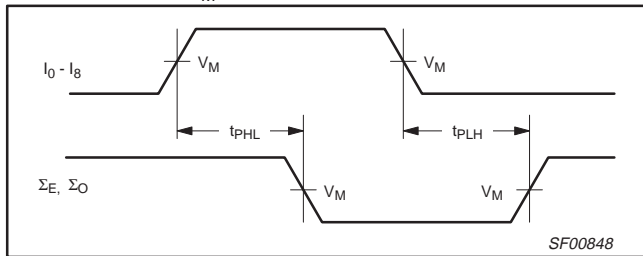
74F280B

AC ELECTRICAL CHARACTERISTICS

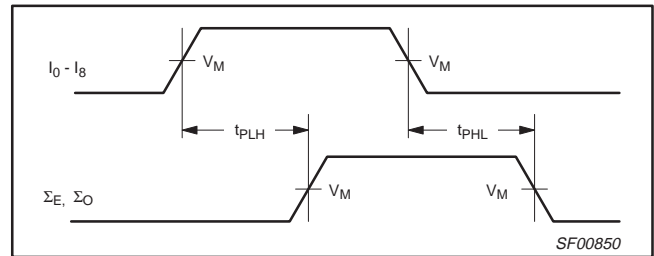
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS								UNIT	
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$				
			Min	Typ	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_E	74F280B	Waveform 1, 2		4.0	6.5	9.0	3.5	10.0	3.0	11.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_0 - I_8$ to Σ_O		Waveform 1, 2		4.0	6.5	9.0	3.5	11.0	3.5	12.0	ns

AC WAVEFORMS

For all waveforms, $V_M = 1.5\text{V}$.



Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM

Test Circuit for Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

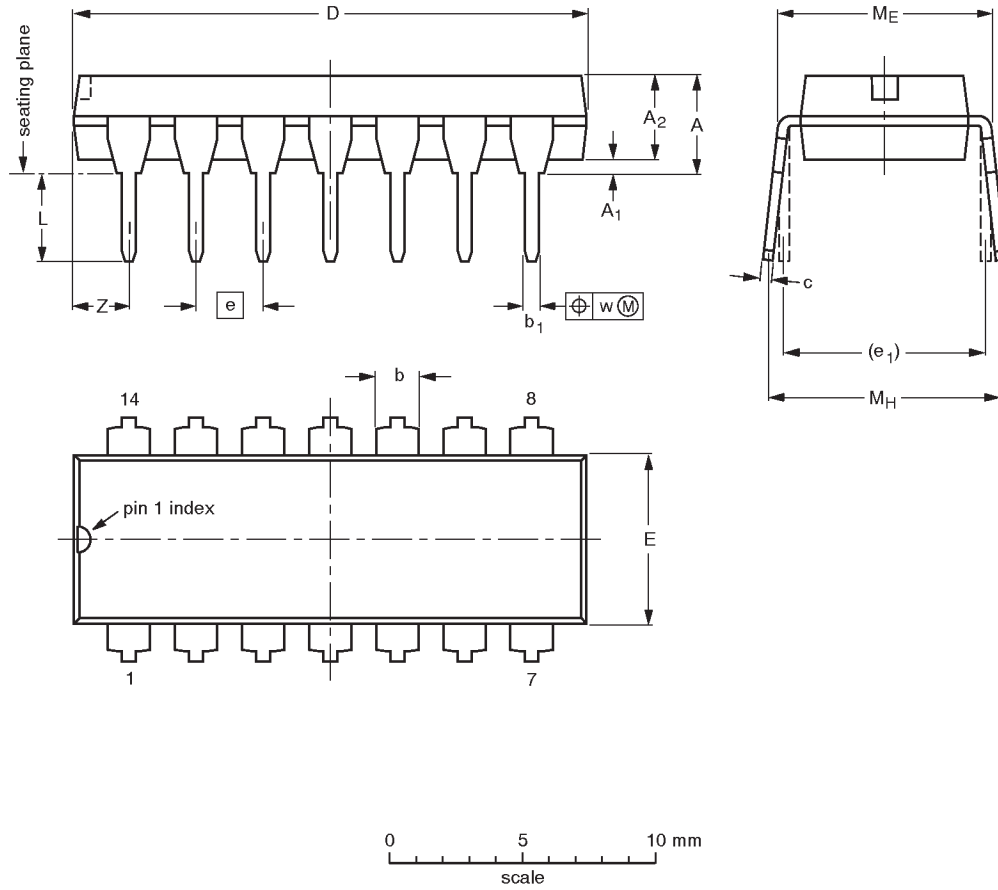
SF00006

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

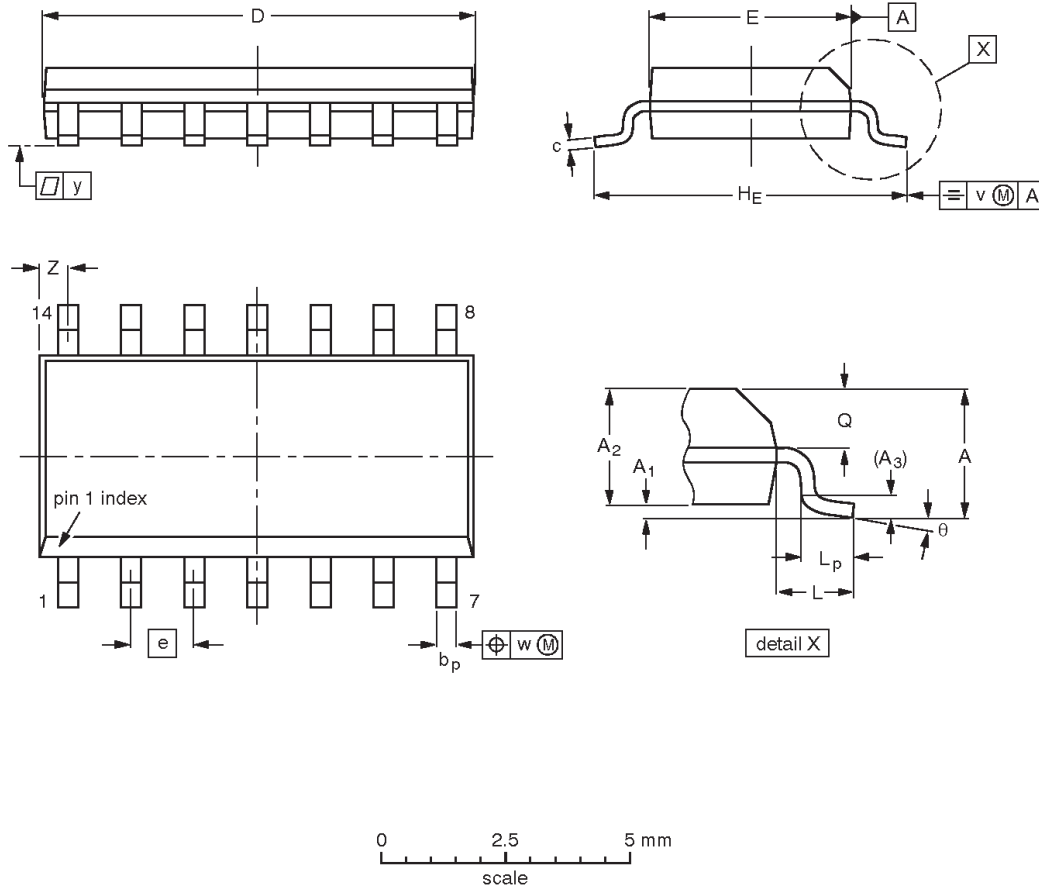
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

9-bit parity odd/even parity generator/checker

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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General description

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The Even (Σ_E) parity output is High when an even number of Data inputs ($I_0 - I_8$) are High. The Odd (Σ_O) parity output is High when an odd number of Data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even (Σ_E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20ns.

Features

- High-impedance NPN base inputs for reduced loading (20µA in Low and High states)
- Buffered inputs - one normalized load
- Word length easily expanded by cascading
- Industrial temperature range available (-40°C to +85°C)

Applications

-  [AN202_1: Testing and specifying FAST logic](#) (date 01-Jun-87)
-  [AN2021_1: Thermal considerations for FAST logic products](#) (date 13-Mar-95)
-  [AN203_2: Test Fixtures for High Speed Logic](#) (date 02-Apr-98)
-  [AN216_2: Arbitration in shared resource systems](#) (date 18-Jul-88)

❑ Datasheet

<u>Type number</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74F280B	9-bit odd/even parity generator/checker	3/12/1996	Product specification	8	90	Download

❑ Blockdiagram(s)

Block diagram of N74F280BN

❑ Parametrics

<u>Type number</u>	<u>Package</u>	<u>Description</u>	<u>Propagation Delay(ns)</u>	<u>Voltage</u>	<u>No. of Pins</u>	<u>Power Dissipation Considerations</u>	<u>Logic Switching Levels</u>	<u>Output Drive Capability</u>
I74F280BD	SOT108-1 (SO14)	9-Bit Odd/Even Parity Generator/Checker	10~15	5 Volts +	14	None	TTL	Low
I74F280BN	SOT27-1 (DIP14)	9-Bit Odd/Even Parity Generator/Checker	10~15	5 Volts +	14	None	TTL	Low
N74F280BD	SOT108-1 (SO14)	9-Bit Odd/Even Parity Generator/Checker	10~15	5 Volts +	14	None	TTL	Low
N74F280BN	SOT27-1 (DIP14)	9-Bit Odd/Even Parity Generator/Checker	10~15	5 Volts +	14	None	TTL	Low

❑ Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u> Discretes packing info	<u>Package</u>	<u>Device status</u>	<u>Buy online</u>
I74F280BD	I74F280BD	9350 295 20602	Standard Marking * Tube (Signetics)	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
	I74F280B D	9350 295 20623	Standard Marking * Reel Pack, SMD, 13" (Signetics)	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
I74F280BN	I74F280BN	9350 295 30602	Standard Marking * Tube (Signetics)	SOT27-1 (DIP14)	Full production	order this <input type="checkbox"/>
N74F280BD	N74F280BD	9338 290 10602	Standard Marking * Tube (Signetics)	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>

	N74F280BD-T	9338 290 10623	Standard Marking * Reel Pack, SMD, 13" (Signetics)	SOT108-1 (SO14)	Full production	order this <input type="checkbox"/>
N74F280BN	N74F280BN	9338 290 00602	Standard Marking * Tube (Signetics)	SOT27-1 (DIP14)	Full production	order this <input type="checkbox"/>

Products in the above table are all in production. Some variants are discontinued; [click here](#) for information on these variants.

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