PaceMips™ PR3010A FPA 32-BIT RISC CO-PROCESSOR (FLOATING POINT ACCELERATOR)

1

FEATURES

- **32-BIT RISC Co-Processor:**
  - **Contains thirty-two 32-bit registers or sixteen 64-bit registers to support Single-Precision or Double-Precision Arithmetic**
- **Fully conforms to requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating Point Arithmetic"**
- **Compatible with the MIPS R3010 RISC Co-Processor**
- **Comprehensive System Development Support**
- **Military Product Compliant to MIL-STD-883C, Class B**
- **Tightly-coupled interface with the PaceMips R3000A increases system performance:**
  - **11.36 MFLOPS @ 40MHz for single precision**
  - **6.56 MFLOPS @ 40MHz for double precision arithmetic when used with the PaceMips PR3000A RISC Processor (Floating Point Operations for LINPACK Benchmark)**
- **Available Packages:**
  - **84-Pin Ceramic Quad Flat Pack/J-Bend**
  - **84-Pin Ceramic Pin-Grid-Array**
  - **84-Pin Ceramic Quad Flat Pack/Straight Lead**
  - **160-Pin Metal Quad Flat Pack**
- **Produced with PACE III Technology™**

DESCRIPTION

The PaceMips PR3010A Co-Processor is a floating point accelerator that operates in conjunction with the PaceMips PR3000A Processor and fully supports the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating Point Arithmetic."

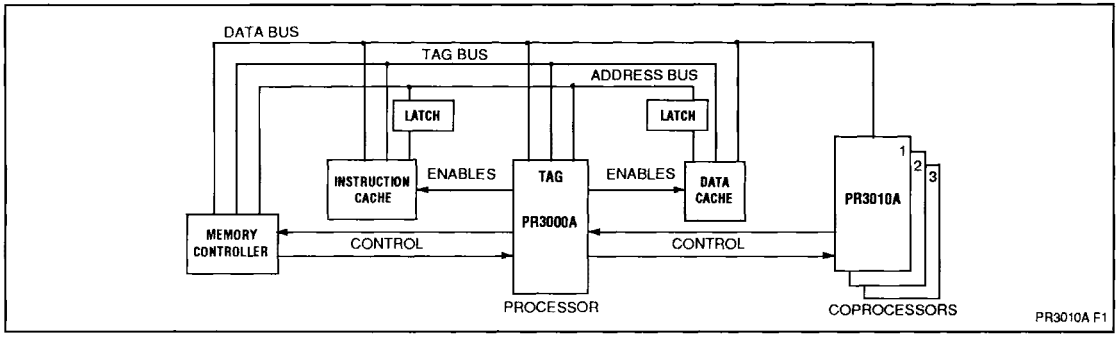
Like the PaceMips PR3000A, the PR3010A uses the LOAD/STORE architecture to increase system performance. In a LOAD/STORE architecture all operations are carried out on operands contained in the processor registers, and only the load and store instructions can access the main memory system. Included in the PR3010A there are sixteen 64-bit registers that can be used to store both single and double-precision values. All IEEE-Standard exception handling requirements are supported by a 32-bit status/control register.

The PaceMips PR3010A Co-Processor is manufactured using PACE III Technology which is Performance Advanced CMOS Engineered to use 0.6 micron effective channel lengths resulting in 250 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

The PaceMips PR3010A Co-Processor is available in an 84-pin Ceramic Quad Flat Pack/J-Bend, 84-pin Ceramic Pin Grid Array, 84-pin Ceramic Quad Flat Pack/Straight Lead and a 84-pin Plastic Leaded Chip Carrier.

* For a fan-in/fan-out of a 4 at 85°C junction temperature and 5.0 V supply.

PROCESSOR SYSTEM BLOCK DIAGRAM



PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

1.0 SIGNAL DESCRIPTIONS

Data(31:0)	I/O	A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.
DataP(3:0)	O	A 4-bit bus containing even parity over the data bus. Parity is generated by the FPA on stores.
$\overline{\text{Run}}$	I	Input to the FPA which indicates whether the processor-coprocessor system is in the run or stall state.
$\overline{\text{Exception}}$	I	Input to the FPA which indicates exception related status information.
FpBusy	O	Signal to the CPU indicating a request for a coprocessor busy stall.
FpCond	O	Signal to the CPU indicating the result of the last comparison operation.
$\overline{\text{FpInt}}$	O	Signal to the CPU indicating that a floating-point exception has occured for the current FPA instruction.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to distinguish the processor-FPA synchronization period from the execution period. $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$ from the CPU.
$\overline{\text{PllOn}}$	I	Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.
$\overline{\text{FpPresent}}$	O	Output which is pulled to ground through an internal impedance of approximately 0.5k ohms. By providing an external pullup on this line an indication of the presence or absence of the FPA can be obtained.
Clk2xSys	I	A double frequency clock input used for generating $\overline{\text{FpSysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the FPA.
Clk2xRd	I	A double frequency clock input used to determine the disable point for the data drivers.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2.
$\overline{\text{FpSysOut}}$	O	Synchronization clock from the FPA.
$\overline{\text{FpSysIn}}$	I	Input used to receive the synchronization clock from the FPA.
$\overline{\text{FpSync}}$	I	Input used to receive the synchronization clock from the CPU.

2.0 ELECTRICAL SPECIFICATIONS, COMMERCIAL TEMPERATURE RANGE (T = 0°C TO 70°C, V = 5V±5%)

2.1 MAXIMUM RATINGS[3]

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	Input Voltage[1,2]		-0.5	+7.0	V

Notes:
1. V_{IN} Min. = -3.0V for pulse width less than 15ns.
2. $V_{in} \leq V_{CC} + 0.5$
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

2.2 RECOMMENDED OPERATING CONDITIONS [1,2&3]

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 5%

Notes:
1. The case temperature must be limited by using adequate air flow and/or an appropriate heat sink or other thermal management design.
2. The maximum operating junction temperature should be limited to 125°C.
3. For optimum performance and improved reliability, it is recommended that the operating junction temperature should be kept below 85°C.

2.3 CAPACITIVE LOAD DERATING FACTOR

Sym.	Parameter	Conditions	20MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
C_{LD}	Load Derate		0.5	1	0.5	1	0.5	1	0.5	1	ns/25pF

2.4 DC ELECTRICAL CHARACTERISTICS

Sym.	Parameter	Conditions	20MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = -4mA	3.5		3.5		3.5	3.5			V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 4mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC}+ 0.5	2	V_{CC}+ 0.5	2	V_{CC}+ 0.5	2	V_{CC}+ 0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V_{IHS}	Input HIGH Voltage[2]		3.0	V_{CC}+ 0.5	3.0	V_{CC}+ 0.5	3.0	V_{CC}+ 0.5	3.0	V_{CC}+ 0.5	V
V_{ILS}	Input LOW Voltage[2]		-0.5	0.4	-0.5	0.4	-0.5	0.4	-0.5	0.4	V
V_{IHC}	Input HIGH Voltage[3]		4.0	V_{CC}+ 0.5	4.0	V_{CC}+ 0.5	4.0	V_{CC}+ 0.5	4.0	V_{CC}+ 0.5	V
V_{ILC}	Input LOW Voltage[3]		-0.5	0.4	-0.5	0.4	-0.5	0.4	-0.5	0.4	V
C_{IN}	Input Capacitance			10		10		10		110	pF
C_{OUT}	Output Capacitance			10		10		10		10	pF
I_{CC}	Operating Current	V_{CC} = Max.		325		400		425		525	mA
C_{Ld}	Load Capacitance			25		25		25		25	pF

Notes:
1. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively are permissible for pulse widths up to 15ns.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2Phi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.

2.5 AC ELECTRICAL CHARACTERISTICS, COMMERCIAL TEMPERATURE RANGE [1,2,3] (T = 0°C TO 70°C, V = 5V±5%)

Symbol	Parameter	Conditions	20MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
$T_{ClkHigh}$	Input Clock High	Transition≤5ns	10		8		6		5		ns
T_{ClkLow}	Input Clock Low	Transition≤5ns	10		8		6		5		ns
T_{ClkP}	Input Clock Period		25	125	20	100	15	75	12.5	60	ns
	Clk2xSys to Clk2xSmp		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xRd		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xPhi		7	$t_{Cyc/4}$	5	$t_{Cyc/4}$	4.0	$t_{Cyc/4}$	3.0	$t_{Cyc/4}$	ns
T_{DEn}	Data Enable			-2		-1.5		-1		-1	ns
T_{DDis}	Data Disable		0	-1	0	-0.5	0	-0.5		-0.5	ns
T_{DVal}	Data Valid		2	3	1	2		2		1.5	ns
T_{DS}	Data Setup		8		6		5		4		ns
T_{DH}	Data Hold		-2.5		-2.5		-1.5		-1.5		ns
T_{FpCond}	Fp Condition		0	30	0	25	0	19	0	15	ns
T_{FpBusy}	Fp Busy		0	13	0	10	0	7	0	5	ns
T_{Fpint}	Fp Interrupt		0	30	0	25	0	19	0	15	ns
T_{FpMov}	Fp Move To		0	30	0	25	0	19	0	15	ns
T_{ExS}	Exception Setup	Run	9		7		7.5		7		ns
T_{ExS}	Exception Setup	Stall	9		7		5.5		5		ns
T_{ExH}	Exception Hold		0		0		0		0		ns
T_{RunS}	Run Setup		9		7		7		5		ns
T_{RunH}	Run Hold		-2		-2		-1.5		-1.5		ns

Notes:
1. All output times are given assuming 25pF of capacitive load.
2. All timings referenced to 1.5V.
3. The clock parameters apply to all four 2x Clocks.

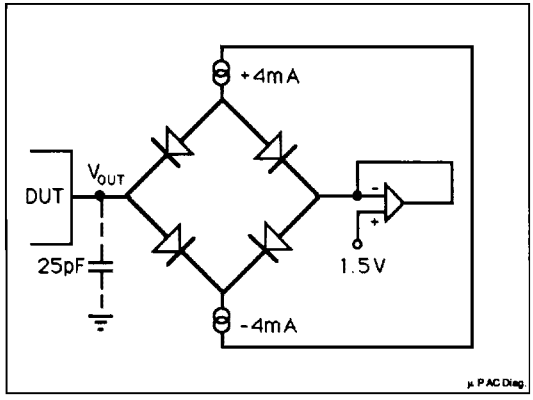


Figure 2.5.1 Output Loading for AC Testing

3.0 ELECTRICAL SPECIFICATIONS, MILITARY TEMPERATURE RANGE (T = 0°C TO 125°C, V = 5V±10%)

3.1 MAXIMUM RATINGS[3]

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	Input Voltage[1,2]		-0.5	+7.0	V

Notes:
1. V_{IN} Min. = -3.0V for pulse width less than 15ns.
2. $V_{in} \leq V_{CC} + 0.5$
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

3.2 RECOMMENDED OPERATING CONDITIONS [1,2&3]

Grade	Case Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0V ± 10%

Notes:
1. The case temperature must be limited by using adequate air flow and/or an appropriate heat sink or other thermal management design.
2. The maximum operating junction temperature should be limited to 125°C.
3. For optimum performance and improved reliability, it is recommended that the operating junction temperature should be kept below 85°C.

3.3 CAPACITIVE LOAD DERATING FACTOR

Sym.	Parameter	Conditions	20MHz		25MHz		28MHz		33MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
C_{LD}	Load Derate		0.5	1	0.5	1	0.5	1	0.5	1	ns/25pF

3.4 DC ELECTRICAL CHARACTERISTICS

Sym.	Parameter	Conditions	20MHz		25MHz		28MHz		33MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = -4mA	3.5		3.5		3.5		3.5		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 4mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC}+ 0.5	2	V_{CC}+ 0.5	2	V_{CC}+ 0.5	2	V_{CC}+ 0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V_{IHS}	Input HIGH Voltage[2]		3.0	V_{CC}+ 0.5	3.0	V_{CC}+ 0.5	3.0	V_{CC}+ 0.5	3.0	V_{CC}+ 0.5	V
V_{ILS}	Input LOW Voltage[2]		-0.5	0.4	-0.5	0.4	-0.5	0.4	-0.5	0.4	V
V_{IHC}	Input HIGH Voltage[3]		4.0	V_{CC}+ 0.5	4.0	V_{CC}+ 0.5	4.0	V_{CC}+ 0.5	4.0	V_{CC}+ 0.5	V
V_{ILC}	Input LOW Voltage[3]		-0.5	0.4	-0.5	0.4	-0.5	0.4	-0.5	0.4	V
C_{IN}	Input Capacitance			10		10		10		10	pF
C_{OUT}	Output Capacitance			10		10		10		10	pF
I_{CC}	Operating Current	V_{CC} = Max.		325		375		425		475	mA
C_{Ld}	Load Capacitance			25		25		25		25	pF

Notes:
1. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively are permissible for pulse widths up to 15ns.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2Phi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.

3.5 AC ELECTRICAL CHARACTERISTICS, MILITARY TEMPERATURE RANGE [1,2,3] (T = -55°C TO 125°C, V = 5V±10%)

Symbol	Parameter	Conditions	20MHz		25MHz		28MHz		33MHZ		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
$T_{ClkHigh}$	Input Clock High	Transitions≤5ns	10		8				6		ns
T_{ClkLow}	Input Clock Low	Transitions≤5ns	10		8				6		ns
T_{ClkP}	Input Clock Period		25	125	20	100			15	75	ns
	Clk2xSys to Clk2xSmp		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$			0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xRd		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$			0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xPhi		7	$t_{Cyc/4}$	5	$t_{Cyc/4}$			4.0	$t_{Cyc/4}$	ns
T_{DEn}	Data Enable			-2		-1.5				−1	ns
T_{DDis}	Data Disable		0	-1	0	-0.5			0	-0.5	ns
T_{DVal}	Data Valid		2	3	1	2				2	ns
T_{DS}	Data Setup		8		6				5		ns
T_{DH}	Data Hold		-2.5		-2.5				-1.5		ns
T_{FpCond}	Fp Condition		0	30	0	25			0	19	ns
T_{FpBusy}	Fp Busy		0	13	0	10			0	7	ns
T_{Fpint}	Fp Interrupt		0	30	0	25			0	19	ns
T_{FpMov}	Fp Move To		0	30	0	25			0	19	ns
T_{ExS}	Exception Setup	Run	9		7				7.5		ns
T_{ExS}	Exception Setup	Stall	9		7				5.5		ns
T_{ExH}	Exception Hold		0		0				0		ns
T_{RunS}	Run Setup		9		7				7		ns
T_{RunH}	Run Hold		-2		-2				−1.5		ns

Notes:
1. All output times are given assuming 25pF of capacitive load.
2. All timings referenced to 1.5V.
3. The clock parameters apply to all four 2x Clocks.

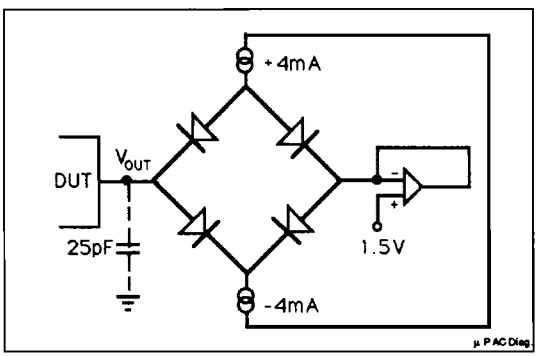


Figure 3.5.1 Output Loading for AC Testing

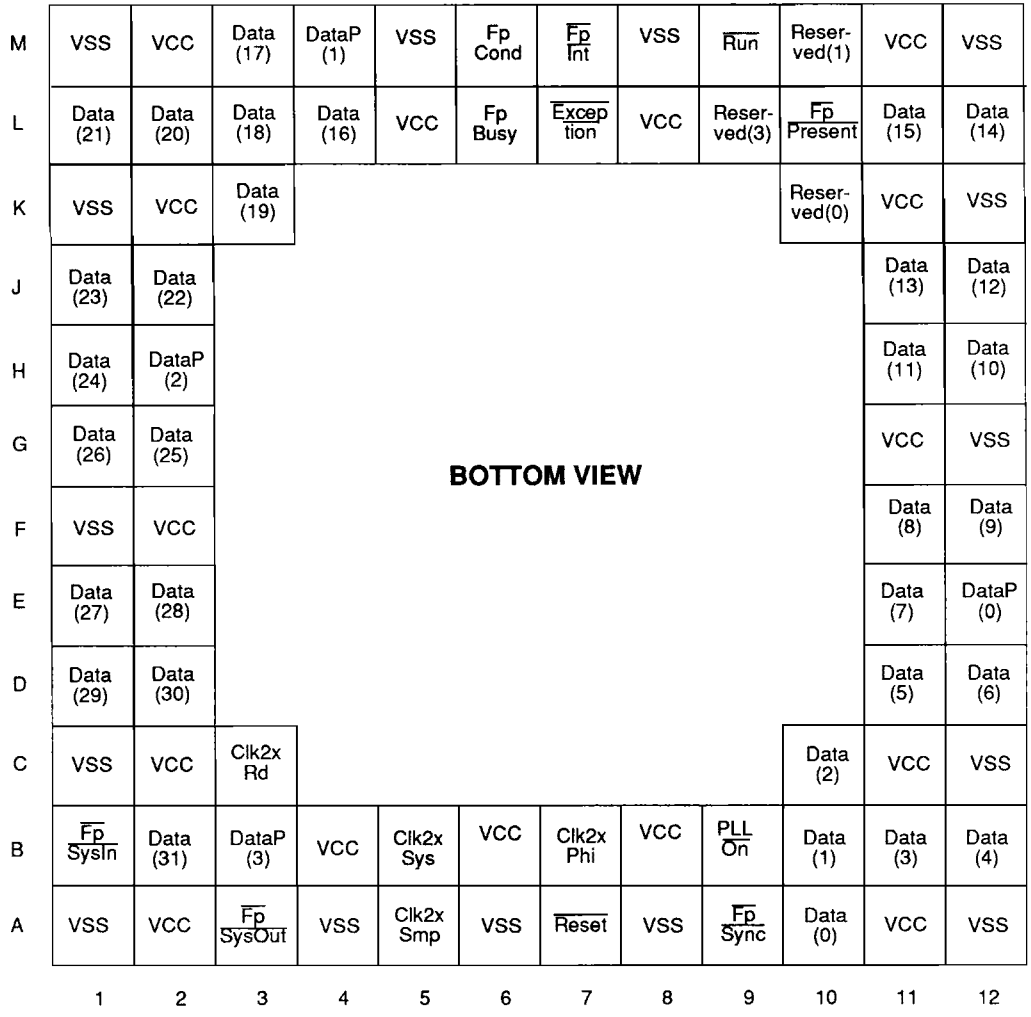
4.0 MECHANICAL DATA — PIN ASSIGNMENTS AND PACKAGE DIMENSIONS

4.1 84-Pin Ceramic Pin-Grid-Array

Table 4.1 PR3010A Pinout — 84-Pin Ceramic Pin Grid Array, Cavity Down

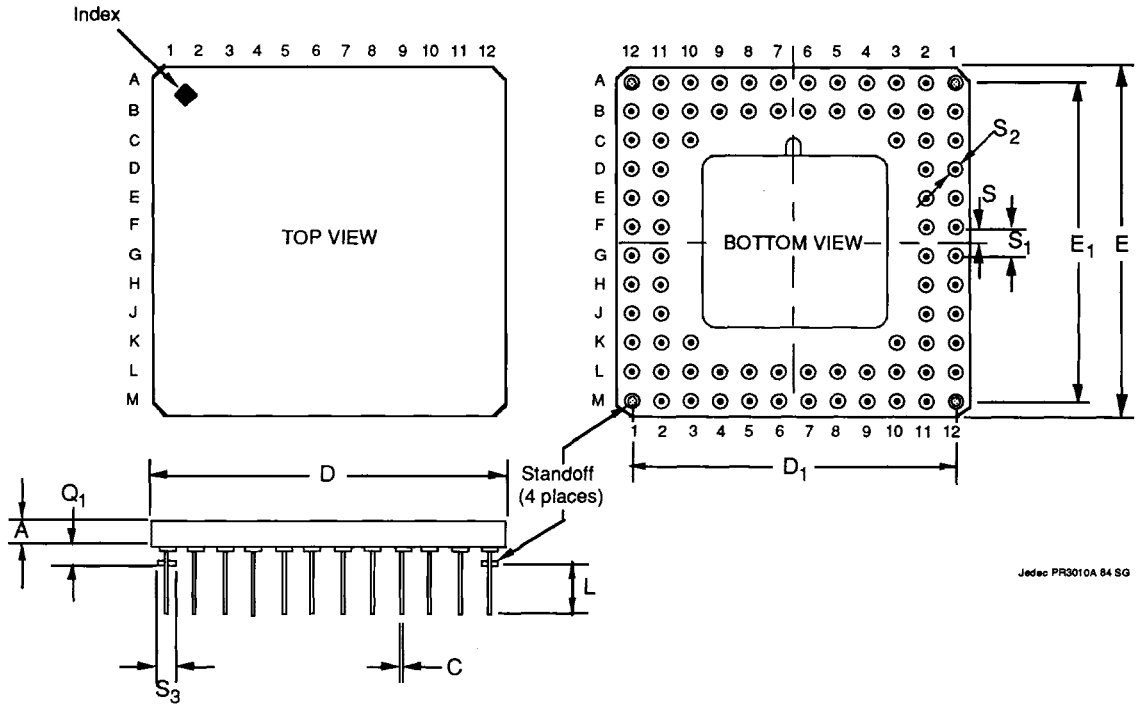
Pin	Designation	Pin	Designation	Pin	Designation
A01	VSS	C11	VCC	K03	Data(19)
A02	VCC	C12	VSS	K10	Reserved(0)
A03	FpSysOut	D01	Data(29)	K11	VCC
A04	VSS	D02	Data(30)	K12	VSS
A05	Clk2xSmp	D11	Data(5)	L01	Data(21)
A06	VSS	D12	Data(6)	L02	Data(20)
A07	Reset	E01	Data(27)	L03	Data(18)
A08	VSS	E02	Data(28)	L04	Data(16)
A09	FpSync	E11	Data(7)	L05	VCC
A10	Data(0)	E12	DataP(0)	L06	FpBusy
A11	VCC	F01	VSS	L07	Exception
A12	VSS	F02	VCC	L08	VCC
B01	FpSysIn	F11	Data(8)	L09	Reserved(2)
B02	Data(31)	F12	Data(9)	L10	FpPresent
B03	DataP(3)	G01	Data(26)	L11	Data(15)
B04	VCC	G02	Data(25)	L12	Data(14)
B05	Clk2xSys	G11	VCC	M01	VSS
B06	VCC	G12	VSS	M02	VCC
B07	Clk2xPhi	H01	Data(24)	M03	Data(17)
B08	VCC	H02	DataP(2)	M04	DataP(1)
B09	PLLOn	H11	Data(11)	M05	VSS
B10	Data(1)	H12	Data(10)	M06	FpCond
B11	Data(3)	J01	Data(23)	M07	FPInt
B12	Data(4)	J02	Data(22)	M08	VSS
C01	VSS	J11	Data(13)	M09	Run
C02	VCC	J12	Data(12)	M10	Reserved(1)
C03	Clk2xRd	K01	VSS	M11	VCC
C10	Data(2)	K02	VCC	M12	VSS

Figure 4.1 PR3010A Pin Diagram — 84-Pin Ceramic Pin Grid Array, Cavity Down



PR3010A 84-SG Pinout

Figure 4.2 PR3010A Package Dimensions — 84-Pin Ceramic Pin Grid Array, Cavity Down



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.060	1,52	0.100	2,54
C	0.013	0,33	0.023	0,58
D/E	1.185	30,0	1.210	30,7
D_1/E_1	1.089	27,65	1.111	28,22
L	0.120	3,05	0.140	3,55
M*	12	12	12	12
N**	84	84	84	84
Q_1	0.050	1,27	0.050	1,27
S	0.050 TYP	1,27 TYP	0.050 TYP	1,27 TYP
S_1	0.100 BSC	2,54 BSC	0.100 BSC	2,54 BSC
S_2	0.055	1,40	0.075	1,90
S_3	0.045	0,11	0.055	0,14

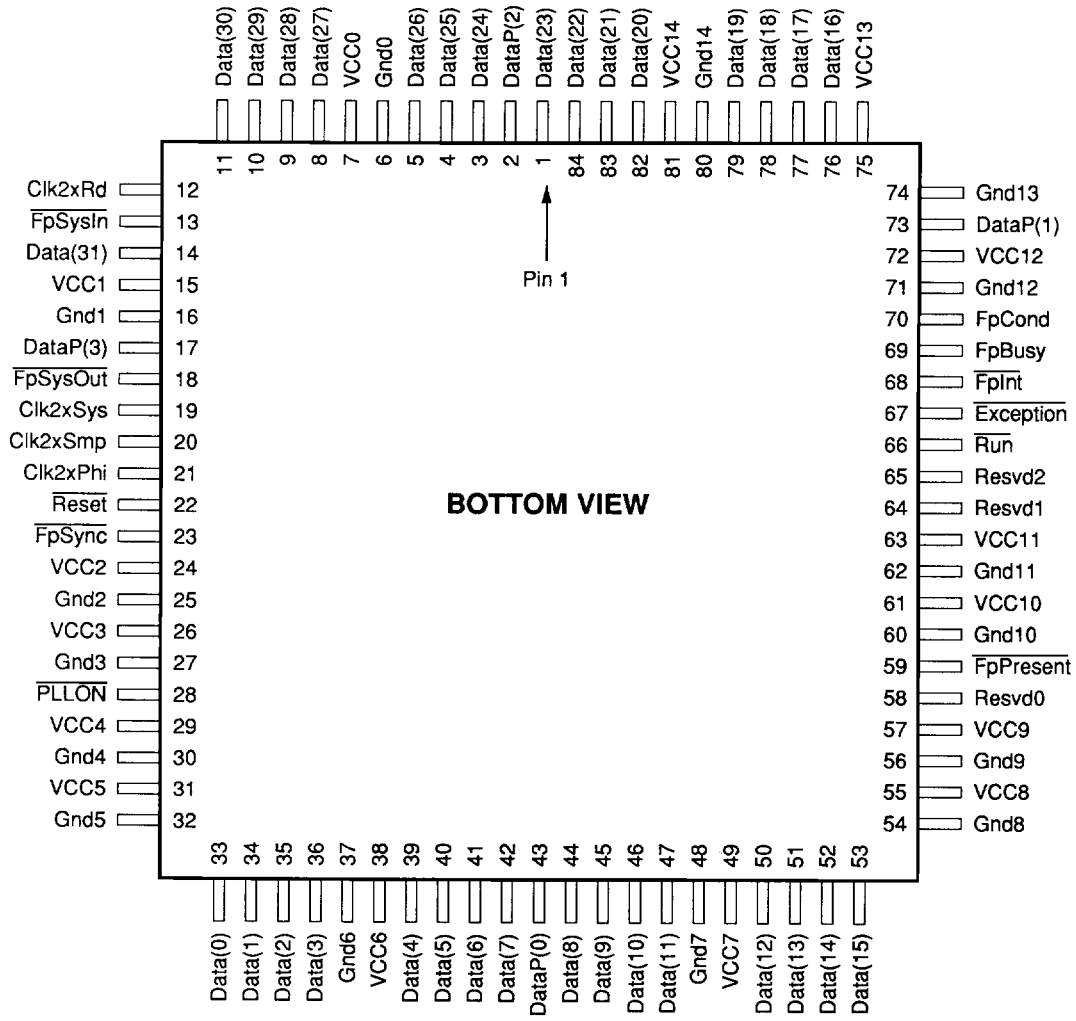
* Typical number of pins per row
** Total number of pins per package
BSC = Basic Spacing between Centers

4.2 84-Pin Ceramic Quad Flat Pack

Table 4.2 PR3010A Pinout — 84-Pin Ceramic Quad Flat Pack Straight Lead, Cavity Down

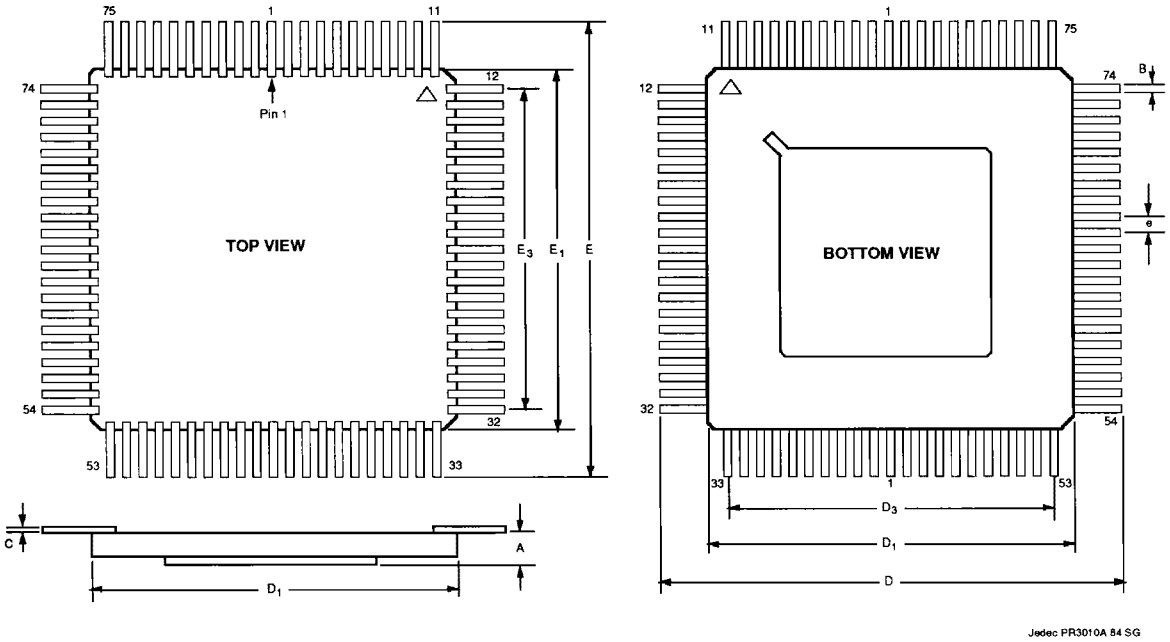
Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	33	$\overline{\text{FpSync}}$	23
Data(1)	34	$\overline{\text{Reset}}$	22
Data(2)	35	$\overline{\text{PllOn}}$	28
Data(3)	36	$\overline{\text{Run}}$	66
Data(4)	39	$\overline{\text{Exception}}$	67
Data(5)	40	$\overline{\text{FpInt}}$	68
Data(6)	41	FpBusy	69
Data(7)	42	$\overline{\text{FpCond}}$	70
Data(8)	44	$\overline{\text{FpFresent}}$	59
Data(9)	45	VCC0	7
Data(10)	46	VCC1	15
Data(11)	47	VCC2	24
Data(12)	50	VCC3	26
Data(13)	51	VCC4	29
Data(14)	52	VCC5	31
Data(15)	53	VCC6	38
Data(16)	76	VCC7	49
Data(17)	77	VCC8	55
Data(18)	78	VCC9	57
Data(19)	79	VCC10	61
Data(20)	82	VCC11	63
Data(21)	83	VCC12	72
Data(22)	84	VCC13	75
Data(23)	1	VCC14	81
Data(24)	3	Gnd0	6
Data(25)	4	Gnd1	16
Data(26)	5	Gnd2	25
Data(27)	8	Gnd3	27
Data(28)	9	Gnd4	30
Data(29)	10	Gnd5	32
Data(30)	11	Gnd6	37
Data(31)	14	Gnd7	48
DataP(0)	43	Gnd8	54
DataP(1)	73	Gnd9	56
DataP(2)	2	Gnd10	60
DataP(3)	17	Gnd11	62
Clk2xSys	19	Gnd12	71
Clk2xSmp	20	Gnd13	74
Clk2xRd	12	Gnd14	80
$\overline{\text{Clk2xPhi}}$	21	Resvd0	58
$\overline{\text{FpSysIn}}$	13	Resvd1	64
$\overline{\text{FpSysOut}}$	18	Resvd2	65

Figure 4.3 PR3010A Pin Diagram — 84-Pin Ceramic Quad Flat Pack Straight Lead, Cavity Down



PR3010A 84-SF Pinout

Figure 4.4 PR3010A Package Dimensions — 84-Pin Ceramic Quad Flat Pack Straight Lead, Cavity Down



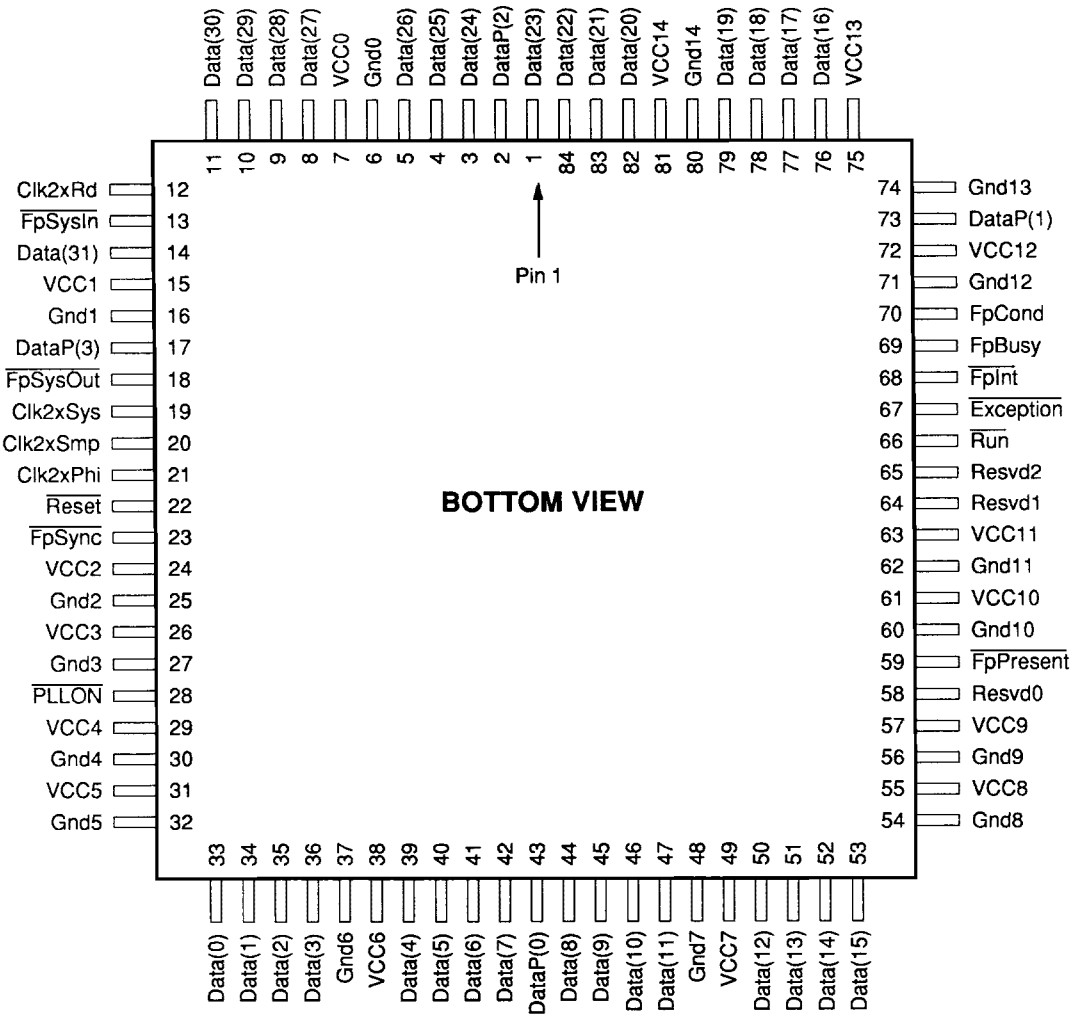
Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.070	1,78	0.090	2,29
B	0.014	0,35	0.022	0,56
C	0.006	0,15	0.010	0,25
D/E	1.760	44,70	1.780	45,21
D_1/E_1	1.140	28,95	1.140	28,95
D_3/E_3	0.990	25,15	1.010	25,65
e	0.25 BSC	0,64	0.25 BSC	0,64

4.3 84-Pin Ceramic Quad Flat Pack

Table 4.3 **PR3010A Pinout — 84-Pin Ceramic Quad Flat Pack J-Bend, Cavity Up**

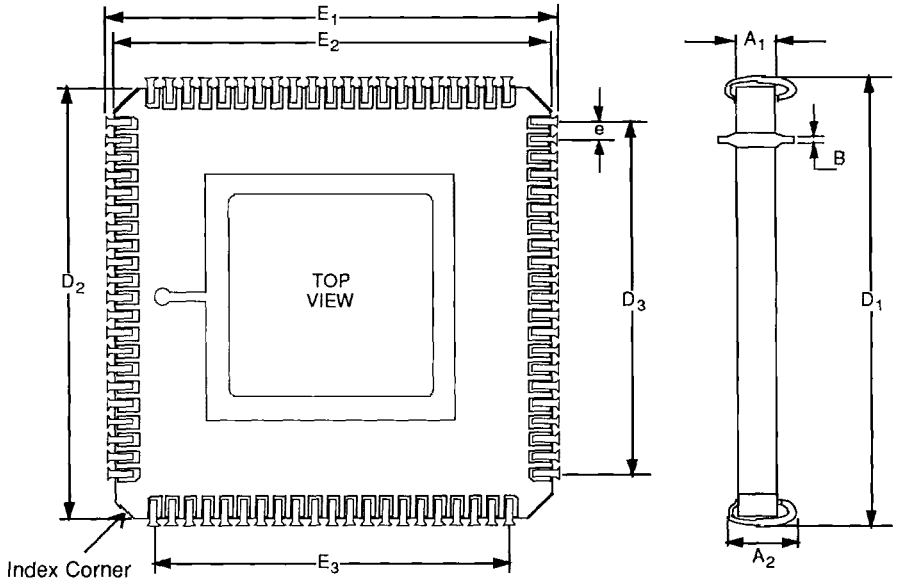
Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	33	$\overline{\text{FpSync}}$	23
Data(1)	34	$\overline{\text{Reset}}$	22
Data(2)	35	$\overline{\text{PllOn}}$	28
Data(3)	36	$\overline{\text{Run}}$	66
Data(4)	39	$\overline{\text{Exception}}$	67
Data(5)	40	$\overline{\text{FpInt}}$	68
Data(6)	41	FpBusy	69
Data(7)	42	$\overline{\text{FpCond}}$	70
Data(8)	44	$\overline{\text{FpFresent}}$	59
Data(9)	45	VCC0	7
Data(10)	46	VCC1	15
Data(11)	47	VCC2	24
Data(12)	50	VCC3	26
Data(13)	51	VCC4	29
Data(14)	52	VCC5	31
Data(15)	53	VCC6	38
Data(16)	76	VCC7	49
Data(17)	77	VCC8	55
Data(18)	78	VCC9	57
Data(19)	79	VCC10	61
Data(20)	82	VCC11	63
Data(21)	83	VCC12	72
Data(22)	84	VCC13	75
Data(23)	1	VCC14	81
Data(24)	3	Gnd0	6
Data(25)	4	Gnd1	16
Data(26)	5	Gnd2	25
Data(27)	8	Gnd3	27
Data(28)	9	Gnd4	30
Data(29)	10	Gnd5	32
Data(30)	11	Gnd6	37
Data(31)	14	Gnd7	48
DataP(0)	43	Gnd8	54
DataP(1)	73	Gnd9	56
DataP(2)	2	Gnd10	60
DataP(3)	17	Gnd11	62
Clk2xSys	19	Gnd12	71
Clk2xSmp	20	Gnd13	74
Clk2xRd	12	Gnd14	80
Clk2xPhi	21	Resvd0	58
$\overline{\text{FpSysIn}}$	13	Resvd1	64
$\overline{\text{FpSysOut}}$	18	Resvd2	65

Figure 4.5 PR3010A Pin Diagram — 84-Pin Ceramic Quad Flat Pack J-Bend, Cavity Up



PR3010A 84-SR Pinout

Figure 4.6 PR3010A Package Dimensions — 84-Pin Ceramic Quad Flat Pack J-Bend, Cavity Up



Jedec PR3010A 84 SR

Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A_1	0.065	1,65	0.075	1,90
A_2	0.110	2,8	0.120	3,0
B	0.018	0,45	0.022	0,55
D_1/E_1	1.185	30,0	1.195	30,5
D_2/E_2	1.140	29,0	1.160	29,5
D_3/E_3	1.000	25,4	1.000	25,4
e	0.050 BSC	1,3 BSC	0.050 BSC	1,3 BSC

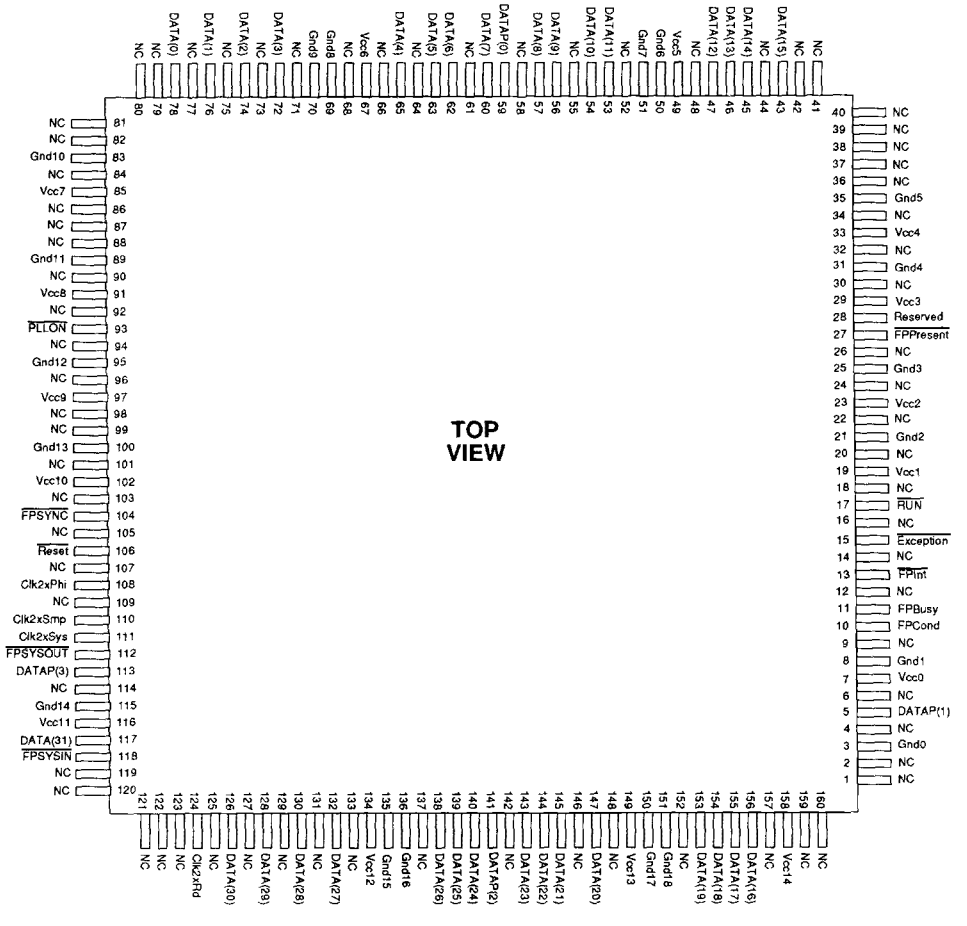
BSC = Basic Spacing between Centers

4.4 160-Pin Metal Quad Flat Pack

Table 4.4 PR3010A Pinout — 160-Pin Metal Quad Flat Pack, Gull-Wing, Cavity Down

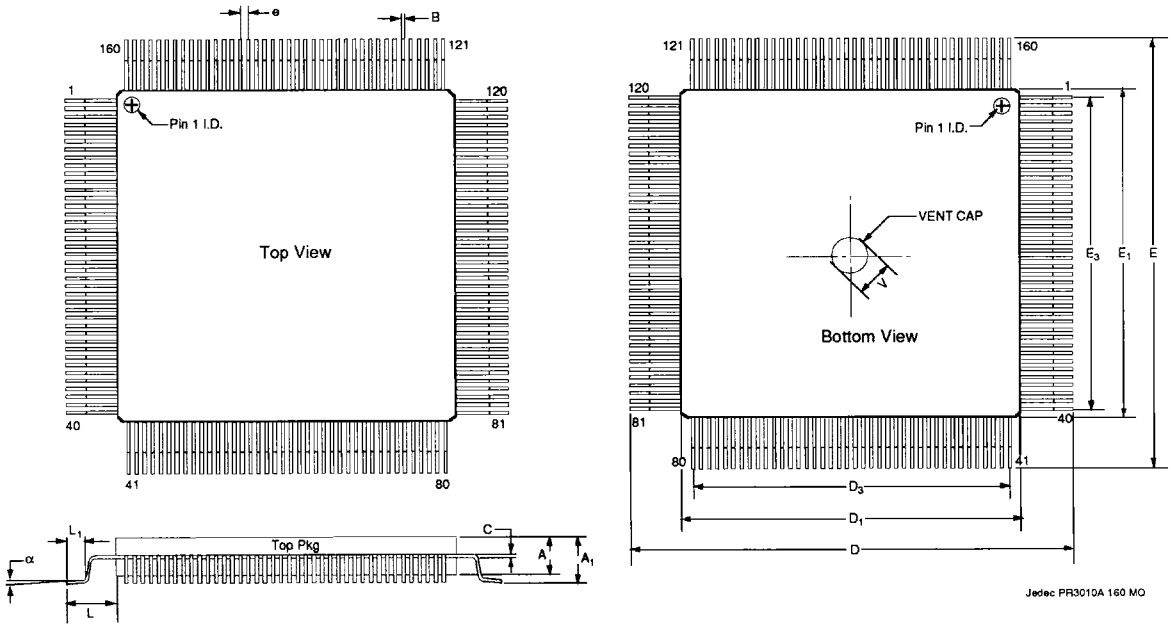
Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	78	FpSysIn	118	Vcc10	102	NC	75
Data(1)	76	FpSysOut	112	Vcc11	116	NC	77
Data(2)	74	FpSync	104	Vcc12	134	NC	79
Data(3)	72	Reset	106	Vcc13	149	NC	80
Data(4)	65	PllOn	93	Vcc14	158	NC	81
Data(5)	63	Run	17	Reserved0	28	NC	82
Data(6)	62	Exception	15	NC	1	NC	84
Data(7)	60	FpInt	13	NC	2	NC	86
Data(8)	57	FpBusy	11	NC	4	NC	87
Data(9)	56	FpCond	10	NC	6	NC	88
Data(10)	54	FpPresent	27	NC	9	NC	90
Data(11)	53	Gnd0	3	NC	12	NC	92
Data(12)	47	Gnd1	8	NC	14	NC	94
Data(13)	46	Gnd2	21	NC	16	NC	96
Data(14)	45	Gnd3	25	NC	18	NC	98
Data(15)	43	Gnd4	31	NC	20	NC	99
Data(16)	156	Gnd5	35	NC	22	NC	101
Data(17)	155	Gnd6	50	NC	24	NC	103
Data(18)	154	Gnd7	51	NC	26	NC	105
Data(19)	153	Gnd8	69	NC	30	NC	107
Data(20)	147	Gnd9	70	NC	32	NC	109
Data(21)	145	Gnd10	83	NC	34	NC	114
Data(22)	144	Gnd11	89	NC	36	NC	119
Data(23)	143	Gnd12	95	NC	37	NC	120
Data(24)	140	Gnd13	100	NC	38	NC	121
Data(25)	139	Gnd14	115	NC	39	NC	122
Data(26)	138	Gnd15	135	NC	40	NC	123
Data(27)	132	Gnd16	136	NC	41	NC	125
Data(28)	130	Gnd17	150	NC	42	NC	127
Data(29)	128	Gnd18	151	NC	44	NC	129
Data(30)	126	Vcc0	7	NC	48	NC	131
Data(31)	117	Vcc1	19	NC	52	NC	133
DataP(0)	59	Vcc2	23	NC	55	NC	137
DataP(1)	5	Vcc3	29	NC	58	NC	142
DataP(2)	141	Vcc4	33	NC	61	NC	146
DataP(3)	113	Vcc5	49	NC	64	NC	148
Clk2xSys	111	Vcc6	67	NC	66	NC	152
Clk2xSmp	110	Vcc7	85	NC	68	NC	157
Clk2xRd	124	Vcc8	91	NC	71	NC	159
Clk2xPhi	108	Vcc9	97	NC	73	NC	160

Figure 4.7 PR3010A Pin Diagram — 160-Pin Metal Quad Flat Pack, Gull-Wing, Cavity Down



PR3010A 160-MQ Pinout

Figure 4.8 PR3010A Package Dimensions — 160-Pin Metal Quad Flat Pack, Gull-Wing, Cavity Down



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.125	3,15	0.135	3,45
A_1	0.135	3,50	0.150	3,85
C	0.004	0,10	0.008	0,20
B	0.010	0,25	0.012	0,30
D/E	1.240	31,50	1,260	32,0
D_1/E_1	1.085	27,55	1.100	27,75
D_3/E_3	1.000	25,4	1.000	25,4
e	0.025 BSC	0,64 BSC	0.25 BSC	0,64 BSC
L	0.040	1,00	0.080	2,00
L_1	0.025	0,65	0.040	0,95
V	0.120	3,10	0.125	3,20
α	0°–5°	0°–5°	0°–5°	0°–5°

BSC = Basic Spacing between Centers

5.0 MOUNTING

A variety of sockets allow low insertion force or zero insertion force mountings, and a choice of terminals such as soldertail, surface mount or wire wrap. Several sockets are available from the following sample list of socket manufacturers. Contact the manufacturer directly for the latest socket specifications.

- AMP Incorporated
  P.O.Box 3608
  Harrisburg, PA 17105-3608
  (800) 522-6752
- Burndy Corporation
  Richards Avenue
  Norwalk, CT 06856
  (203) 838-4444
- Yamaichi Electronics Inc.
  1425 Koll Circle, Suite 106
  San Jose, CA 95112
  (408) 452-0797
- Textool/3M Test
  and Interconnect Products Department
  3M Austin Center
  P.O.Box 2963
  Austin, TX 78769-2963
  (800) 225-5373

6.0 ORDERING INFORMATION

PACEMIPS Microprocessor Products