Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers

Datasheet

The Cortina Systems® LXT9785 and LXT9785E are 8-port Fast Ethernet PHY Transceivers supporting IEEE 802.3 physical layer applications at 10 Mbps and 100 Mbps. These devices provide Serial/Source Synchronous Serial Media Independent Interfaces (SMII/SS-SMII) and Reduced Media Independent Interface (RMII) for switching and other independent port applications. The LXT9785 and LXT9785E are identical except for the IP telephony features included in the LXT9785E transceiver. The LXT9785E is an enhanced version of the LXT9785 that detects Data Terminal Equipment (DTE) requiring power from the switch over a CAT5 cable. The system uses the information collected by the LXT9785E to apply power if the DTE at the far end requires power over the cable, such as an IP telephone.

Each network port can provide a twisted-pair (TP) or Low-Voltage Positive Emitter Coupled Logic (LVPECL) interface. The twisted-pair interface supports 10 Mbps and 100 Mbps (10BASE-T and 100BASE-TX) Ethernet over twisted-pair. The LVPECL interface supports 100 Mbps (100BASE-FX) Ethernet over fiber-optic media.

The LXT9785/LXT9785E provides three discrete LED driver outputs for each port. The devices support both half-duplex and full-duplex operation at 10 Mbps and 100 Mbps and require only a single 2.5 V power supply.

Applications

- Enterprise switches
- IP telephony switches
- Storage Area Networks
- Multi-port Network Interface Cards (NICs)

Product Features

- Eight IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters.
- 100BASE-FX fiber-optic capability on all ports.
- 2.5 V operation.
- Low power consumption; 250 mW per port typical.
- Multiple RMII or SMII/SS-SMII ports for independent PHY port operation.
- Auto MDI/MDIX crossover capability.
- Proprietary Optimal Signal Processing™ architecture improves SNR by 3 dB over ideal analog filters.
- Optimized for dual-high stacked RJ-45 applications.
- MDIO sectionalization into 2x4 or 1x8 configurations.
- Supports both auto-negotiation systems and legacy systems without auto-negotiation capability.
- Robust baseline wander correction.
- Configurable through the MDIO port or external control pins.
- JTAG boundary scan.
- 208-pin PQFP: LXT9785HC, LXT9785EHC, LXT9785HE.
- 241-ball BGA: LXT9785BC, LXT9785EBC.
- 196-ball BGA: LXT9785MBC (includes DTE detection similar to the LXT9785E)
- DTE detection for remote powering applications (LXT9785E and LXT9785MBC only).
- Extended temperature operation of -40 ^{o}C to +85 ^{o}C (LXT9785E only).

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Revision History

Revision 11.0 Revision Date: 16 April 2007
First release of this document from Cortina Systems, Inc.

Revision Number: 010 Revision Date: 30-Mar-2006	
Page	**Description**
page 48	Modified signal description text for VCCPECL in Table 15, *Power Supply Signal Descriptions – PQFP*.
page 93	Modified signal description text for VCCPECL in Table 34, *Power Supply Signal Descriptions – BGA23*.
page 123	Added note under Section 4.4.2.5, *RxCLK Signal (SS-SMII Only)*.
page 126	Modified CFG (1,2,3) settings for Register bit 0.8 when set to “1” in Table 42, *Global Hardware Configuration Settings*.
page 192	Added table note 6 to Register bit 0.14 (Loopback) in Table 84, *Control Register (Address 0)* .
page 195	Modified table note 6 (for Register bit 4.13) in Table 88, *Auto-Negotiation Advertisement Register (Address 4)*.
page 200	Modified note in Register bit 17.11 (Collision Status) in Table 94, *Quick Status Register (Address 17, Hex 11)*.
page 217	Added Section 8.1, *Top Label Markings*.
page 219	Modified Section 9.0, *Ordering Information* (Table 105, *Product Information* and Figure 72, *Ordering Information - Sample*.

Revision Number: 009 Revision Date: April 30, 2004	
Page	**Description**
1	Modified 196-Ball BGA and DTE Detection bullets under Product Features.
43	Added table note 3 (regarding LINKHOLD) to Table 13, *Miscellaneous Signal Descriptions – PQFP*, on page 43.
88	Added table note 3 (regarding LINKHOLD) to Table 32, *Miscellaneous Signal Descriptions – BGA23*, on page 88.
53	Modified Table 18 “RMII BGA23 Ball List in Alphanumeric Order by Signal Name” through Table 23 “SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location” for ball, type, and reference page corrections.
229	Modified Table 104 “Product Information” [added new packaging information].
230	Modified Figure 69 “Ordering Information - Sample” [changed Internal Package Designator for B and E, and added the GD and definition under Package Designator).

Revision Number: 008 Revision Date: April 15, 2004	
Page	**Description**
All	Globally added LEDn_3 to BGA15.
229	Added Figure 68 “Cortina Systems® LXT9785MBC 196-Ball BGA15 Package – Bottom View”.

Revision Number: 007 Revision Date: August 28, 2003	
Page	**Description**
21	Modified Figure 2 “Cortina Systems® LXT9785 and Cortina Systems® LXT9785E RMII 208-Pin PQFP Assignments”.
22	Modified Table 2 “Cortina Systems® LXT9785/LXT9785E RMII PQFP Pin List”.
26	Modified Figure 3 “Cortina Systems® LXT9785/LXT9785E SMII 208-Pin PQFP Assignments”.
27	Modified Table 3 “Cortina Systems® LXT9785/LXT9785E SMII PQFP Pin List”.
31	Modified Figure 4 “Cortina Systems® LXT9785/LXT9785E SS-SMII 208-Pin PQFP Assignments”.
32	Modified Table 4 “Cortina Systems® LXT9785/LXT9785 SS-SMII PQFP Pin List”.
36	Modified Table 5 “Cortina Systems® LXT9785/LXT9785E RMII Signal Descriptions – PQFP”.
40	Modified Table 8 “Cortina Systems® LXT9785/LXT9785E SS-SMII Specific Signal Descriptions – PQFP”.
43	Modified Table 13 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions – PQFP”.
50	Modified Table 16 “Cortina Systems® LXT9785/LXT9785E Unused/Reserved Pins – PQFP”.
51	Replaced old Figures 5, 6, and 7 with Figure 5 “Cortina Systems® LXT9785/LXT9785E 241-Ball BGA23 Assignments (Top View)”.
52	Modified Table 18 “Cortina Systems® LXT9785/LXT9785E RMII BGA23 Ball List in Alphanumeric Order by Signal Name”.
57	Modified Table 19 “Cortina Systems® LXT9785/LXT9785E RMII BGA23 Ball List in Alphanumeric Order by Ball Location”.
62	Modified Table 20 “Cortina Systems® LXT9785/LXT9785E SMII BGA23 Ball List in Alphanumeric Order by Signal Name”.
67	Modified Table 21 “Cortina Systems® LXT9785/LXT9785E SMII BGA23 Ball List in Alphanumeric Order by Ball Location”
72	Modified Table 22 “Cortina Systems® LXT9785/LXT9785E SS-SMII BGA23 Ball List in Alphanumeric Order by Signal Name”.
77	Modified Table 23 “Cortina Systems® LXT9785/LXT9785E SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location”.
82	Modified Table 23 “Cortina Systems® LXT9785/LXT9785E SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location”.
86	Modified Table 27 “Cortina Systems® LXT9785/LXT9785E SS-SMII Specific Signal Descriptions – BGA23”.
90	Modified Table 32 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions – BGA23”.
97	Modified Table 35 “Cortina Systems® LXT9785/LXT9785E Unused/Reserved Pins – BGA23”.
98	Added Section 3.5, “BGA15 Ball Assignments” (including Figure 6 “Cortina Systems® LXT9785MBC 196-Ball BGA15 Assignments (Top View)”, Table 37 “Cortina Systems® LXT9785MBC BGA15 Ball List in Alphanumeric Order by Signal Name” through Table 39 “Cortina Systems® LXT9785 BGA15 Signal Descriptions”.
116	Added second paragraph under Section 4.1, “Introduction”.
117	Added note under Section 4.1.2.1, “Sectionalization”.
119	Added note under Table 40 “Cortina Systems® LXT9785/LXT9785E MDIX Selection”.
119	Added note under Section 4.3, “Media Independent Interface (MII) Interfaces”.
120	Added note to Table 41 “Cortina Systems® LXT9785/LXT9785E MII Mode Select”.
120	Modified/added text under Section 4.3.2, “Internal Loopback”.
121	Modified text under Section 4.3.6, “MII Isolate”.

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Page	**Description**
121	Section 4.3.7, “MDIO Management Interface”: Added note under second paragraph. Added last paragraph.
123	Added note under Section 4.3.8, “MII Sectionalization”.
124	Added new Section 4.3.11, “FIFO Initial Fill Values”
125	Modified paragraph three under Section 4.4.1, “Power Requirements”.
127	Added notes under second and last paragraphs under Section 4.5.3, “Power-Down Mode”.
128	Modified last bullet under Section 4.5.3.1, “Global (Hardware) Power Down”.
128	Added last paragraph to Section 4.5.4, “Reset”.
129	Modified Table 42 “Cortina Systems® LXT9785/LXT9785E Global Hardware Configuration Settings”.
130	Change heading and modified last line under Section 4.6.1.2, “Manual Next Page Exchange”.
130	Section 4.6.1.4, “Link Criteria”: Changed scrambler to descrambler in first line. Modified second paragraph. Added two new paragraphs.
131	Added second paragraph under Section 4.6.1.5, “Parallel Detection”.
131	Modified paragraphs under Section 4.6.1.6, “Reliable Link Establishment While Auto MDI/MDIX is Enabled in Forced Speed Mode”.
136	Changed “1110” to “0101” under Section 4.7.4.3, “Receive Error”.
141	Added note under first paragraph of Section 4.8, “RMII Operation”
148	Changed “asynchronously” to “synchronously” in second paragraph under Section 4.9.3.3, “Carrier Sense/Data Valid (RMII)”.
148	Modified last sentence in first paragraph under Section 4.9.3.4, “Carrier Sense (SMII)”.
149	Modified paragraph under Section 4.9.3.6.3, “Polarity Correction”.
149	Added note under Section 4.9.3.7, “Fiber PMD Sublayer”.
149	Added second paragraph under Section 4.9.3.7.1, “Far End Fault Indications”.
150	Modified/added text under Section 4.10.1, “Preamble Handling”.
151	Modified text under Section 4.10.4, “Jabber”.
152	Modified first paragraph under Section 4.11, “DTE Discovery Process”.
153	Modified Item 1 of Section 4.11.2, “Interaction between Processor, MAC, and PHY”.
154	Modified second paragraph under Section 4.11.4, “DTE Discovery Process Flow”.
155	Added Section 4.11.5, “DTE Discovery Behavior”
157	Added BGA15 information into first paragraph under Section 4.12.2, “Per-Port LED Driver Functions”.
158	Added last sentence to first paragraph and note under first paragraph under Section 4.12.3, “Out-of-Band Signaling”.
160	Added Section 4.13, “Cable Diagnostics Overview”.
161	Modified/added text under Section 4.13.3, “Implementation Considerations”.
162	Added Section 4.14, “Link Hold-Off Overview”.
173	Modified Table 52 “Cortina Systems® LXT9785/LXT9785E Operating Conditions”
176	Modified Table 58 “Cortina Systems® LXT9785/LXT9785E 100BASE-FX Transceiver Characteristics”

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Page	**Description**
178-195	Added note to Table 60 “Cortina Systems® LXT9785/LXT9785E SMII - 100BASE-TX Receive Timing Parameters” through Table 77 “Cortina Systems® LXT9785/LXT9785E RMII - 10BASE-T Transmit Timing Parameters”.
178	Added table note to Table 60 “Cortina Systems® LXT9785/LXT9785E SMII - 100BASE-TX Receive Timing Parameters”.
184	Added table note to Table 66 “Cortina Systems® LXT9785/LXT9785E SS-SMII - 100BASE-TX Receive Timing Parameters”.
190	Added table note to Table 72 “Cortina Systems® LXT9785/LXT9785E RMII - 100BASE-TX Receive Timing Parameters”
198	Added software power-down and note to Table 80 “Cortina Systems® LXT9785/LXT9785E Power-Up Timing Parameters”.
199	Modified paragraphs and added last paragraph under Section 7.0, “Register Definitions”.
199	Modified Table 82 “Cortina Systems® LXT9785/LXT9785E Register Set”.
200	Modified Table 83 “Control Register (Address 0)”.
201	Modified Table 84 “Status Register (Address 1)”.
203	Modified Table 85 “PHY Identification Register 1 (Address 2)”.
203	Modified Table 86 “PHY Identification Register 2 (Address 3)”
204	Modified Table 87 “Auto-Negotiation Advertisement Register (Address 4)”
205	Modified Table 88 “Auto-Negotiation Link Partner Base Page Ability Register (Address 5)”.
206	Modified Table 89 “Auto-Negotiation Expansion Register (Address 6)”.
206	Modified Table 90 “Auto-Negotiation Next Page Transmit Register (Address 7)”.
206	Modified Table 91 “Auto-Negotiation Link Partner Next Page Receive Register (Address 8)”.
207	Modified Table 92 “Port Configuration Register (Address 16, Hex 10)”. (Register bits 16.6, 16.4:3)
209	Modified Table 93 “Quick Status Register (Address 17, Hex 11)”. (Register bit 17.8)
211	Modified Table 94 “Interrupt Enable Register (Address 18, Hex 12)”
212	Modified Table 95 “Interrupt Status Register (Address 19, Hex 13)”
213	Modified Table 96 “LED Configuration Register (Address 20, Hex 14)”
214	Modified Table 97 “Receive Error Count Register (Address 21, Hex 15)”.
215	Modified Table 98 “RMII Out-of-Band Signaling Register (Address 25, Hex 19)”.
216	Modified Table 99 “Trim Enable Register (Address 27, Hex 1B)”. (Register bit 27.6)
217	Added Table 100 “Cable Diagnostics Register (Address 29, Hex 1D)”.
219	Modified Table 101 “Cortina Systems® LXT9785/LXT9785E Register Bit Map”.
226	Added Figure 102 “Cortina Systems® LXT9785MBC 196-Ball BGA15 Package Dimensions”
227	Modified table and figure under Section 9.0, “Ordering Information”.

Revision Number: 006 (INTERNAL RELEASE) Revision Date: June 10, 2003	
Page	**Description**
1	Changed "pseudo-ECL (PECL)" to "Low Voltage Positive Emitter Coupled Logic (LVPECL)" in the second paragraph, front page.
36	Modified Table 5 “Cortina Systems® LXT9785/LXT9785E RMII Signal Descriptions – PQFP”. Added last sentence to RXER0 through RXER7 signal description.
42	Modified Table 10 “Cortina Systems® LXT9785/LXT9785E Signal Detect – PQFP”.
42	Modified Table 11 “Cortina Systems® LXT9785/LXT9785E Network Interface Signal Descriptions – PQFP”,
43	Modified Table 13 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions – PQFP”. Added note to PREASEL signal description.
116	Modified Section 4.1, “Introduction”. Changed "Pseudo-ECL (PECL)" to "Low Voltage PECL (LVPECL)" in the first paragraph, second sentence.
119	Replace text under Section 4.2.1.3, “Fiber Interface”.
120	Modified Section 4.3.2, “Internal Loopback”.
130	Modified last sentence under Section 4.6.1.4, “Link Criteria”.
131	Modified text under Section 4.6.1.5, “Parallel Detection”. Added second paragraph.
136	Modified text under Section 4.7.4.3, “Receive Error”.
145	Changed "PECL" to "LVPECL in third paragraph, first sentence under Section 4.9.1, “100BASE-X Network Operations”.
146	Modified Figure 28 “Cortina Systems® LXT9785/LXT9785E Protocol Sublayers”.
148	Modified Section 4.9.3.3, “Carrier Sense/Data Valid (RMII)”. Changed “asynchronously to “synchronously.”
148	Modified text under Section 4.9.3.4, “Carrier Sense (SMII)”. Revised last sentence in first paragraph.
149	Modified paragraph under Section 4.9.3.6.3, “Polarity Correction”.
149	Replaced text under Section 4.9.3.7, “Fiber PMD Sublayer”.
150	Modified Section 4.10.1, “Preamble Handling”. Added text to last paragraph.
151	Modified first sentence under Section 4.10.4, “Jabber”.
152	Modified first paragraph of Section 4.11, “DTE Discovery Process”.
153	Modified Item 1 of Section 4.11.2, “Interaction between Processor, MAC, and PHY”.
158	Modified Section 4.12.3, “Out-of-Band Signaling”. Added sentence to end of first paragraph.
166	Replaced text under Section 5.2.5, “The Fiber Interface”.
170	Replaced Figure 36 “Recommended Cortina Systems® LXT9785/LXT9785E-to-3.3 V Fiber Transceiver Interface Circuitry”.
171	Replaced Figure 37 “Recommended Cortina Systems® LXT9785/LXT9785E-to-5 V Fiber Transceiver Interface Circuitry”.
173	Modified Table 52 “Cortina Systems® LXT9785/LXT9785E Operating Conditions”.
174	Modified Table 53 “Cortina Systems® LXT9785/LXT9785E Digital I/O DC Electrical Characteristics (VCCIO = 2.5 V +/- 5%)”.
175	Modified Table 54 “Cortina Systems® LXT9785/LXT9785E Digital I/O DC Electrical Characteristics (VCCIO = 3.3 V +/- 5%)”.
175	Added Table 55 “Cortina Systems® LXT9785/LXT9785E Digital I/O DC Electrical Characteristics – SD Pins”.
176	Modified Table 58 “Cortina Systems® LXT9785/LXT9785E 100BASE-FX Transceiver Characteristics”.

Revision Number: 006 (INTERNAL RELEASE) Revision Date: June 10, 2003	
Page	**Description**
200	Modified Table 83 “Control Register (Address 0)”.
201	Modified Table 84 “Status Register (Address 1)”.
204	Modified Table 87 “Auto-Negotiation Advertisement Register (Address 4)”.
205	Modified Table 88 “Auto-Negotiation Link Partner Base Page Ability Register (Address 5)”.
207	Modified Table 91 “Auto-Negotiation Link Partner Next Page Receive Register (Address 8)”.
207	Modified Table 92 “Port Configuration Register (Address 16, Hex 10)”.
209	Modified Table 93 “Quick Status Register (Address 17, Hex 11)”.
211	Modified Table 94 “Interrupt Enable Register (Address 18, Hex 12)”
212	Modified Table 95 “Interrupt Status Register (Address 19, Hex 13)”. Changed all references of RO/SC to R/LH.
214	Modified Table 97 “Receive Error Count Register (Address 21, Hex 15)”.
215	Modified Table 98 “RMII Out-of-Band Signaling Register (Address 25, Hex 19)”. Added note to Register bit 25.0.
216	Modified Table 99 “Trim Enable Register (Address 27, Hex 1B)”.
227	Modified Table 103 “Product Information”.

Revision Number: 005 Revision Date: January 2002	
Page	**Description**
1	Added bullet to Product Features
49	Modified Table 12 “Cortina Systems® LXT9785/LXT9785E Miscellaneous Signal Descriptions” (Added FIFOSEL1 and FIFOSEL0)
70	Added Section 2.6.1.6, “Reliable Link Establishment While Auto MDI/MDIX is Enabled in Forced Speed Mode”
109	Modified Figure 38 “Recommended Cortina Systems® LXT9785/LXT9785E-to-3.3 V Fiber Transceiver Interface Circuitry”
110	Added Figure 39 “Recommended Cortina Systems® LXT9785/LXT9785E-to-5 V Fiber Transceiver Interface Circuitry”
111	Added Figure 40 “ON Semiconductor Triple PECL-to-LVPECL Translator”
112	Modified Table 28 “Absolute Maximum Ratings”
112	Modified Table 29 “Operating Conditions”
114	Modified Table 31 “Digital I/O DC Electrical Characteristics (VCCIO = 3.3 V +/- 5%)”(Output low voltage SD pins - Max)
129	Modified Figure 53 “RMII - 100BASE-TX Receive Timing” and Table 49 “RMII - 100BASE-TX Receive Timing Parameters”
131	Modified Figure 55 “RMII - 100BASE-FX Receive Timing” and Table 51 “RMII - 100BASE-FX Receive Timing Parameters”
133	Modified Figure 57 “RMII - 10BASE-T Receive Timing” and Table 53 “RMII - 10BASE-T Receive Timing Parameters”

Revision Number: 005 Revision Date: January 2002	
Page	**Description**
146	Modified Table 69 “Port Configuration Register (Address 16, Hex 10)” (Bits 16.5 and 16.6)
148	Modified Table 71 “Interrupt Enable Register (Address 18, Hex 12)”
168	Added product ordering table and diagram.

Revision Number: 003 Revision Date: April 2001	
Page	**Description**
1	Modified and added new language to front page.
61	Reset: Modified language in first paragraph.
85	Added new section on DTE discovery.
93	Supported JTAG Instructions table: replaced long hit streams with hex.
97	LED Circuit: Modified paragraph language.
97	LED Circuit diagram: Modified diagram.
99	Replaced Typical Fiber Interface diagram.
102	Required Clock Characteristics table: Replaced SMII Input frequency and RMII Input frequency symbol with “f”.
122	Auto-Negotiation and Fast Link Pulse Timing Parameters: FLP burst width under Typ = 2.
126	Control Register table: Modified table and table notes.
128	PHY Identification Register 2 (Address 3): Modified table.
128	PHY Identifier Bit Mapping: Modified diagram.
131	Auto-Negotiation Expansion: Modified table and table notes.
133	Port Configuration Register table: Modified table and table notes.
140	Trim Enable Register: Modified table (DTE Discovery).
141	Modified Register Bit Map table.

1.0 Introduction

This document contains information on the Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers.

1.1 What You Will Find in This Document

This document contains the following sections:

- Section 2.0, *Block Diagram*, on page 19
- Section 3.0, *Pin/Ball Assignments and Signal Descriptions*, on page 20
  This section contains pin/ball assignments and signal descriptions for the following:
  - Section 3.1, *PQFP Pin Assignments*, on page 20
  - Section 3.2, *PQFP Signal Descriptions*, on page 36
  - Section 3.3, *BGA23 Ball Assignments*, on page 51
  - Section 3.4, *BGA23 Signal Descriptions*, on page 79
  - Section 3.5, *BGA15 Ball Assignments*, on page 97
  - Section 3.6, *BGA15 Signal Descriptions*, on page 106
- Section 4.0, *Functional Description*, on page 113
- Section 5.0, *Application Information*, on page 161
- Section 6.0, *Test Specifications*, on page 170
- Section 7.0, *Register Definitions*, on page 191
- Section 8.0, *Package Specifications*, on page 212
- Section 9.0, *Ordering Information*, on page 219

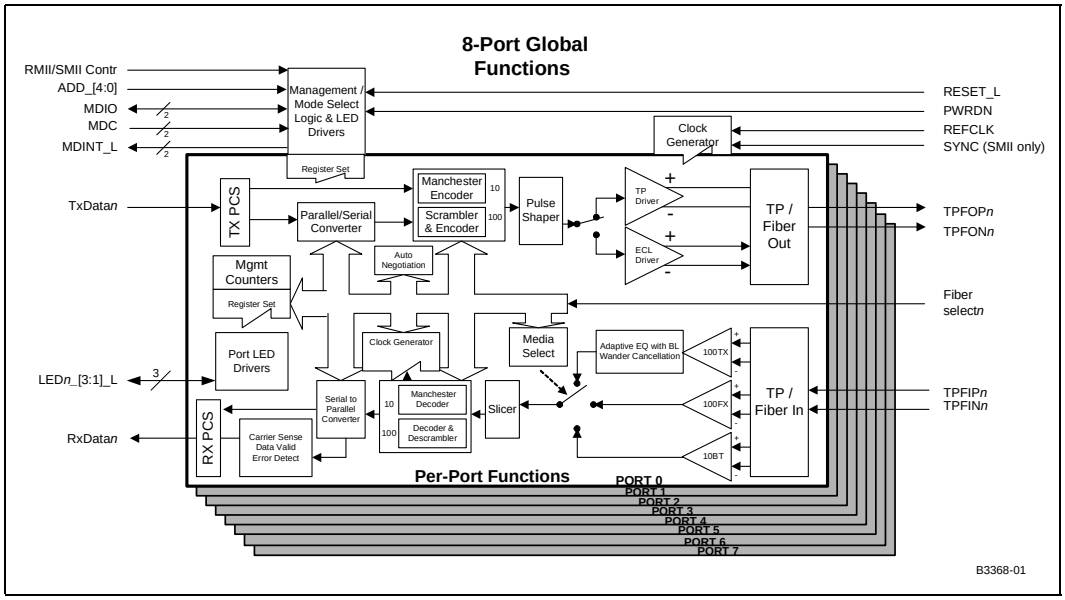
1.2 Related Documents

Document	Document Number
Cortina Systems® LXT9785/LXT9785E Design and Layout Guide	249509
Cortina Systems® LXT9785/LXT9785E Specification Update	249357
Cortina Systems® LXT9785/LXT9785E 100BASE-FX Fiber Optic Transceivers: Connecting a PECL/LVPECL Interface	250781
IP Telephony and DTE Discovery Using Cortina Systems® Ethernet PHYs	249611

2.0 Block Diagram

Figure 1 provides the LXT9785/LXT9785E block diagram.

Figure 1 Block Diagram



3.0 Pin/Ball Assignments and Signal Descriptions

3.1 PQFP Pin Assignments

The following sections show PQFP pin assignments and signal descriptions:

- Section 3.1.1, *PQFP Pin Assignments – RMII Configuration*, on page 20
- Section 3.1.2, *PQFP Pin Assignments – SMII Configuration*, on page 26
- Section 3.1.3, *PQFP Pin Assignments – SS-SMII Configuration*, on page 31

Table 1 lists the acronyms and descriptions for signal types.

Table 1 Signal Type Descriptions

Acronym	Description
AI	Analog Input
AO	Analog Output
I	Input
O	Output
OD	Open Drain Output
ST	Schmitt Triggered Input
TS	Three-State-able Output
SL	Slew-rate Limited Output
IP	Weak Internal Pull-Up
ID	Weak Internal Pull-Down

3.1.1 PQFP Pin Assignments – RMII Configuration

Figure 2 and Table 2, *RMII PQFP Pin List*, on page 22 provide LXT9785/LXT9785E RMII PQFP pin assignments.

Figure 2 RMII 208-Pin PQFP Assignments

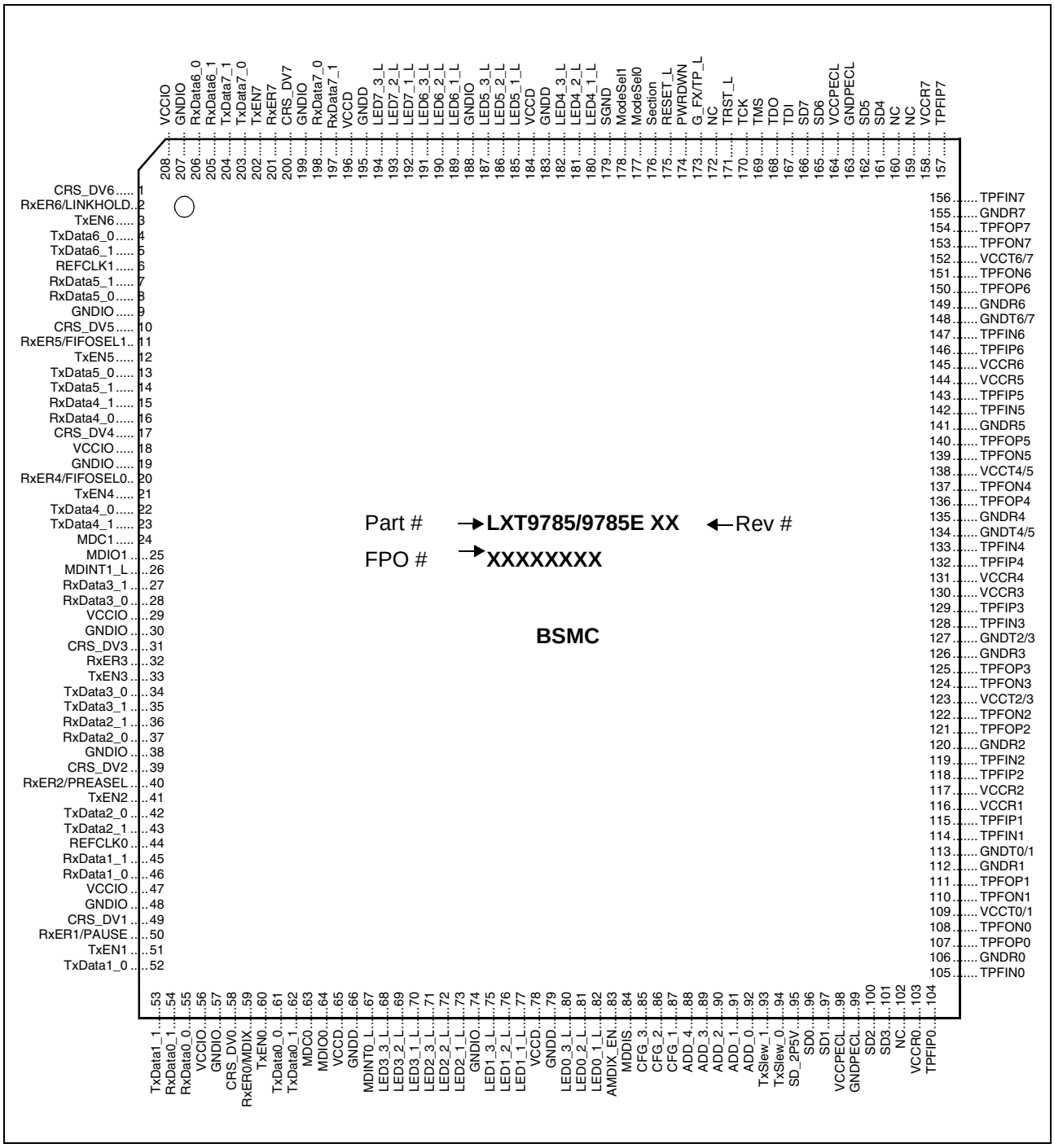


Table 2 RMII PQFP Pin List

Pin	Symbol	Type	Reference for Full Description
1	CRS_DV6	O, TS, SL	Table 5
2	RxER6/ LINKHOLD	O, TS, SL, ID, I, ST	Table 5 Table 13
3	TxEN6	I, ID	Table 5
4	TxData6_0	I, ID	Table 5
5	TxData6_1	I, ID	Table 5
6	REFCLK1	I	Table 5
7	RxData5_1	O, TS, ID	Table 5
8	RxData5_0	O, TS	Table 5
9	GNDIO	–	Table 15
10	CRS_DV5	O, TS, SL	Table 5
11	RxER5 / FIFOSEL1	O, TS, SL, ID, I, ST	Table 5 Table 13
12	TxEN5	I, ID	Table 5
13	TxData5_0	I, ID	Table 5
14	TxData5_1	I, ID	Table 5
15	RxData4_1	O, TS,ID	Table 5
16	RxData4_0	O, TS	Table 5
17	CRS_DV4	O, TS, SL	Table 5
18	VCCIO	–	Table 15
19	GNDIO	–	Table 15
20	RxER4 / FIFOSEL0	O, TS, SL, ID, I, ST	Table 5 Table 13
21	TxEN4	I, ID	Table 5
22	TxData4_0	I, ID	Table 5
23	TxData4_1	I, ID	Table 5
24	MDC1	I, ST, ID	Table 8
25	MDIO1	I/O, TS, SL, IP	Table 8
26	MDINT1_L	OD, TS, SL, IP	Table 8
27	RxData3_1	O, TS, ID	Table 5
28	RxData3_0	O, TS	Table 5
29	VCCIO	–	Table 15
30	GNDIO	–	Table 15
31	CRS_DV3	O, TS, SL	Table 5
32	RxER3	O, TS, SL, ID	Table 5
33	TxEN3	I, ID	Table 5
34	TxData3_0	I, ID	Table 5
35	TxData3_1	I, ID	Table 5
36	RxData2_1	O, TS, ID	Table 5
37	RxData2_0	O, TS	Table 5
38	GNDIO	–	Table 15
39	CRS_DV2	O, TS, SL	Table 5
40	RxER2 (PREASEL)	O, TS, SL, ID, I, ST	Table 5 Table 13
41	TxEN2	I, ID	Table 5
42	TxData2_0	I, ID	Table 5
43	TxData2_1	I, ID	Table 5
44	REFCLK0	I	Table 5
45	RxData1_1	O, TS, ID	Table 5
46	RxData1_0	O, TS	Table 5
47	VCCIO	–	Table 15
48	GNDIO	–	Table 15
49	CRS_DV1	O, TS, SL	Table 5
50	RxER1/ PAUSE	O, TS, SL, ID, I, ST	Table 5
51	TxEN1	I, ID	Table 5
52	TxData1_0	I, ID	Table 5
53	TxData1_1	I, ID	Table 5
54	RxData0_1	O, TS, ID	Table 5
55	RxData0_0	O, TS	Table 5
56	VCCIO	–	Table 15
57	GNDIO	–	Table 15
58	CRS_DV0	O, TS, SL	Table 5

Pin	Symbol	Type	Reference for Full Description
59	RxER0/ MDIX	O, TS, SL, ID, I, ST	Table 5
60	TxEN0	I, ID	Table 5
61	TxData0_0	I, ID	Table 5
62	TxData0_1	I, ID	Table 5
63	MDC0	I, ST, ID	Table 8
64	MDIO0	I/O, TS, SL, IP	Table 8
65	VCCD	–	Table 15
66	GNDD	–	Table 15
67	MDINT0_L	OD, TS, SL, IP	Table 8
68	LED3_3_L	OD, TS, SO, IP	Table 14
69	LED3_2_L	OD, TS, SL, IP	Table 14
70	LED3_1_L	OD, TS, SL, IP	Table 14
71	LED2_3_L	OD, TS, SL, IP	Table 14
72	LED2_2_L	OD, TS, SL, IP	Table 14
73	LED2_1_L	OD, TS, SL, IP	Table 14
74	GNDIO	–	Table 15
75	LED1_3_L	OD, TS, SL, IP	Table 14
76	LED1_2_L	OD, TS, SL, IP	Table 14
77	LED1_1_L	OD, TS, SL, IP	Table 14
78	VCCD	–	Table 15
79	GNDD	–	Table 15
80	LED0_3_L	OD, TS, SL, IP	Table 14
81	LED0_2_L	OD, TS, SL, IP	Table 14
82	LED0_1_L	OD, TS, SL, IP	Table 14
83	AMDIX_EN	I, ST, IP	Table 13
84	MDDIS	I, ST, ID	Table 9
85	CFG_3	I, ST, ID	Table 13
86	CFG_2	I, ST, ID	Table 13

Pin	Symbol	Type	Reference for Full Description
87	CFG_1	I, ST, ID	Table 13
88	ADD_4	I, ST, ID	Table 13
89	ADD_3	I, ST, ID	Table 13
90	ADD_2	I, ST, ID	Table 13
91	ADD_1	I, ST, ID	Table 13
92	ADD_0	I, ST, ID	Table 13
93	TxSLEW_1	I, ST, ID	Table 13
94	TxSLEW_0	I, ST, ID	Table 13
95	SD_2P5V	I, ST, ID	Table 10
96	SD0	I	Table 10
97	SD1	I	Table 10
98	VCCPECL	–	Table 15
99	GNDPECL	–	Table 15
100	SD2	I	Table 10
101	SD3	I	Table 10
102	NC	–	Table 17
103	VCCR0	–	Table 15
104	TPFIP0	AO/AI	Table 11
105	TPFIN0	AO/AI	Table 11
106	GNDR0	–	Table 15
107	TPFOP0	AO/AI	Table 11
108	TPFON0	AO/AI	Table 11
109	VCCT0/1	–	Table 15
110	TPFON1	AO/AI	Table 11
111	TPFOP1	AO/AI	Table 11
112	GNDR1	–	Table 15
113	GNDT0/1	–	Table 15
114	TPFIN1	AO/AI	Table 11
115	TPFIP1	AO/AI	Table 11
116	VCCR1	–	Table 15
117	VCCR2	–	Table 15
118	TPFIP2	AO/AI	Table 11
119	TPFIN2	AO/AI	Table 11
120	GNDR2	–	Table 15
121	TPFOP2	AO/AI	Table 11
122	TPFON2	AO/AI	Table 11
123	VCCT2/3	–	Table 15
124	TPFON3	AO/AI	Table 11

Pin	Symbol	Type	Reference for Full Description
125	TPFOP3	AO/AI	Table 11
126	GNDR3	–	Table 15
127	GNDT2/3	–	Table 15
128	TPFIN3	AO/AI	Table 11
129	TPFIP3	AO/AI	Table 11
130	VCCR3	–	Table 15
131	VCCR4	–	Table 15
132	TPFIP4	AO/AI	Table 11
133	TPFIN4	AO/AI	Table 11
134	GNDT4/5	–	Table 15
135	GNDR4	–	Table 15
136	TPFOP4	AO/AI	Table 11
137	TPFON4	AO/AI	Table 11
138	VCCT4/5	–	Table 15
139	TPFON5	AO/AI	Table 11
140	TPFOP5	AO/AI	Table 11
141	GNDR5	–	Table 15
142	TPFIN5	AO/AI	Table 11
143	TPFIP5	AO/AI	Table 11
144	VCCR5	–	Table 15
145	VCCR6	–	Table 15
146	TPFIP6	AO/AI	Table 11
147	TPFIN6	AO/AI	Table 11
148	GNDT6/7	–	Table 15
149	GNDR6	–	Table 15
150	TPFOP6	AO/AI	Table 11
151	TPFON6	AO/AI	Table 11
152	VCCT6/7	–	Table 15
153	TPFON7	AO/AI	Table 11
154	TPFOP7	AO/AI	Table 11
155	GNDR7	–	Table 15
156	TPFIN7	AO/AI	Table 11
157	TPFIP7	AO/AI	Table 11
158	VCCR7	–	Table 15
159	NC	–	Table 17
160	NC	–	Table 17
161	SD4	I	Table 10
162	SD5	I	Table 10

Pin	Symbol	Type	Reference for Full Description
163	GNDPECL	–	Table 15
164	VCCPECL	–	Table 15
165	SD6	I	Table 10
166	SD7	I	Table 10
167	TDI	I, ST, IP	Table 12
168	TDO	O, TS	Table 12
169	TMS	I, ST, IP	Table 12
170	TCK	I, ST, ID	Table 12
171	TRST_L	I, ST, IP	Table 12
172	NC	–	Table 17
173	G_FX/TP_L	I, ST, ID	Table 13
174	PWRDWN	I, ST, ID	Table 13
175	RESET_L	I, ST, IP	Table 13
176	SECTION	I, ST, ID	Table 13
177	ModeSel0	I, ST, ID	Table 13
178	ModeSel1	I, ST, ID	Table 13
179	SGND	–	Table 15
180	LED4_1_L	OD, TS, SL, IP	Table 14
181	LED4_2_L	OD, TS, SL, IP	Table 14
182	LED4_3_L	OD, TS, SL, IP	Table 14
183	GNDD	–	Table 15
184	VCCD	–	Table 15
185	LED5_1_L	OD, TS, SL, IP	Table 14
186	LED5_2_L	OD, TS, SL, IP	Table 14
187	LED5_3_L	OD, TS, SL, IP	Table 14
188	GNDIO	–	Table 15
189	LED6_1_L	OD, TS, SL, IP	Table 14
190	LED6_2_L	OD, TS, SL, IP	Table 14
191	LED6_3_L	OD, TS, SL, IP	Table 14
192	LED7_1_L	OD, TS, SL, IP	Table 14
193	LED7_2_L	OD, TS, SL, IP	Table 14

Pin	Symbol	Type	Reference for Full Description
194	LED7_3_L	OD, TS, SL, IP	Table 5
195	GNDD	–	Table 15
196	VCCD	–	Table 15
197	RxData7_1	O, TS, ID	Table 5
198	RxData7_0	O, TS	Table 5
199	GNDIO	–	Table 15
200	CRS_DV7	O, TS, SL	Table 5
201	RxER7	O, TS, SL, ID	Table 5
202	TxEN7	I, ID	Table 5
203	TxData7_0	I, ID	Table 5
204	TxData7_1	I, ID	Table 5
205	RxData6_1	O, TS, ID	Table 5
206	RxData6_0	O, TS	Table 5
207	GNDIO	–	Table 15
208	VCCIO	–	Table 15

3.1.2 PQFP Pin Assignments – SMII Configuration

Figure 3 and Table 3, *SMII PQFP Pin List*, on page 27 provide the LXT9785/LXT9785E SMII PQFP pin assignments.

Figure 3 SMII 208-Pin PQFP Assignments

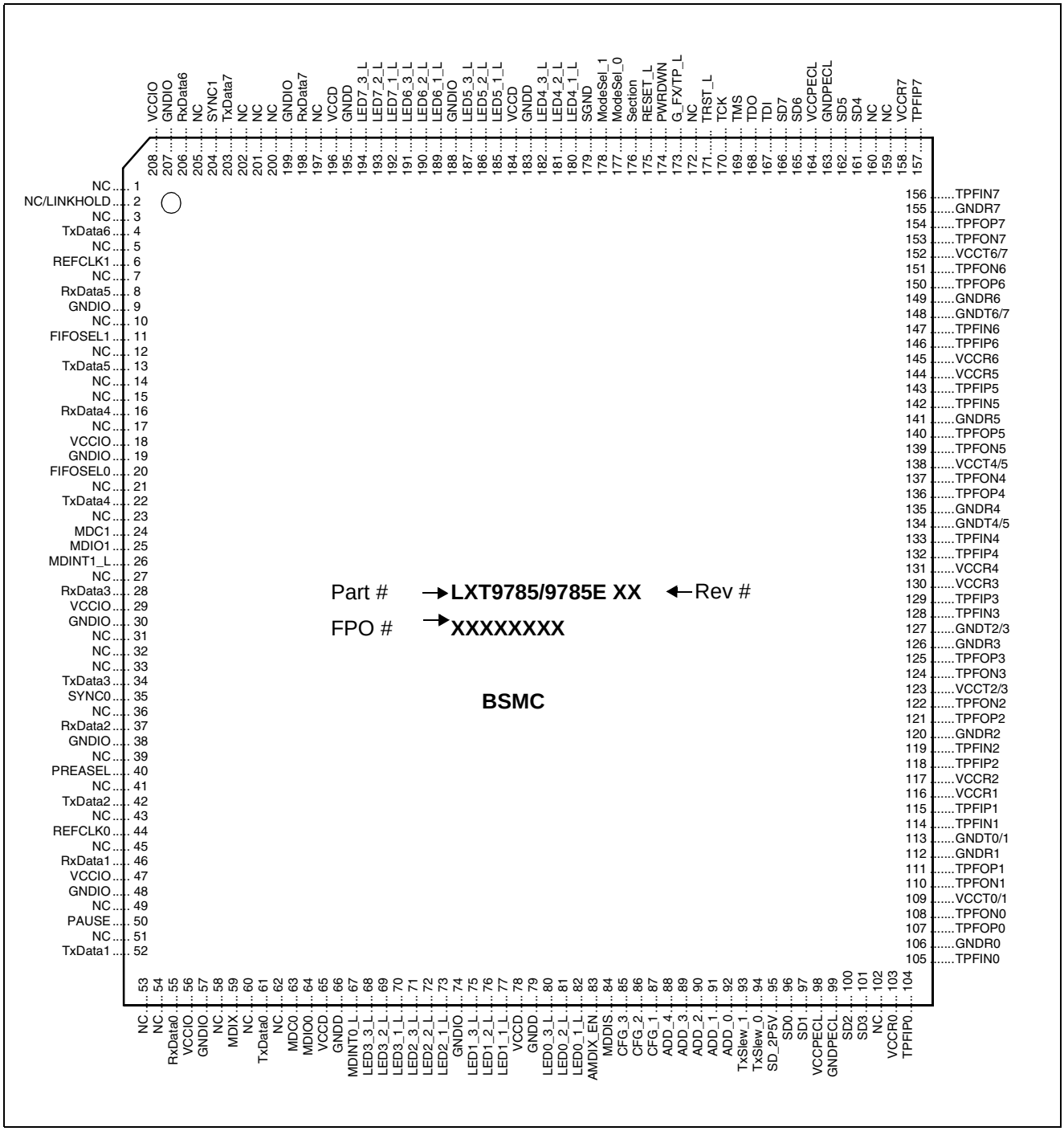


Table 3 SMII PQFP Pin List

Pin	Symbol	Type[1]	Reference for Full Description
1	NC	–	Table 16
2	NC/ LINKHOLD	I, ID,	Table 16 Table 13
3	NC	–	Table 16
4	TxData6	I, ID	Table 6
5	NC	–	Table 16
6	REFCLK1	I	Table 5
7	NC	–	Table 16
8	RxData5	O, TS	Table 6
9	GNDIO	–	Table 15
10	NC	–	Table 16
11	FIFOSEL1	I, ID, ST	Table 13
12	NC	–	Table 16
13	TxData5	I, ID	Table 6
14	NC	–	Table 16
15	NC	–	Table 16
16	RxData4	O, TS	Table 6
17	NC	–	Table 16
18	VCCIO	–	Table 15
19	GNDIO	–	Table 15
20	FIFOSEL0	I, ID, ST	Table 13
21	NC	I, ID	Table 16
22	TxData4	I, ID	Table 6
23	NC	–	Table 16
24	MDC1	I, ST, ID	Table 9
25	MDIO1	I/O, TS, SL, IP	Table 9
26	MDINT1_L	OD, TS, SL, IP	Table 9
27	NC	–	Table 16
28	RxData3	O, TS	Table 6
29	VCCIO	–	Table 15
30	GNDIO	–	Table 15
31	NC	–	Table 16
32	NC	–	Table 16
33	NC	–	Table 16
34	TxData3	I, ID	Table 6
35	SYNC0	I, ID	Table 7
36	NC	–	Table 16
37	RxData2	O, TS	Table 6
38	GNDIO	–	Table 15
39	NC	–	Table 16
40	PREASEL	I, ID, ST	Table 13
41	NC	–	Table 16
42	TxData2	I, ID	Table 6
43	NC	–	Table 16
44	REFCLK0	I	Table 5
45	NC	–	Table 16
46	RxData1	O, TS	Table 6
47	VCCIO	–	Table 15
48	GNDIO	–	Table 15
49	NC	–	Table 16
50	PAUSE	I, ID, ST	Table 13
51	NC	–	Table 16
52	TxData1	I, ID	Table 6
53	NC	–	Table 16
54	NC	–	Table 16
55	RxData0	O, TS	Table 6
56	VCCIO	–	Table 15
57	GNDIO	–	Table 15
58	NC	–	Table 16
59	MDIX	I, ID, ST	Table 13
60	NC	–	Table 16
61	TxData0	I, ID	Table 6
62	NC	–	Table 16
63	MDC0	I, ST, ID	Table 9
64	MDIO0	I/O, TS, SL, IP	Table 9
65	VCCD	–	Table 15
66	GNDD	–	Table 15
67	MDINT0_L	OD, TS, SL, IP	Table 9

Pin	Symbol	Type[1]	Reference for Full Description
68	LED3_3_L	OD, TS, SO, IP	Table 14
69	LED3_2_L	OD, TS, SL, IP	Table 14
70	LED3_1_L	OD, TS, SL, IP	Table 14
71	LED2_3_L	OD, TS, SL, IP	Table 14
72	LED2_2_L	OD, TS, SL, IP	Table 14
73	LED2_1_L	OD, TS, SL, IP	Table 14
74	GNDIO	–	Table 15
75	LED1_3_L	OD, TS, SL, IP	Table 14
76	LED1_2_L	OD, TS, SL, IP	Table 14
77	LED1_1_L	OD, TS, SL, IP	Table 14
78	VCCD	–	Table 15
79	GNDD	–	Table 15
80	LED0_3_L	OD, TS, SL, IP	Table 14
81	LED0_2_L	OD, TS, SL, IP	Table 14
82	LED0_1_L	OD, TS, SL, IP	Table 14
83	AMDIX_EN	I, ST, IP	Table 13
84	MDDIS	I, ST, ID	Table 8
85	CFG_3	I, ST, ID	Table 13
86	CFG_2	I, ST, ID	Table 13
87	CFG_1	I, ST, ID	Table 13
88	ADD_4	I, ST, ID	Table 13
89	ADD_3	I, ST, ID	Table 13
90	ADD_2	I, ST, ID	Table 13
91	ADD_1	I, ST, ID	Table 13

Pin	Symbol	Type[1]	Reference for Full Description
92	ADD_0	I, ST, ID	Table 13
93	TxSLEW_1	I, ST, ID	Table 13
94	TxSLEW_0	I, ST, ID	Table 13
95	SD_2P5V	I, ST, ID	Table 10
96	SD0	I	Table 10
97	SD1	I	Table 10
98	VCCPECL	–	Table 15
99	GNDPECL	–	Table 15
100	SD2	I	Table 10
101	SD3	I	Table 10
102	NC	–	Table 17
103	VCCR0	–	Table 15
104	TPFIP0	AI/AO	Table 11
105	TPFIN0	AI/AO	Table 11
106	GNDR0	–	Table 15
107	TPFOP0	AO/AI	Table 11
108	TPFON0	AO/AI	Table 11
109	VCCT0/1	–	Table 15
110	TPFON1	AO/AI	Table 11
111	TPFOP1	AO/AI	Table 11
112	GNDR1	–	Table 15
113	GNDT0/1	–	Table 15
114	TPFIN1	AI/AO	Table 11
115	TPFIP1	AI/AO	Table 11
116	VCCR1	–	Table 15
117	VCCR2	–	Table 15
118	TPFIP2	AI/AO	Table 11
119	TPFIN2	AI/AO	Table 11
120	GNDR2	–	Table 15
121	TPFOP2	AO/AI	Table 11
122	TPFON2	AO/AI	Table 11
123	VCCT2/3	–	Table 15
124	TPFON3	AO/AI	Table 11
125	TPFOP3	AO/AI	Table 11
126	GNDR3	–	Table 15
127	GNDT2/3	–	Table 15
128	TPFIN3	AI/AO	Table 11
129	TPFIP3	AI/AO	Table 11

Pin	Symbol	Type[1]	Reference for Full Description
130	VCCR3	–	Table 15
131	VCCR4	–	Table 15
132	TPFIP4	AI/AO	Table 11
133	TPFIN4	AI/AO	Table 11
134	GNDT4/5	–	Table 15
135	GNDR4	–	Table 15
136	TPFOP4	AO/AI	Table 11
137	TPFON4	AO/AI	Table 11
138	VCCT4/5	–	Table 15
139	TPFON5	AO/AI	Table 11
140	TPFOP5	AO/AI	Table 11
141	GNDR5	–	Table 15
142	TPFIN5	AI/AO	Table 11
143	TPFIP5	AI/AO	Table 11
144	VCCR5	–	Table 15
145	VCCR6	–	Table 15
146	TPFIP6	AI/AO	Table 11
147	TPFIN6	AI/AO	Table 11
148	GNDT6/7	–	Table 15
149	GNDR6	–	Table 15
150	TPFOP6	AO/AI	Table 11
151	TPFON6	AO/AI	Table 11
152	VCCT6/7	–	Table 15
153	TPFON7	AO/AI	Table 11
154	TPFOP7	AO/AI	Table 11
155	GNDR7	–	Table 15
156	TPFIN7	AI/AO	Table 11
157	TPFIP7	AI/AO	Table 11
158	VCCR7	–	Table 15
159	NC	–	Table 17
160	NC	–	Table 17
161	SD4	I	Table 10
162	SD5	I	Table 10
163	GNDPECL	–	Table 15
164	VCCPECL	–	Table 15
165	SD6	I	Table 10
166	SD7	I	Table 10
167	TDI	I, ST, IP	Table 12
168	TDO	O, TS	Table 12
169	TMS	I, ST, IP	Table 12
170	TCK	I, ST, ID	Table 12
171	TRST_L	I, ST, IP	Table 12
172	NC	–	Table 17
173	G_FX/TP_L	I, ST, ID	Table 13
174	PWRDWN	I, ST, ID	Table 13
175	RESET_L	I, ST, IP	Table 13
176	Section	I, ST, ID	Table 13
177	ModeSel0	I, ST, ID	Table 13
178	ModeSel1	I, ST, ID	Table 13
179	SGND	–	Table 15
180	LED4_1_L	OD, TS, SL, IP	Table 14
181	LED4_2_L	OD, TS, SL, IP	Table 14
182	LED4_3_L	OD, TS, SL, IP	Table 14
183	GNDD	–	Table 15
184	VCCD	–	Table 15
185	LED5_1_L	OD, TS, SL, IP	Table 14
186	LED5_2_L	OD, TS, SL, IP	Table 14
187	LED5_3_L	OD, TS, SL, IP	Table 14
188	GNDIO	–	Table 15
189	LED6_1_L	OD, TS, SL, IP	Table 14
190	LED6_2_L	OD, TS, SL, IP	Table 14
191	LED6_3_L	OD, TS, SL, IP	Table 14
192	LED7_1_L	OD, TS, SL, IP	Table 14

Pin	Symbol	Type[1]	Reference for Full Description
193	LED7_2_L	OD, TS, SL, IP	Table 14
194	LED7_3_L	OD, TS, SL, IP	Table 5
195	GNDD	–	Table 15
196	VCCD	–	Table 15
197	NC	O, TS, ID	Table 16
198	RxData7	O, TS	Table 6
199	GNDIO	–	Table 15
200	NC	–	Table 16
201	NC	–	Table 16
202	NC	–	Table 16
203	TxData7	I, ID	Table 6
204	SYNC1	I, ID	Table 5
205	NC	–	Table 16
206	RxData6	O, TS	Table 6
207	GNDIO	–	Table 15
208	VCCIO	–	Table 15

3.1.3 PQFP Pin Assignments – SS-SMII Configuration

Figure 4 and Table 4, *SS-SMII PQFP Pin List*, on page 32 provide the LXT9785/ LXT9785E SS-SMII PQFP pin assignments.

Figure 4 SS-SMII 208-Pin PQFP Assignments

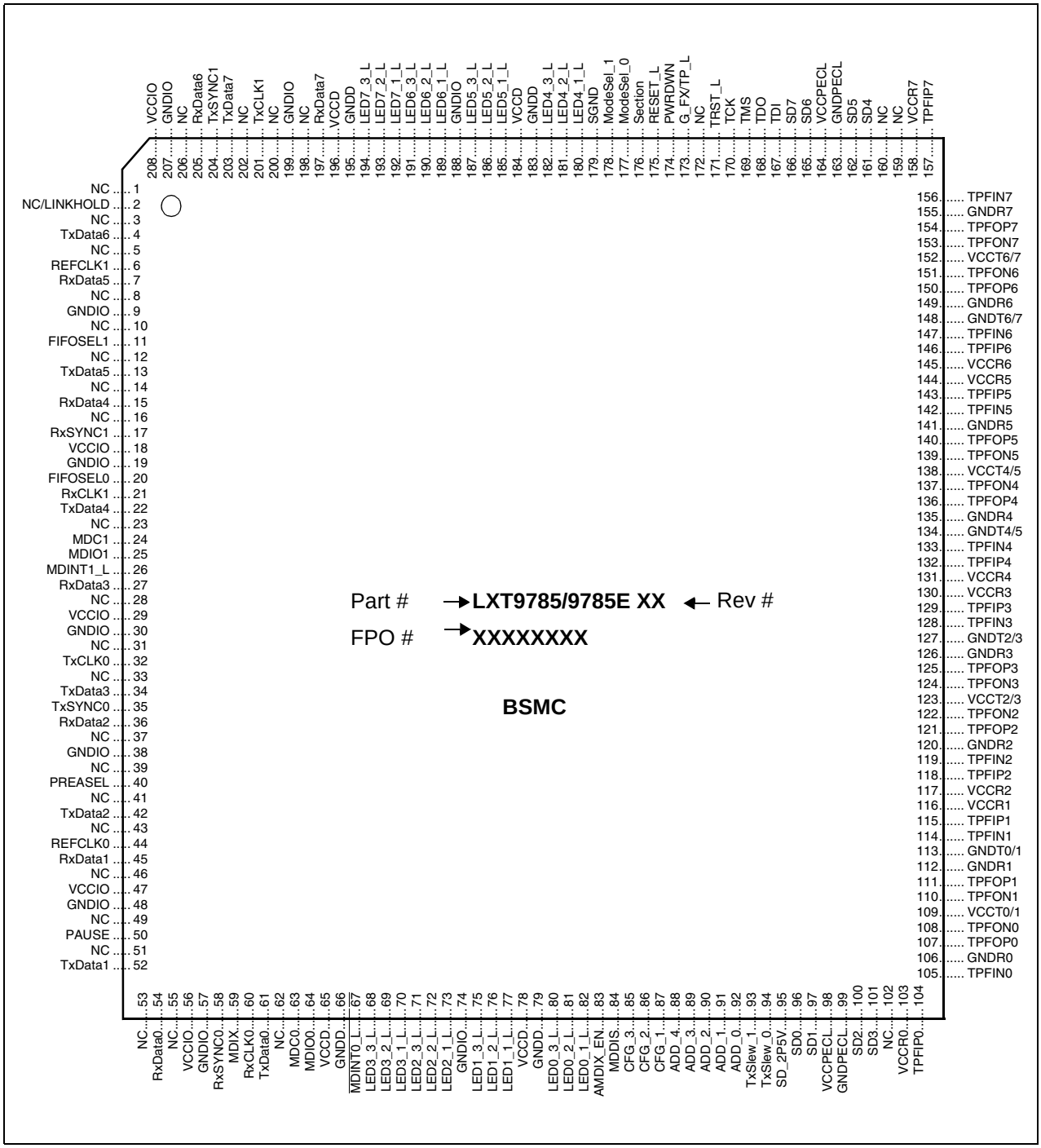


Table 4 SS-SMII PQFP Pin List

Pin	Symbol	Type[1]	Reference for Full Description
1	NC	–	Table 16
2	NC/ LINKHOLD	– I, ID	Table 16 Table 13
3	NC	–	Table 16
4	TxData6	I, ID	Table 6
5	NC	I	Table 16
6	REFCLK1	I	Table 6
7	RxData5	O, TS, ID	Table 8
8	NC	–	Table 16
9	GNDIO	–	Table 15
10	NC	–	Table 16
11	FIFOSEL1	I, ID, ST	Table 13
12	NC	–	Table 16
13	TxData5	I, ID	Table 6
14	NC	–	Table 16
15	RxData4	O, TS, ID	Table 8
16	NC	–	Table 16
17	RxSYNC1	O, TS, ID	Table 8
18	VCCIO	–	Table 15
19	GNDIO	–	Table 15
20	FIFOSEL0	I, ID, ST	Table 13
21	RxCLK1	O, TS, ID	Table 8
22	TxData4	I, ID	Table 6
23	NC	–	Table 16
24	MDC1	I, ST, ID	Table 9
25	MDIO1	I/O, TS, SL, IP	Table 9
26	MDINT1_L	OD, TS, SL, IP	Table 9
27	RxData3	O, TS, ID	Table 8
28	NC	–	Table 16
29	VCCIO	–	Table 15
30	GNDIO	–	Table 15
31	NC	–	Table 16
32	TxCLK0	I, ID	Table 8
33	NC	–	Table 16
34	TxData3	I, ID	Table 6
35	TxSYNC0	I, ID	Table 8
36	RxData2	O, TS, ID	Table 8
37	NC	–	Table 16
38	GNDIO	–	Table 15
39	NC	–	Table 16
40	PREASEL	I, ST	Table 13
41	NC	–	Table 16
42	TxData2	I, ID	Table 6
43	NC	–	Table 16
44	REFCLK0	I	Table 6
45	RxData1	O, TS, ID	Table 8
46	NC	–	Table 16
47	VCCIO	–	Table 15
48	GNDIO	–	Table 15
49	NC	–	Table 16
50	PAUSE	I, ID, ST	Table 13
51	NC	–	Table 16
52	TxData1	I, ID	Table 6
53	NC	–	Table 16
54	RxData0	O, TS, ID	Table 8
55	NC	–	Table 16
56	VCCIO	–	Table 15
57	GNDIO	–	Table 15
58	RxSYNC0	O, TS, ID	Table 8
59	MDIX	I, ID, ST	Table 13
60	RxCLK0	–	Table 8
61	TxData0	I, ID	Table 6
62	NC	–	Table 16
63	MDC0	I, ST, ID	Table 9
64	MDIO0	I/O, TS, SL, IP	Table 9
65	VCCD	–	Table 15
66	GNDD	–	Table 15
67	MDINT0_L	OD, TS, SL, IP	Table 9

Pin	Symbol	Type[1]	Reference for Full Description
68	LED3_3_L	OD, TS, SO, IP	Table 14
69	LED3_2_L	OD, TS, SL, IP	Table 14
70	LED3_1_L	OD, TS, SL, IP	Table 14
71	LED2_3_L	OD, TS, SL, IP	Table 14
72	LED2_2_L	OD, TS, SL, IP	Table 14
73	LED2_1_L	OD, TS, SL, IP	Table 14
74	GNDIO	–	Table 15
75	LED1_3_L	OD, TS, SL, IP	Table 14
76	LED1_2_L	OD, TS, SL, IP	Table 14
77	LED1_1_L	OD, TS, SL, IP	Table 14
78	VCCD	–	Table 15
79	GNDD	–	Table 15
80	LED0_3_L	OD, TS, SL, IP	Table 14
81	LED0_2_L	OD, TS, SL, IP	Table 14
82	LED0_1_L	OD, TS, SL, IP	Table 14
83	AMDIX_EN	I, ST, IP	Table 13
84	MDDIS	I, ST, ID	Table 9
85	CFG_3	I, ST, ID	Table 13
86	CFG_2	I, ST, ID	Table 13
87	CFG_1	I, ST, ID	Table 13
88	ADD_4	I, ST, ID	Table 13
89	ADD_3	I, ST, ID	Table 13
90	ADD_2	I, ST, ID	Table 13
91	ADD_1	I, ST, ID	Table 13
92	ADD_0	I, ST, ID	Table 13
93	TxSLEW_1	I, ST, ID	Table 13
94	TxSLEW_0	I, ST, ID	Table 13
95	SD_2P5V	I, ST, ID	Table 10
96	SD0	I	Table 10
97	SD1	I	Table 10
98	VCCPECL	–	Table 15
99	GNDPECL	–	Table 15
100	SD2	I	Table 10
101	SD3	I	Table 10
102	NC	–	Table 16
103	VCCR0	–	Table 15
104	TPFIP0	AI/AO	Table 11
105	TPFIN0	AI/AO	Table 11
106	GNDR0	–	Table 15
107	TPFOP0	AO/AI	Table 11
108	TPFON0	AO/AI	Table 11
109	VCCT0/1	–	Table 15
110	TPFON1	AO/AI	Table 11
111	TPFOP1	AO/AI	Table 11
112	GNDR1	–	Table 15
113	GNDT0/1	–	Table 15
114	TPFIN1	AI/AO	Table 11
115	TPFIP1	AI/AO	Table 11
116	VCCR1	–	Table 15
117	VCCR2	–	Table 15
118	TPFIP2	AI/AO	Table 11
119	TPFIN2	AI/AO	Table 11
120	GNDR2	–	Table 15
121	TPFOP2	AO/AI	Table 11
122	TPFON2	AO/AI	Table 11
123	VCCT2/3	–	Table 15
124	TPFON3	AO/AI	Table 11
125	TPFOP3	AO/AI	Table 11
126	GNDR3	–	Table 15
127	GNDT2/3	–	Table 15
128	TPFIN3	AI/AO	Table 11
129	TPFIP3	AI/AO	Table 11
130	VCCR3	–	Table 15
131	VCCR4	–	Table 15
132	TPFIP4	AI/AO	Table 11
133	TPFIN4	AI/AO	Table 11
134	GNDT4/5	–	Table 15
135	GNDR4	–	Table 15
136	TPFOP4	AO/AI	Table 11

Pin	Symbol	Type[1]	Reference for Full Description
137	TPFON4	AO/AI	Table 11
138	VCCT4/5	–	Table 15
139	TPFON5	AO/AI	Table 11
140	TPFOP5	AO/AI	Table 11
141	GNDR5	–	Table 15
142	TPFIN5	AI/AO	Table 11
143	TPFIP5	AI/AO	Table 11
144	VCCR5	–	Table 15
145	VCCR6	–	Table 15
146	TPFIP6	AI/AO	Table 11
147	TPFIN6	AI/AO	Table 11
148	GNDT6/7	–	Table 15
149	GNDR6	–	Table 15
150	TPFOP6	AO/AI	Table 11
151	TPFON6	AO/AI	Table 11
152	VCCT6/7	–	Table 15
153	TPFON7	AO/AI	Table 11
154	TPFOP7	AO/AI	Table 11
155	GNDR7	–	Table 15
156	TPFIN7	AI/AO	Table 11
157	TPFIP7	AI/AO	Table 11
158	VCCR7	–	Table 15
159	NC	–	Table 16
160	NC	–	Table 16
161	SD4	I	Table 10
162	SD5	I	Table 10
163	GNDPECL	–	Table 15
164	VCCPECL	–	Table 15
165	SD6	I	Table 10
166	SD7	I	Table 10
167	TDI	I, ST, IP	Table 12
168	TDO	O, TS	Table 12
169	TMS	I, ST, IP	Table 12
170	TCK	I, ST, ID	Table 12
171	TRST_L	I, ST, IP	Table 12
172	NC	–	Table 16
173	G_FX/TP_L	I, ST, ID	Table 13
174	PWRDWN	I, ST, ID	Table 13

Pin	Symbol	Type[1]	Reference for Full Description
175	RESET_L	I, ST, IP	Table 13
176	SECTION	I, ST, ID	Table 13
177	ModeSel0	I, ST, ID	Table 13
178	ModeSel1	I, ST, ID	Table 13
179	SGND	–	Table 15
180	LED4_1_L	OD, TS, SL, IP	Table 14
181	LED4_2_L	OD, TS, SL, IP	Table 14
182	LED4_3_L	OD, TS, SL, IP	Table 14
183	GNDD	–	Table 15
184	VCCD	–	Table 15
185	LED5_1_L	OD, TS, SL, IP	Table 14
186	LED5_2_L	OD, TS, SL, IP	Table 14
187	LED5_3_L	OD, TS, SL, IP	Table 14
188	GNDIO	–	Table 15
189	LED6_1_L	OD, TS, SL, IP	Table 14
190	LED6_2_L	OD, TS, SL, IP	Table 14
191	LED6_3_L	OD, TS, SL, IP	Table 14
192	LED7_1_L	OD, TS, SL, IP	Table 14
193	LED7_2_L	OD, TS, SL, IP	Table 14
194	LED7_3_L	OD, TS, SL, IP	Table 14
195	GNDD	–	Table 15
196	VCCD	–	Table 15
197	RxData7	O, TS, ID	Table 8
198	NC	–	Table 16
199	GNDIO	–	Table 15
200	NC	–	Table 16
201	TxCLK1	I, ID	Table 8
202	NC	–	Table 16
203	TxData7	I, ID	Table 6
204	TxSYNC1	I, ID	Table 8

Pin	Symbol	Type[1]	Reference for Full Description
205	RxData6	O, TS, ID	Table 8
206	NC	–	Table 16
207	GNDIO	–	Table 15
208	VCCIO	–	Table 15

3.2 PQFP Signal Descriptions

3.2.1 Signal Name Conventions

Signal names may contain either a port designation or a serial designation, or a combination of the two designations. Signal naming conventions are as follows:

- **Port Number Only.** Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by the Port Designation. For example, Transmit Enable signals would be identified as TxEN0, TxEN1, and TxEN2.
- **Serial Number Only.** A set of signals which are not tied to any specific port are designated by the Signal Mnemonic, followed by an underscore and a serial designation. For example, a set of three Global Configuration signals would be identified as CFG_1, CFG_2, and CFG_3.
- **Port and Serial Number.** In cases where each port is assigned a set of multiple signals, each signal is designated in the following order: Signal Mnemonic, Port Designation, an underscore, and the serial designation. For example, a set of three Port Configuration signals would be identified as RxData0_0 and RxData0_1, RxData1_0 and RxData1_1, and RxData2_0 and RxData2_1.

3.2.2 PQFP Signal Descriptions – RMII, SMII, and SS-SMII Configurations

Table 5 through Table 17, *Receive FIFO Depth Considerations*, on page 50 provide PQFP signal descriptions. Ball designations are included for cross-reference.

Table 5 RMII Signal Descriptions – PQFP (Sheet 1 of 3)

Pin-Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
44 6	E6, E12	REFCLK0 REFCLK1	I	**Reference Clock.** 50 MHz RMII reference clock is always required. RMII inputs are sampled on the rising edge of REFCLK, RMII outputs are sourced on the falling edge.
61 62	E2, F4	TxData0_0 TxData0_1	I, ID	**Transmit Data - Port 0.** Inputs containing 2-bit parallel di-bits to be transmitted from port 0 are clocked in synchronously to REFCLK.
52 53	C3, D4	TxData1_0 TxData1_1	I, ID	**Transmit Data - Port 1.** Inputs containing 2-bit parallel di-bits to be transmitted from port 1 are clocked in synchronously to REFCLK
42 43	B5 A4	TxData2_0 TxData2_1	I, ID	**Transmit Data - Port 2.** Inputs containing 2-bit parallel di-bits to be transmitted from port 2 are clocked in synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 5 RMII Signal Descriptions – PQFP (Sheet 2 of 3)

Pin-Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
34 35	D8, A6	TxData3_0 TxData3_1	I, ID	**Transmit Data - Port 3.** Inputs containing 2-bit parallel di-bits to be transmitted from port 3 are clocked in synchronously to REFCLK.
22 23	A11, C10	TxData4_0 TxData4_1	I, ID	**Transmit Data - Port 4.** Inputs containing 2-bit parallel di-bits to be transmitted from port 4 are clocked in synchronously to REFCLK.
13 14	B13, D11	TxData5_0 TxData5_1	I, ID	**Transmit Data - Port 5.** Inputs containing 2-bit parallel di-bits to be transmitted from port 5 are clocked in synchronously to REFCLK.
4 5	D13, A16	TxData6_0 TxData6_1	I, ID	**Transmit Data - Port 6.** Inputs containing 2-bit parallel di-bits to be transmitted from port 6 are clocked in synchronously to REFCLK.
203 204	E14, C16	TxData7_0 TxData7_1	I, ID	**Transmit Data - Port 7.** Inputs containing 2-bit parallel di-bits to be transmitted from port 7 are clocked in synchronously to REFCLK.
60 51 41 33 21 12 3 202	E3, B2, C6, A7, B11, A14, C14, D16	TxEN0 TxEN1 TxEN2 TxEN3 TxEN4 TxEN5 TxEN6 TxEN7	I, ID	**Transmit Enable - Ports 0-7.** Active High input enables respective port transmitter. This signal must be synchronous to the REFCLK.
55 54	C2, B1	RxData0_0 RxData0_1	O, TS O, TS, ID	**Receive Data - Port 0.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
46 45	A3, B4	RxData1_0 RxData1_1	O, TS O, TS, ID	**Receive Data - Port 1.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
37 36	B6, C7	RxData2_0 RxData2_1	O, TS O, TS, ID	**Receive Data - Port 2.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
28 27	D9, B9	RxData3_0 RxData3_1	O, TS O, TS, ID	**Receive Data - Port 3.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
16 15	A13, C12	RxData4_0 RxData4_1	O, TS O, TS, ID	**Receive Data - Port 4.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
8 7	B14, B15	RxData5_0 RxData5_1	O, TS O, TS, ID	**Receive Data - Port 5.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 5 RMII Signal Descriptions – PQFP (Sheet 3 of 3)

Pin-Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
206 205	C15, B17	RxData6_0 RxData6_1	O, TS O, TS, ID	**Receive Data - Port 6.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
198 197	E16, F14	RxData7_0 RxData7_1	O, TS O, TS, ID	**Receive Data - Port 7.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
58 49 39 31 17 10 1 200	E4, C4, A5, B8, B12, D12, B16, E15	CRS_DV0 CRS_DV1 CRS_DV2 CRS_DV3 CRS_DV4 CRS_DV5 CRS_DV6 CRS_DV7	O, TS, SL, ID	**Carrier Sense/Receive Data Valid - Ports 0-7.** On detection of valid carrier, these signals are asserted asynchronously with respect to REFCLK. CRS_DVn is de-asserted on loss of carrier, synchronous to REFCLK.
59 50 40 32 20 11 2 201	D2, D5, D7, C8, A12, A15, A17, D17	RxER0 RxER1 RxER2 RxER3 RxER4 RxER5 RxER6 RxER7	O, TS, SL, ID	**Receive Error - Ports 0-7.** These signals are synchronous to the respective REFCLK. Active High indicates that received code group is invalid, or that PLL is not locked. The RxER signals have the following additional function pins: RxER0 (MDIX) RxER1 (PAUSE) RxER2 (PREASEL) RxER4 (FIFOSEL0) RxER5 (FIFOSEL1) RxER6 (LINKHOLD)

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 6 SMII/SS-SMII Common Signal Descriptions – PQFP

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
61 52 42 34 22 13 4 203	E2, C3, B5, D8, A11, B13, D13, E14	TxData0 TxData1 TxData2 TxData3 TxData4 TxData5 TxData6 TxData7	I, ID	**Transmit Data - Ports 0-7.** These serial input streams provide data to be transmitted to the network. The LXT9785/LXT9785E clocks the data in synchronously to REFCLK.
44 6	E6, E12	REFCLK0 REFCLK1	I	**Reference Clock.** The LXT9785/LXT9785E always requires a 125 MHz reference clock input. Refer to Functional Description for detailed clock requirements. REFCLK0 and REFCLK1 are always connected regardless of sectionalization mode.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.

Table 7 SMII Specific Signal Descriptions – PQFP

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
35 204	A6, C16	SYNC0 SYNC1	I, ID	**SMII Synchronization.** The MAC must generate a SYNC pulse every 10 REFCLK cycles to synchronize the SMII. SYNC0 is used when 1x8 port sectionalization is selected. SYNC0 and SYNC1 are to be used when 2x4 port sectionalization is chosen.
55 46 37 28 16 8 206 198	C2, A3, B6, D9, A13, B14, C15, E16	RxData0 RxData1 RxData2 RxData3 RxData4 RxData5 RxData6 RxData7	O, TS	**Receive Data - Ports 0-7**. These serial output streams provide data received from the network. The LXT9785/LXT9785E drives the data out synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.
3. RxData[0:7] outputs are three-stated in Isolation and hardware power-down modes and during hardware reset.

Table 8 SS-SMII Specific Signal Descriptions – PQFP

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
35 204	A6, C16	TxSYNC0 TxSYNC1	I, ID	**SS-SMII Transmit Synchronization.** The MAC must generate a TxSYNC pulse every 10 TxCLK cycles to mark the start of TxData segments. TxSYNC0 is used when 1x8 port sectionalization is selected.
58 17	E4, B12	RxSYNC0 RxSYNC1	O, TS, ID	**SS-SMII Receive Synchronization.** The LXT9785/LXT9785E generates these pulses every 10 RxCLK cycles to mark the start of RxData segments for the MAC. RxSYNC1 is used when 1x8 port sectionalization is selected. RxSYNC0 may not be used. These outputs are only enabled when SS-SMII mode is enabled.
32 201	C8, D17	TxCLK0 TxCLK1	I, ID	**SS-SMII Transmit Clock.** The MAC sources this 125 MHz clock as the timing reference for TxData and TxSYNC. Only TxCLK0 is used when 1x8 port sectionalization is selected. See Section 4.4.2, *Clock/SYNC Requirements*, on page 122 for detailed clock requirements.
60 21	E3, B11	RxCLK0 RxCLK1	O, TS, ID	**SS-SMII Receive Clock.** The LXT9785/LXT9785E generates these clocks, based on REFCLK, to provide a timing reference for RxData and RxSYNC to the MAC. RxCLK1 is used when 1x8 port sectionalization is selected. RxCLK0 may not be used. See Section 4.4.2, *Clock/SYNC Requirements*, on page 122 for detailed clock requirements. These outputs are only enabled when SS-SMII mode is enabled.
54 45 36 27 15 7 205 197	B1, B4, C7, B9, C12, B15, B17, F14	RxData0 RxData1 RxData2 RxData3 RxData4 RxData5 RxData6 RxData7	O, TS, ID	**Receive Data - Ports 0-7.** These serial output streams provide data received from the network. The LXT9785/LXT9785E drives the data out synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7], RxSYNC[0:1], and RxCLK[0:1] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 9 MDIO Control Interface Signals – PQFP

Pin / Ball Designation		Symbol	Type[1]	Signal Description[2,3,4]
PQFP	PBGA			
64 25	F3, A10	MDIO0 MDIO1	I/O, TS, SL, IP	**Management Data Input/Output.** Bidirectional serial data channel for communication between the PHY and MAC or switch ASIC. Only MDIO0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDIO0 accesses ports 0-3 and MDIO1 accesses ports 4-7. Refer to Figure 21 on page 136.
67 26	F1, C9	MDINT0_L MDINT1_L	OD,TS, SL, IP	**Management Data Interrupt.** When Register bit 18.1 = 1, an active Low output on this Pin indicates status change. Only MDINT0_L is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDINT0_L is associated with ports 0-3 and MDINT1_L is associated with ports 4-7. Refer to Figure 21 on page 136.
63 24	E1, B10	MDC0 MDC1	I, ST, ID	**Management Data Clock.** Clock for the MDIO serial data channel. Maximum frequency is 20 MHz. Only MDC0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDC0 clocks ports 0-3 register accesses and MDC1 clocks ports 4-7 register accesses. Refer to Figure 21 on page 136.
84	L1	MDDIS	I, ST, ID	**Management Disable.** When MDDIS is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power up and reset. When MDDIS is pulled Low at power up or reset, via the internal pull-down resistor or by tying it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. MDIO[0:1] and MDINT[0:1] outputs are three-stated in H/W Power-Down mode and during H/W reset.
4. Supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 10 Signal Detect – PQFP

Pin/Ball Designation		Symbol	Type[1]	Signal Description2,3
PQFP	PBGA			
95	P1	SD_2P5V	I, ST, ID	**Signal Detect 2.5 Volt Interface.** SD input threshold voltage select. **Tie to VCCPECL =** Select 2.5 V LVPECL input levels **Float or Tie to GNDPECL =** Select 3.3 V LVPECL input levels
96 97 100 101 161 162 165 166	P2, N4, P3, N5, P15, P16, P17, N17	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	I	**Signal Detect - Ports 0-7.** Signal Detect input from the fiber transceiver (these inputs are only active for ports operating in fiber mode). **Logic High =** Normal operation (the process of searching for receive idles for the purpose of bringing link up is initiated) **Logic Low =** Link is declared lost

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.
3. Tie SD[0:7] inputs to GNDPECL if unused.

Table 11 Network Interface Signal Descriptions – PQFP

Pin/Ball Designation		Symbol	Type[1]	Signal Description
PQFP	PBGA			
107, 108 111, 110 121, 122 125, 124 136, 137 140, 139 150, 151 154, 153	T2, U1, T3, R4, T6, U5, U7, T7, T10, R10, T11, U11, T14,U15, R14, T15	TPFOP0, TPFON0 TPFOP1, TPFON1 TPFOP2, TPFON2 TPFOP3, TPFON3 TPFOP4, TPFON4 TPFOP5, TPFON5 TPFOP6, TPFON6 TPFOP7, TPFON7	AO/AI	**Twisted-Pair/Fiber Outputs[2], Positive & Negative, Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPFO pins drive 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFO pins produce differential LVPECL outputs for fiber transceivers.
104, 105 115, 114 118, 119 129, 128 132, 133 143, 142 146, 147 157, 156	R2, T1, U3, T4, R6, T5, T8, R8, T9, U9, U13, T12, R12, T13, R16, T16	TPFIP0, TPFIN0 TPFIP1, TPFIN1 TPFIP2, TPFIN2 TPFIP3, TPFIN3 TPFIP4, TPFIN4 TPFIP5, TPFIN5 TPFIP6, TPFIN6 TPFIP7, TPFIN7	AI/AO	**Twisted-Pair/Fiber Inputs[3], Positive & Negative, Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPFI pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFI pins receive differential LVPECL inputs from fiber transceivers.

1. Type Column Coding: AI = Analog Input, AO = Analog Output.
2. Switched to Inputs (see TPFIP/N description) when not in fiber mode and MDIX is not active [that is, twisted-pair, non-crossover MDI mode].
3. Switched to Outputs (see TPFOP/N description) when not in fiber mode and MDIX is not active [that is, twisted-pair, non-crossover MDI mode].

Table 12 JTAG Test Signal Descriptions – PQFP

Pin / Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
167	N14	TDI	I, ST, IP	**Test Data Input.** Test data sampled with respect to the rising edge of TCK.
168	N15	TDO	O, TS	**Test Data Output.** Test data driven with respect to the falling edge of TCK.
169	N16	TMS	I, ST, IP	**Test Mode Select.**
170	M16	TCK	I, ST, ID	**Test Clock.** Clock input for JTAG test.
171	M17	TRST	I, ST, IP	**Test Reset.** Reset input for JTAG test.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain, TS = Three-State-able output, SMT = Schmitt Triggered input, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. TDO output is three-stated in H/W Power-Down mode and during H/W reset.

Table 13 Miscellaneous Signal Descriptions – PQFP (Sheet 1 of 4)

Pin / Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
94 93	N3, M4	TxSLEW_0 TxSLEW_1	I, ST, ID	**Tx Output Slew Controls 0 and 1 Defaults.** These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 27.11:10 for all ports. These register bits can be read and overwritten after startup / reset. These pins select the TX output slew rate for all ports (rise and fall time) as follows:

TxSLEW_1	TxSLEW_0	Slew Rate (Rise and Fall Time)
0	0	3.3 ns
0	1	3.6 ns
1	0	3.9 ns
1	1	4.2 ns

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 13 Miscellaneous Signal Descriptions – PQFP (Sheet 2 of 4)

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
50	D5	PAUSE	I, ID, ST	**Pause Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 4.10 for all ports. This register bit can be read and overwritten after startup / reset. When High, the LXT9785/LXT9785E advertises Pause capabilities on all ports during auto-negotiation. This pin is shared with RMII-RxER1. An external pull-up resistor (see applications section for value) can be used to set Pause active while RxER1 is three-stated during H/W reset. If no pull-up is used, the default Pause state is set inactive via the internal pull-down resistor.
174	L14	PWRDWN	I, ST, ID	**Power-Down.** When High, forces the LXT9785/LXT9785E into global power-down mode. Pin is not on JTAG chain.
175	M15	RESET_L	I, ST, IP	**Reset.** This active low input is ORed with the control register Reset Register bit 0.15. When held Low, all outputs are forced to inactive state. Pin is not on JTAG chain.
88 89 90 91 92	L4, M2, M3, N1, N2	ADD_4 ADD_3 ADD_2 ADD_1 ADD_0	I, ST, ID	**Address <4:0>.** Sets base address. Each port adds its port number (starting with 0) to this address to determine its PHY address. Port 0 Address = Base Port 1 Address = Base + 1 Port 2 Address = Base + 2 Port 3 Address = Base + 3 Port 4 Address = Base + 4 Port 5 Address = Base + 5 Port 6 Address = Base + 6 Port 7 Address = Base + 7
178 177	L17, L16	MODESEL_1 MODESEL_0	I, ST, ID	**Mode Select[1:0].** 00 = RMII 01 = SMII 10 = SS-SMII 11 = Reserved All ports are configured the same. Interfaces cannot be mixed and must be all RMII, SMII, or SS-SMII.
176	L15	SECTION	I, ST, ID	**Sectionalization Select.** This pin selects sectionalization into separate ports. 0 = 1x8 ports, 1 = 2x4 ports

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 13 Miscellaneous Signal Descriptions – PQFP (Sheet 3 of 4)

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
83	K1	AMDIX_EN	I, ST, IP	**Auto MDIX Enable Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.9 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 40 on page 116. When active (High), automatic MDI crossover (MDIX) (regardless of segmentation) is selected for all ports. When inactive (Low) MDIX is selected according to the MDIX pin.
59	D2	MDIX	I, ID, ST	**MDIX Select Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.8 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 40, *MDIX Selection*, on page 116. When AMDIX_EN is active this pin is ignored. When AMDIX_EN is inactive, all ports are forced to the MDI or the MDIX function regardless of segmentation. If this pin is active (high), MDI crossover (MDIX) is selected. If this pin is inactive, non-crossover MDI mode is set. This pin is shared with RMII-RxER0. An external pull-up resistor (see applications section for value) can be used to set MDIX active while RxER0 is three-stated during H/W reset. If no pull-up is used, the default MDIX state is set inactive via the internal pull-down resistor. Do not tie this pin directly to VCCIO (vs. using a pull-up) in non-RMII modes.
85 86 87	L2, L3, M1	CFG_3 CFG_2 CFG_1	I, ST, ID	**Global Port Configuration Defaults 1-3.** These pins are read at startup or reset. Their value at that time is used to set the default state of register bits shown in Table 42, *Global Hardware Configuration Settings*, on page 126 for all ports. These register bits can be read and overwritten after startup / reset. When operating in Hardware Control Mode, these pins provide configuration control options for all the ports (refer to page 126 for details).
173	M14	G_FX/TP_L	I, ST, ID	**Global FX/TP_L Enable Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 16.0 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 93, *Port Configuration Register (Address 16, Hex 10)*, on page 199. This input selects whether all the ports are defaulted to TP vs. FX mode.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 13 Miscellaneous Signal Descriptions – PQFP (Sheet 4 of 4)

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2]
PQFP	PBGA			
11 20	A15 A12	FIFOSEL1 FIFOSEL0	I, ID, ST	**FIFO Select <1:0>.** These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 18.15:14 for all ports. These register bits can be read and overwritten after startup/reset. These pins are shared with RMII-RxER<5:4>. An external pull-up resistor (see applications section for value) can be used to set FIFO Select<1:0> to active while RxER<5:4> are three-stated during hardware reset. If no pull-up is used, the default FIFO select state is set via the internal pull-down resistors. See Table 17, *Receive FIFO Depth Considerations*, on page 50.
40	D7	PREASEL	I, ID, ST	**Preamble Select.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 16.5 for all ports. This register bit can be read and overwritten after startup/reset. This pin is shared with RMII-RxER2. An external pull-up resistor (see applications section for value) can be used to set Preamble Select to active while RxER2 is three-stated during hardware reset. If no pull-up is used, the default Preamble Select state is set via the internal pull-down resistors. **Note:** Preamble select has no effect in 100 Mbps operation.
2	A17	LINKHOLD[3]	ID	**LINKHOLD Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 0.11 for all ports. This register bit can be read and overwritten after startup / reset. When High, the LXT9785/LXT9785E powers down all ports. This pin is shared with RMII-RxER6. An external pull-up resistor (see applications section for value) can be used to set LINKHOLD active while RxER6 is tri-stated during H/W reset. If no pull-up is used, the default LINKHOLD state is set inactive via the internal pull-down resistor.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 14 LED Signal Descriptions – PQFP (Sheet 1 of 2)

Pin / Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
82 81 80	K3, K2, J1	LED0_1_L LED0_2_L LED0_3_L	OD, TS, SL, IP	**Port 0 LED Drivers 1-3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
77 76 75	J4, J3, H1	LED1_1_L LED1_2_L LED1_3_L	OD, TS, SL, IP	**Port 1 LED Drivers 1-3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
73 72 71	H2, H3, G1	LED2_1_L LED2_2_L LED2_3_L	OD, TS, SL, IP	**Port 2 LED Drivers 1-3.** These pins drive LED indicators for Port 2. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
70 69 68	F2, G3, G4	LED3_1_L LED3_2_L LED3_3_L	OD, TS, SL, IP	**Port 3 LED Drivers 1-3.** These pins drive LED indicators for Port 3. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
180 181 182	K16, K17, J17	LED4_1_L LED4_2_L LED4_3_L	OD, TS, SL, IP	**Port 4 LED Drivers 1-3.** These pins drive LED indicators for Port 4. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. The LED outputs are three-stated in H/W Power-Down mode and during H/W reset.

Table 14 LED Signal Descriptions – PQFP (Sheet 2 of 2)

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
PQFP	PBGA			
185 186 187	J15, J16, H17	LED5_1_L LED5_2_L LED5_3_L	OD, TS, SL, IP	**Port 5 LED Drivers 1-3.** These pins drive LED indicators for Port 5. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
189 190 191	H15, H16, G17	LED6_1_L LED6_2_L LED6_3_L	OD, TS, SL, IP	**Port 6 LED Drivers 1-3.** These pins drive LED indicators for Port 6. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
192 193 194	G15, F17, F16	LED7_1_L LED7_2_L LED7_3_L	OD, TS, SL, IP	**Port 7 LED Drivers 1-3.** These pins drive LED indicators for Port 7. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. The LED outputs are three-stated in H/W Power-Down mode and during H/W reset.

Table 15 Power Supply Signal Descriptions – PQFP (Sheet 1 of 2)

Pin/Ball Designation		Symbol	Type	Signal Description
PQFP	PBGA			
65, 78, 184, 196	G13, J14, F5, J5	VCCD	-	**Digital Power Supply - Core.** +2.5 V supply for core digital circuits.
18, 29, 47, 56, 208	A2, A8, C1, C11, D14	VCCIO	-	**Digital Power Supply - I/O Ring.** +2.5/3.3 V supply for digital I/O circuits. The digital input circuits running off of this rail, having a TTL-level threshold and over-voltage protection, may be interfaced with 3.3/5.0 V, when the IO supply is 3.3 V, and 2.5/3.3/5.0 V when 2.5 V.
98, 164	L13, L5	VCCPECL	-	**Digital Power Supply - PECL Signal Detect Inputs.** +2.5/3.3 V supply for PECL Signal Detect input circuits. If Fiber Mode is not used (that is, G_FX/TP_L is pulled Low), the VCCPECL pins may be tied to GNDPECL to save power.
103, 116, 117, 130, 131, 144, 145, 158	N13, P4, P7, P8, P9, P10, P11, P12	VCCR	-	**Analog Power Supply - Receive.** +2.5 V supply for all analog receive circuits.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 15 Power Supply Signal Descriptions – PQFP (Sheet 2 of 2)

Pin/Ball Designation		Symbol	Type	Signal Description
PQFP	PBGA			
109, 123, 138, 152	N6, N7, N9, N11, N12	VCCT	-	**Analog Power Supply - Transmit.** +2.5 V supply for all analog transmit circuits.
66, 79, 183, 195	A1, A9, B3, B7, C5, C13, C17, D1, D3, D6, D10, D15, E5, E7, E9, E11, E13, E17, F13, H8, H9, H10, J8, J9, J10, K8, K9, K10	GNDD	-	**Digital Ground.** Ground return for core digital supplies (VCCD). All ground pins can be tied together using a single ground plane.
9, 19, 30, 38, 48, 57, 74, 188, 199, 207	–	GNDIO	-	**Digital GND - I/O Ring.** Ground return for digital I/O circuits (VCCIO).
99, 163	M5, M13	GNDPECL	-	**Digital GND - PECL Signal Detect Inputs.** Ground return for PECL Signal Detect input circuits.
106, 112, 120, 126, 135, 141, 149, 155	P5, P6, P13, R7, R9, R11, R13, U8	GNDR	-	**Analog Ground - Receive.** Ground return for receive analog supply. All ground pins can be tied together using a single ground plane.
113, 127, 134, 148	P14, R1, R3, R5, R15, R17, T17, U2, U4, U6, U10, U12, U14, U16, U17	GNDT	-	**Analog Ground - Transmit.** Ground return for transmit analog supply. All ground pins can be tied together using a single ground plane.
179	K14	SGND	-	**Substrate Ground.** Ground for chip substrate. All ground pins can be tied together using a single ground plane.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 16 Unused/Reserved Pins – PQFP

Pin/Ball Designation		Symbol	Type[1]	Signal Description
PQFP	PBGA			
NC	F15, G2, G5, G14, G16, H4, H14, J2, J13, K4, K15	NC	–	No Connection.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 17 Receive FIFO Depth Considerations

FIFOSEL1	FIFOSEL0	Register 18.15 Value	Register 18.14 Value
0	0	1	0
0	1	1	1
1	0	0	0
1	1	0	1

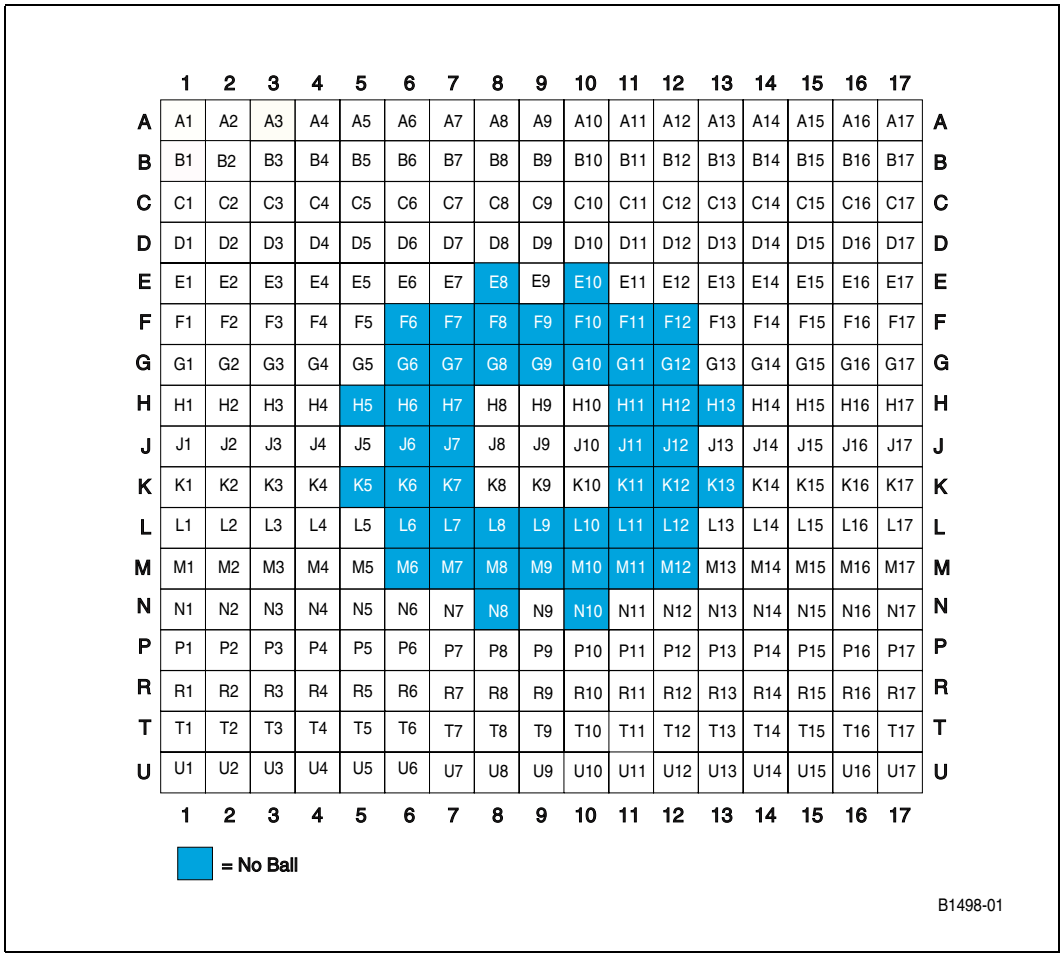
3.3 BGA23 Ball Assignments

The following sections provide BGA23 ball location and signal description information for RMII, SMII, and SS-SMII:

- 3.3.1, *RMII BGA23 Ball List*, on page 52
- 3.3.2, *SMII BGA23 Ball List*, on page 61
- 3.3.3, *SS-SMII BGA23 Ball List*, on page 70
- 3.4, *BGA23 Signal Descriptions*, on page 79

Figure 5 illustrates the LXT9785/LXT9785E 241-ball BGA23 ball locations for RMII, SMII, and SS-SMII.

Figure 5 241-Ball BGA23 Assignments (Top View)



3.3.1 RMII BGA23 Ball List

The following tables provide the RMII BGA23 ball locations and signal names arranged in alphanumeric order as follows:

- Table 18, *RMII BGA23 Ball List in Alphanumeric Order by Signal Name*
- Table 19, *RMII BGA23 Ball List in Alphanumeric Order by Ball Location*, on page 57

Table 18 RMII BGA23 Ball List in Alphanumeric Order by Signal Name

Signal	Ball	Type[1]	Reference for Full Description
ADD_0	N2	I, ST, ID	Table 32
ADD_1	N1	I, ST, ID	Table 32
ADD_2	M3	I, ST, ID	Table 32
ADD_3	M2	I, ST, ID	Table 32
ADD_4	L4	I, ST, ID	Table 32
AMDIX_EN	K1	I, ST, IP	Table 32
CFG_1	M1	I, ST, ID	Table 32
CFG_2	L3	I, ST, ID	Table 32
CFG_3	L2	I, ST, ID	Table 32
CRS_DV0	E4	O, TS, SL, ID	Table 24
CRS_DV1	C4	O, TS, SL, ID	Table 24
CRS_DV2	A5	O, TS, SL, ID	Table 24
CRS_DV3	B8	O, TS, SL, ID	Table 24
CRS_DV4	B12	O, TS, SL, ID	Table 24
CRS_DV5	D12	O, TS, SL, ID	Table 24
CRS_DV6	B16	O, TS, SL, ID	Table 24
CRS_DV7	E15	O, TS, SL, ID	Table 24
G_FX/TP_L	M14	I, ST, ID	Table 32
GNDD	A1	–	Table 34
GNDD	A9	–	Table 34
GNDD	B3	–	Table 34
GNDD	B7	–	Table 34
GNDD	C5	–	Table 34
GNDD	C13	–	Table 34
GNDD	C17	–	Table 34
GNDD	D1	–	Table 34
GNDD	D3	–	Table 34
GNDD	D6	–	Table 34
GNDD	D10	–	Table 34
GNDD	D15	–	Table 34
GNDD	E5	–	Table 34
GNDD	E7	–	Table 34
GNDD	E9	–	Table 34
GNDD	E11	–	Table 34
GNDD	E13	–	Table 34
GNDD	E17	–	Table 34
GNDD	F13	–	Table 34
GNDD	H8	–	Table 34
GNDD	H9	–	Table 34
GNDD	H10	–	Table 34
GNDD	J8	–	Table 34
GNDD	J9	–	Table 34
GNDD	J10	–	Table 34
GNDD	K8	–	Table 34
GNDD	K9	–	Table 34
GNDD	K10	–	Table 34
GNDPECL	M5	–	Table 34
GNDPECL	M13	–	Table 34
GNDR	P5	–	Table 34
GNDR	P6	–	Table 34
GNDR	P13	–	Table 34
GNDR	R7	–	Table 34
GNDR	R9	–	Table 34
GNDR	R11	–	Table 34
GNDR	R13	–	Table 34
GNDR	U8	–	Table 34
GNDT	P14	–	Table 34

Signal	Ball	Type[1]	Reference for Full Description
GNDT	R1	–	Table 34
GNDT	R3	–	Table 34
GNDT	R5	–	Table 34
GNDT	R15	–	Table 34
GNDT	R17	–	Table 34
GNDT	T17	–	Table 34
GNDT	U2	–	Table 34
GNDT	U4	–	Table 34
GNDT	U6	–	Table 34
GNDT	U10	–	Table 34
GNDT	U12	–	Table 34
GNDT	U14	–	Table 34
GNDT	U16	–	Table 34
GNDT	U17	–	Table 34
LED0_1_L	K3	OD, TS, SL, IP	Table 33
LED0_2_L	K2	OD, TS, SL, IP	Table 33
LED0_3_L	J1	OD, TS, SL, IP	Table 33
LED1_1_L	J4	OD, TS, SL, IP	Table 33
LED1_2_L	J3	OD, TS, SL, IP	Table 33
LED1_3_L	H1	OD, TS, SL, IP	Table 33
LED2_1_L	H2	OD, TS, SL, IP	Table 33
LED2_2_L	H3	OD, TS, SL, IP	Table 33
LED2_3_L	G1	OD, TS, SL, IP	Table 33
LED3_1_L	F2	OD, TS, SL, IP	Table 33
LED3_2_L	G3	OD, TS, SL, IP	Table 33
LED3_3_L	G4	OD, TS, SO, IP	Table 33
LED4_1_L	K16	OD, TS, SL, IP	Table 33
LED4_2_L	K17	OD, TS, SL, IP	Table 33
LED4_3_L	J17	OD, TS, SL, IP	Table 33
LED5_1_L	J15	OD, TS, SL, IP	Table 33
LED5_2_L	J16	OD, TS, SL, IP	Table 33
LED5_3_L	H17	OD, TS, SL, IP	Table 33
LED6_1_L	H15	OD, TS, SL, IP	Table 33
LED6_2_L	H16	OD, TS, SL, IP	Table 33
LED6_3_L	G17	OD, TS, SL, IP	Table 33
LED7_1_L	G15	OD, TS, SL, IP	Table 33
LED7_2_L	F17	OD, TS, SL, IP	Table 33
LED7_3_L	F16	OD, TS, SL, IP	Table 33
MDC0	E1	I, ST, ID	Table 28
MDC1	B10	I, ST, ID	Table 28
MDDIS	L1	I, ST, ID	Table 28
MDINT0_L	F1	OD, TS, SL, IP	Table 28
MDINT1_L	C9	OD, TS, SL, IP	Table 28
MDIO0	F3	I/O, TS, SL, IP	Table 28
MDIO1	A10	I/O, TS, SL, IP	Table 28
ModeSel0	L16	I, ST, ID	Table 32
ModeSel1	L17	I, ST, ID	Table 32
NC	F15	–	Table 35
NC	G2	–	Table 35
NC	G5	–	Table 35
NC	G14	–	Table 35
NC	G16	–	Table 35
NC	H4	–	Table 35
NC	H14	–	Table 35
NC	J2	–	Table 35
NC	J13	–	Table 35
NC	K4	–	Table 35
NC	K15	–	Table 35
No ball	F6	–	–

Signal	Ball	Type[1]	Reference for Full Description
No ball	F7	–	–
No ball	F8	–	–
No Ball	E8	–	–
No Ball	E10		
No Ball	F9	–	–
No Ball	F10	–	–
No Ball	F11	–	–
No Ball	F12	–	–
No Ball	G6	–	–
No Ball	G7	–	–
No Ball	G8	–	–
No Ball	G9	–	–
No Ball	G10	–	–
No Ball	G11	–	–
No Ball	G12	–	–
No Ball	H5	–	–
No Ball	H6	–	–
No Ball	H7	–	–
No Ball	H11	–	–
No Ball	H12	–	–
No Ball	H13	–	–
No Ball	J6	–	–
No Ball	J7	–	–
No Ball	J11	–	–
No Ball	J12	–	–
No Ball	K5	–	–
No Ball	K6	–	–
No Ball	K7	–	–
No Ball	K11	–	–
No Ball	K12	–	–
No Ball	K13	–	–
No Ball	L6	–	–
No Ball	L7	–	–
No Ball	L8	–	–
No Ball	L9	–	–
No Ball	L10	–	–
No Ball	L11	–	–
No Ball	L11	–	–

Signal	Ball	Type[1]	Reference for Full Description
No Ball	M6	–	–
No Ball	M7	–	–
No Ball	M8	–	–
No Ball	M9	–	–
No Ball	M10	–	–
No Ball	M11	–	–
No Ball	M12	–	–
No Ball	N8	–	–
No Ball	N10	–	–
PWRDWN	L14	I, ST, ID	Table 32
REFCLK0	E6	I	Table 24
REFCLK1	E12	I	Table 24
RESET_L	M15	I, ST, IP	Table 32
RxData0_0	C2	O, TS	Table 24
RxData0_1	B1	O, TS, ID	Table 24
RxData1_0	A3	O, TS	Table 24
RxData1_1	B4	O, TS, ID	Table 24
RxData2_0	B6	O, TS	Table 24
RxData2_1	C7	O, TS, ID	Table 24
RxData3_0	D9	O, TS	Table 24
RxData3_1	B9	O, TS, ID	Table 24
RxData4_0	A13	O, TS	Table 24
RxData4_1	C12	O, TS,ID	Table 24
RxData5_0	B14	O, TS	Table 24
RxData5_1	B15	O, TS, ID	Table 24
RxData6_0	C15	O, TS	Table 24
RxData6_1	B17	O, TS, ID	Table 24
RxData7_0	E16	O, TS	Table 24
RxData7_1	F14	O, TS, ID	Table 24
RxER0 (MDIX)	D2	O, TS, SL, ID, I, ST	Table 24 Table 32
RxER1 (PAUSE)	D5	O, TS, SL, ID, I, ST	Table 24 Table 32
RxER2 (PREASEL)	D7	O, TS, SL, ID, I, ST	Table 24 Table 32
RxER3	C8	O, TS, SL, ID	Table 24

Signal	Ball	Type[1]	Reference for Full Description
RxER4 (FIFOSEL0)	A12	O, TS, SL, ID, I, ST	Table 24 Table 32
RxER5 (FIFOSEL1)	A15	O, TS, SL, ID, I, ST	Table 24 Table 32
RxER6 LINKHOLD	A17	O, TS, SL, I, ID, ST	Table 24 Table 32
RxER7	D17	O, TS, SL, ID	Table 24
SD_2P5V	P1	I, ST, ID	Table 29
SD0	P2	I	Table 29
SD1	N4	I	Table 29
SD2	P3	I	Table 29
SD3	N5	I	Table 29
SD4	P15	I	Table 29
SD5	P16	I	Table 29
SD6	P17	I	Table 29
SD7	N17	I	Table 29
SECTION	L15	I, ST, ID	Table 32
SGND	K14	–	Table 34
TCK	M16	I, ST, ID	Table 31
TDI	N14	I, ST, IP	Table 31
TDO	N15	O, TS	Table 31
TMS	N16	I, ST, IP	Table 31
TPFIN0	T1	AO/AI	Table 30
TPFIN1	T4	AO/AI	Table 30
TPFIN2	T5	AO/AI	Table 30
TPFIN3	R8	AO/AI	Table 30
TPFIN4	U9	AO/AI	Table 30
TPFIN5	T12	AO/AI	Table 30
TPFIN6	T13	AO/AI	Table 30
TPFIN7	T16	AO/AI	Table 30
TPFIP0	R2	AO/AI	Table 30
TPFIP1	U3	AO/AI	Table 30
TPFIP2	R6	AO/AI	Table 30
TPFIP3	T8	AO/AI	Table 30
TPFIP4	T9	AO/AI	Table 30
TPFIP5	U13	AO/AI	Table 30
TPFIP6	R12	AO/AI	Table 30

Signal	Ball	Type[1]	Reference for Full Description
TPFIP7	R16	AO/AI	Table 30
TPFON0	U1	AO/AI	Table 30
TPFON1	R4	AO/AI	Table 30
TPFON2	U5	AO/AI	Table 30
TPFON3	T7	AO/AI	Table 30
TPFON4	R10	AO/AI	Table 30
TPFON5	U11	AO/AI	Table 30
TPFON6	U15	AO/AI	Table 30
TPFON7	T15	AO/AI	Table 30
TPFOP0	T2	AO/AI	Table 30
TPFOP1	T3	AO/AI	Table 30
TPFOP2	T6	AO/AI	Table 30
TPFOP3	U7	AO/AI	Table 30
TPFOP4	T10	AO/AI	Table 30
TPFOP5	T11	AO/AI	Table 30
TPFOP6	T14	AO/AI	Table 30
TPFOP7	R14	AO/AI	Table 30
TRST_L	M17	I, ST, IP	Table 31
TxData0_0	E2	I, ID	Table 24
TxData0_1	F4	I, ID	Table 24
TxData1_0	C3	I, ID	Table 24
TxData1_1	D4	I, ID	Table 24
TxData2_0	B5	I, ID	Table 24
TxData2_1	A4	I, ID	Table 24
TxData3_0	D8	I, ID	Table 24
TxData3_1	A6	I, ID	Table 24
TxData4_0	A11	I, ID	Table 24
TxData4_1	C10	I, ID	Table 24
TxData5_0	B13	I, ID	Table 24
TxData5_1	D11	I, ID	Table 24
TxData6_0	D13	I, ID	Table 24
TxData6_1	A16	I, ID	Table 24
TxData7_0	E14	I, ID	Table 24
TxData7_1	C16	I, ID	Table 24
TxEN0	E3	I, ID	Table 24
TxEN1	B2	I, ID	Table 24
TxEN2	C6	I, ID	Table 24

Signal	Ball	Type[1]	Reference for Full Description
TxEN3	A7	I, ID	Table 24
TxEN4	B11	I, ID	Table 24
TxEN5	A14	I, ID	Table 24
TxEN6	C14	I, ID	Table 24
TxEN7	D16	I, ID	Table 24
TxSLEW_0	N3	I, ST, ID	Table 32
TxSLEW_1	M4	I, ST, ID	Table 32
VCCD	F5	–	Table 34
VCCD	G13	–	Table 34
VCCD	J5	–	Table 34
VCCD	J14	–	Table 34
VCCIO	A2	–	Table 34
VCCIO	A8	–	Table 34
VCCIO	C1	–	Table 34
VCCIO	C11	–	Table 34
VCCIO	D14	–	Table 34
VCCPECL	L5	–	Table 34
VCCPECL	L13	–	Table 34
VCCR	N13	–	Table 34
VCCR	P4	–	Table 34
VCCR	P7	–	Table 34
VCCR	P8	–	Table 34
VCCR	P9	–	Table 34
VCCR	P10	–	Table 34
VCCR	P11	–	Table 34
VCCR	P12	–	Table 34
VCCT	N6	–	Table 34
VCCT	N7	–	Table 34
VCCT	N9	–	Table 34
VCCT	N11	–	Table 34
VCCT	N12	–	Table 34

Table 19 RMII BGA23 Ball List in Alphanumeric Order by Ball Location

Ball	Signal	Type[1]	Reference for Full Description
A1	GNDD	–	Table 34
A2	VCCIO	–	Table 34
A3	RxData1_0	O, TS	Table 24
A4	TxData2_1	I, ID	Table 24
A5	CRS_DV2	O, TS, SL, ID	Table 24
A6	TxData3_1	I, ID	Table 24
A7	TxEN3	I, ID	Table 24
A8	VCCIO	–	Table 34
A9	GNDD	–	Table 34
A10	MDIO1	I/O, TS, SL, IP	Table 28
A11	TxData4_0	I, ID	Table 24
A12	RxER4 (FIFOSEL0)	O, TS, SL, ID, I, ST	Table 24 Table 32
A13	RxData4_0	O, TS	Table 24
A14	TxEN5	I, ID	Table 24
A15	RxER5 (FIFOSEL1)	O, TS, SL, ID, I, ST	Table 24 Table 32
A16	TxData6_1	I, ID	Table 24
A17	RxER6LINK HOLD	O, TS, SL, I, ID, ST	Table 24 Table 32
B1	RxData0_1	O, TS, ID	Table 24
B2	TxEN1	I, ID	Table 24
B3	GNDD	–	Table 34
B4	RxData1_1	O, TS, ID	Table 24
B5	TxData2_0	I, ID	Table 24
B6	RxData2_0	O, TS	Table 24
B7	GNDD	–	Table 34
B8	CRS_DV3	O, TS, SL, ID	Table 24
B9	RxData3_1	O, TS, ID	Table 24
B10	MDC1	I, ST, ID	Table 28
B11	TxEN4	I, ID	Table 24
B12	CRS_DV4	O, TS, SL, ID	Table 24
B13	TxData5_0	I, ID	Table 24
B14	RxData5_0	O, TS	Table 24
B15	RxData5_1	O, TS, ID	Table 24
B16	CRS_DV6	O, TS, SL, ID	Table 24
B17	RxData6_1	O, TS, ID	Table 24
C1	VCCIO	–	Table 34
C2	RxData0_0	O, TS	Table 24
C3	TxData1_0	I, ID	Table 24
C4	CRS_DV1	O, TS, SL, ID	Table 24
C5	GNDD	–	Table 34
C6	TxEN2	I, ID	Table 24
C7	RxData2_1	O, TS, ID	Table 24
C8	RxER3	O, TS, SL, ID	Table 24
C9	MDINT1_L	OD, TS, SL, IP	Table 28
C10	TxData4_1	I, ID	Table 24
C11	VCCIO	–	Table 34
C12	RxData4_1	O, TS,ID	Table 24
C13	GNDD	–	Table 34
C14	TxEN6	I, ID	Table 24
C15	RxData6_0	O, TS	Table 24
C16	TxData7_1	I, ID	Table 24
C17	GNDD	–	Table 34
D1	GNDD	–	Table 34
D2	RxER0 (MDIX)	O, TS, SL, I, ID, ST	Table 24 Table 32
D3	GNDD	–	Table 34
D4	TxData1_1	I, ID	Table 24
D5	RxER1 (PAUSE)	O, TS, SL, ID, I, ST	Table 24 Table 32
D6	GNDD	–	Table 34
D7	RxER2 (PREASEL)	O, TS, SL, I, ID, ST	Table 24 Table 32
D8	TxData3_0	I, ID	Table 24
D9	RxData3_0	O, TS	Table 24
D10	GNDD	–	Table 34
D11	TxData5_1	I, ID	Table 24

Ball	Signal	Type[1]	Reference for Full Description
D12	CRS_DV5	O, TS, SL, ID	Table 24
D13	TxData6_0	I, ID	Table 24
D14	VCCIO	–	Table 34
D15	GNDD	–	Table 34
D16	TxEN7	I, ID	Table 24
D17	RxER7	O, TS, SL, ID	Table 24
E1	MDC0	I, ST, ID	Table 28
E2	TxData0_0	I, ID	Table 24
E3	TxEN0	I, ID	Table 24
E4	CRS_DV0	O, TS, SL, ID	Table 24
E5	GNDD	–	Table 34
E6	REFCLK0	I	Table 24
E7	GNDD	–	Table 34
E8	No Ball	–	–
E9	GNDD	–	Table 34
E10	No Ball		
E11	GNDD	–	Table 34
E12	REFCLK1	I	Table 24
E13	GNDD	–	Table 34
E14	TxData7_0	I, ID	Table 24
E15	CRS_DV7	O, TS, SL, ID‘	Table 24
E16	RxData7_0	O, TS	Table 24
E17	GNDD	–	Table 34
F1	MDINT0_L	OD, TS, SL, IP	Table 28
F2	LED3_1_L	OD, TS, SL, IP	Table 33
F3	MDIO0	I/O, TS, SL, IP	Table 28
F4	TxData0_1	I, ID	Table 24
F5	VCCD	–	Table 34
F6	No ball	–	–
F7	No ball	–	–
F8	No ball	–	–
F9	No Ball	–	–
F10	No Ball	–	–
F11	No Ball	–	–

Ball	Signal	Type[1]	Reference for Full Description
F12	No Ball	–	–
F13	GNDD	–	Table 34
F14	RxData7_1	O, TS, ID	Table 24
F15	NC	–	Table 35
F16	LED7_3_L	OD, TS, SL, IP	Table 33
F17	LED7_2_L	OD, TS, SL, IP	Table 33
G1	LED2_3_L	OD, TS, SL, IP	Table 33
G2	NC	–	Table 35
G3	LED3_2_L	OD, TS, SL, IP	Table 33
G4	LED3_3_L	OD, TS, SO, IP	Table 33
G5	NC	–	Table 35
G6	No Ball	–	–
G7	No Ball	–	–
G8	No Ball	–	–
G9	No Ball	–	–
G10	No Ball	–	–
G11	No Ball	–	–
G12	No Ball	–	–
G13	VCCD	–	Table 34
G14	NC	–	Table 35
G15	LED7_1_L	OD, TS, SL, IP	Table 33
G16	NC	–	Table 35
G17	LED6_3_L	OD, TS, SL, IP	Table 33
H1	LED1_3_L	OD, TS, SL, IP	Table 33
H2	LED2_1_L	OD, TS, SL, IP	Table 33
H3	LED2_2_L	OD, TS, SL, IP	Table 33
H4	NC	–	Table 35
H5	No Ball	–	–
H6	No Ball	–	–
H7	No Ball	–	–
H8	GNDD	–	Table 34
H9	GNDD	–	Table 34

Ball	Signal	Type[1]	Reference for Full Description
H10	GNDD	–	Table 34
H11	No Ball	–	–
H12	No Ball	–	–
H13	No Ball	–	–
H14	NC	–	Table 35
H15	LED6_1_L	OD, TS, SL, IP	Table 33
H16	LED6_2_L	OD, TS, SL, IP	Table 33
H17	LED5_3_L	OD, TS, SL, IP	Table 33
J1	LED0_3_L	OD, TS, SL, IP	Table 33
J2	NC	–	Table 35
J3	LED1_2_L	OD, TS, SL, IP	Table 33
J4	LED1_1_L	OD, TS, SL, IP	Table 33
J5	VCCD	–	Table 34
J6	No Ball	–	–
J7	No Ball	–	–
J8	GNDD	–	Table 34
J9	GNDD	–	Table 34
J10	GNDD	–	Table 34
J11	No Ball	–	–
J12	No Ball	–	–
J13	NC	–	Table 35
J14	VCCD	–	Table 34
J15	LED5_1_L	OD, TS, SL, IP	Table 33
J16	LED5_2_L	OD, TS, SL, IP	Table 33
J17	LED4_3_L	OD, TS, SL, IP	Table 33
K1	AMDIX_EN	I, ST, IP	Table 32
K2	LED0_2_L	OD, TS, SL, IP	Table 33
K3	LED0_1_L	OD, TS, SL, IP	Table 33
K4	NC	–	Table 35
K5	No Ball	–	–
K6	No Ball	–	–

Ball	Signal	Type[1]	Reference for Full Description
K7	No Ball	–	–
K8	GNDD	–	Table 34
K9	GNDD	–	Table 34
K10	GNDD	–	Table 34
K11	No Ball	–	–
K12	No Ball	–	–
K13	No Ball	–	–
K14	SGND	–	Table 34
K15	NC	–	Table 35
K16	LED4_1_L	OD, TS, SL, IP	Table 33
K17	LED4_2_L	OD, TS, SL, IP	Table 33
L1	MDDIS	I, ST, ID	Table 28
L2	CFG_3	I, ST, ID	Table 32
L3	CFG_2	I, ST, ID	Table 32
L4	ADD_4	I, ST, ID	Table 32
L5	VCCPECL	–	Table 34
L6	No Ball	–	–
L7	No Ball	–	–
L8	No Ball	–	–
L9	No Ball	–	–
L10	No Ball	–	–
L11	No Ball	–	–
L11	No Ball	–	–
L13	VCCPECL	–	Table 34
L14	PWRDWN	I, ST, ID	Table 32
L15	SECTION	I, ST, ID	Table 32
L16	ModeSel0	I, ST, ID	Table 32
L17	ModeSel1	I, ST, ID	Table 32
M1	CFG_1	I, ST, ID	Table 32
M2	ADD_3	I, ST, ID	Table 32
M3	ADD_2	I, ST, ID	Table 32
M4	TxSLEW_1	I, ST, ID	Table 32
M5	GNDPECL	–	Table 34
M6	No Ball	–	–
M7	No Ball	–	–
M8	No Ball	–	–
M9	No Ball	–	–

Ball	Signal	Type[1]	Reference for Full Description
M10	No Ball	–	–
M11	No Ball	–	–
M12	No Ball	–	–
M13	GNDPECL	–	Table 34
M14	G_FX/TP_L	I, ST, ID	Table 32
M15	RESET_L	I, ST, IP	Table 32
M16	TCK	I, ST, ID	Table 31
M17	TRST_L	I, ST, IP	Table 31
N1	ADD_1	I, ST, ID	Table 32
N2	ADD_0	I, ST, ID	Table 32
N3	TxSLEW_0	I, ST, ID	Table 32
N4	SD1	I	Table 29
N5	SD3	I	Table 29
N6	VCCT	–	Table 34
N7	VCCT	–	Table 34
N8	No Ball	–	–
N9	VCCT	–	Table 34
N10	No Ball	–	–
N11	VCCT	–	Table 34
N12	VCCT	–	Table 34
N13	VCCR	–	Table 34
N14	TDI	I, ST, IP	Table 31
N15	TDO	O, TS	Table 31
N16	TMS	I, ST, IP	Table 31
N17	SD7	I	Table 29
P1	SD_2P5V	I, ST, ID	Table 29
P2	SD0	I	Table 29
P3	SD2	I	Table 29
P4	VCCR	–	Table 34
P5	GNDR	–	Table 34
P6	GNDR	–	Table 34
P7	VCCR	–	Table 34
P8	VCCR	–	Table 34
P9	VCCR	–	Table 34
P10	VCCR	–	Table 34
P11	VCCR	–	Table 34
P12	VCCR	–	Table 34
P13	GNDR	–	Table 34

Ball	Signal	Type[1]	Reference for Full Description
P14	GNDT	–	Table 34
P15	SD4	I	Table 29
P16	SD5	I	Table 29
P17	SD6	I	Table 29
R1	GNDT	–	Table 34
R2	TPFIP0	AO/AI	Table 30
R3	GNDT	–	Table 34
R4	TPFON1	AO/AI	Table 30
R5	GNDT	–	Table 34
R6	TPFIP2	AO/AI	Table 30
R7	GNDR	–	Table 34
R8	TPFIN3	AO/AI	Table 30
R9	GNDR	–	Table 34
R10	TPFON4	AO/AI	Table 30
R11	GNDR	–	Table 34
R12	TPFIP6	AO/AI	Table 30
R13	GNDR	–	Table 34
R14	TPFOP7	AO/AI	Table 30
R15	GNDT	–	Table 34
R16	TPFIP7	AO/AI	Table 30
R17	GNDT	–	Table 34
T1	TPFIN0	AO/AI	Table 30
T2	TPFOP0	AO/AI	Table 30
T3	TPFOP1	AO/AI	Table 30
T4	TPFIN1	AO/AI	Table 30
T5	TPFIN2	AO/AI	Table 30
T6	TPFOP2	AO/AI	Table 30
T7	TPFON3	AO/AI	Table 30
T8	TPFIP3	AO/AI	Table 30
T9	TPFIP4	AO/AI	Table 30
T10	TPFOP4	AO/AI	Table 30
T11	TPFOP5	AO/AI	Table 30
T12	TPFIN5	AO/AI	Table 30
T13	TPFIN6	AO/AI	Table 30
T14	TPFOP6	AO/AI	Table 30
T15	TPFON7	AO/AI	Table 30
T16	TPFIN7	AO/AI	Table 30
T17	GNDT	–	Table 34

Ball	Signal	Type[1]	Reference for Full Description
U1	TPFON0	AO/AI	Table 30
U2	GNDT	–	Table 34
U3	TPFIP1	AO/AI	Table 30
U4	GNDT	–	Table 34
U5	TPFON2	AO/AI	Table 30
U6	GNDT	–	Table 34
U7	TPFOP3	AO/AI	Table 30
U8	GNDR	–	Table 34
U9	TPFIN4	AO/AI	Table 30
U10	GNDT	–	Table 34
U11	TPFON5	AO/AI	Table 30
U12	GNDT	–	Table 34
U13	TPFIP5	AO/AI	Table 30
U14	GNDT	–	Table 34
U15	TPFON6	AO/AI	Table 30
U16	GNDT	–	Table 34
U17	GNDT	–	Table 34

3.3.2 SMII BGA23 Ball List

The following tables provide the SMII ball locations and signal names arranged in alphanumeric order as follows:

- Table 20, *SMII BGA23 Ball List in Alphanumeric Order by Signal Name*
- Table 21, *SMII BGA23 Ball List in Alphanumeric Order by Ball Location*, on page 66

Table 20 SMII BGA23 Ball List in Alphanumeric Order by Signal Name

Signal	Ball	Type[1]	Reference for Full Description
ADD_0	N2	I, ST, ID	Table 32
ADD_1	N1	I, ST, ID	Table 32
ADD_2	M3	I, ST, ID	Table 32
ADD_3	M2	I, ST, ID	Table 32
ADD_4	L4	I, ST, ID	Table 32
AMDIX_EN	K1	I, ST, IP	Table 32
CFG_1	M1	I, ST, ID	Table 32
CFG_2	L3	I, ST, ID	Table 32
CFG_3	L2	I, ST, ID	Table 32
FIFOSEL0	A12	O, TS, SL, ID, I, ST	Table 32
FIFOSEL1	A15	O, TS, SL, ID, I, ST	Table 32
G_FX/TP_L	M14	I, ST, ID	Table 32
GNDD	A1	–	Table 34
GNDD	A9	–	Table 34
GNDD	B3	–	Table 34
GNDD	B7	–	Table 34
GNDD	C5	–	Table 34
GNDD	C13	–	Table 34
GNDD	C17	–	Table 34
GNDD	D1	–	Table 34

Signal	Ball	Type[1]	Reference for Full Description
GNDD	D3	–	Table 34
GNDD	D6	–	Table 34
GNDD	D10	–	Table 34
GNDD	D15	–	Table 34
GNDD	E5	–	Table 34
GNDD	E7	–	Table 34
GNDD	E9	–	Table 34
GNDD	E11	–	Table 34
GNDD	E13	–	Table 34
GNDD	E17	–	Table 34
GNDD	F13	–	Table 34
GNDD	H8	–	Table 34
GNDD	H9	–	Table 34
GNDD	H10	–	Table 34
GNDD	J8	–	Table 34
GNDD	J9	–	Table 34
GNDD	J10	–	Table 34
GNDD	K8	–	Table 34
GNDD	K9	–	Table 34
GNDD	K10	–	Table 34
GNDPECL	M5	–	Table 34
GNDPECL	M13	–	Table 34
GNDR	P5	–	Table 34
GNDR	P6	–	Table 34
GNDR	P13	–	Table 34
GNDR	R7	–	Table 34
GNDR	R9	–	Table 34
GNDR	R11	–	Table 34
GNDR	R13	–	Table 34
GNDR	U8	–	Table 34
GNDT	P14	–	Table 34
GNDT	R1	–	Table 34
GNDT	R3	–	Table 34
GNDT	R5	–	Table 34
GNDT	R15	–	Table 34
GNDT	R17	–	Table 34
GNDT	T17	–	Table 34

Signal	Ball	Type[1]	Reference for Full Description
GNDT	U2	–	Table 34
GNDT	U4	–	Table 34
GNDT	U6	–	Table 34
GNDT	U10	–	Table 34
GNDT	U12	–	Table 34
GNDT	U14	–	Table 34
GNDT	U16	–	Table 34
GNDT	U17	–	Table 34
LED0_1_L	K3	OD, TS, SL, IP	Table 33
LED0_2_L	K2	OD, TS, SL, IP	Table 33
LED0_3_L	J1	OD, TS, SL, IP	Table 33
LED1_1_L	J4	OD, TS, SL, IP	Table 33
LED1_2_L	J3	OD, TS, SL, IP	Table 33
LED1_3_L	H1	OD, TS, SL, IP	Table 33
LED2_1_L	H2	OD, TS, SL, IP	Table 33
LED2_2_L	H3	OD, TS, SL, IP	Table 33
LED2_3_L	G1	OD, TS, SL, IP	Table 33
LED3_1_L	F2	OD, TS, SL, IP	Table 33
LED3_2_L	G3	OD, TS, SL, IP	Table 33
LED3_3_L	G4	OD, TS, SO, IP	Table 33
LED4_1_L	K16	OD, TS, SL, IP	Table 33
LED4_2_L	K17	OD, TS, SL, IP	Table 33
LED4_3_L	J17	OD, TS, SL, IP	Table 33
LED5_1_L	J15	OD, TS, SL, IP	Table 33
LED5_2_L	J16	OD, TS, SL, IP	Table 33
LED5_3_L	H17	OD, TS, SL, IP	Table 33
LED6_1_L	H15	OD, TS, SL, IP	Table 33

Signal	Ball	Type[1]	Reference for Full Description
LED6_2_L	H16	OD, TS, SL, IP	Table 33
LED6_3_L	G17	OD, TS, SL, IP	Table 33
LED7_1_L	G15	OD, TS, SL, IP	Table 33
LED7_2_L	F17	OD, TS, SL, IP	Table 33
LED7_3_L	F16	OD, TS, SL, IP	Table 33
MDC0	E1	I, ST, ID	Table 28
MDC1	B10	I, ST, ID	Table 28
MDDIS	L1	I, ST, ID	Table 28
MDINT0_L	F1	OD, TS, SL, IP	Table 28
MDINT1_L	C9	OD, TS, SL, IP	Table 28
MDIO0	F3	I/O, TS, SL, IP	Table 28
MDIO1	A10	I/O, TS, SL, IP	Table 28
MDIX	D2	I, ID, ST	Table 32
ModeSel0	L16	I, ST, ID	Table 32
ModeSel1	L17	I, ST, ID	Table 32
NC	A4	–	Table 35
NC	A5	–	Table 35
NC	A7	–	Table 35
NC	A14	–	Table 35
NC	A16	–	Table 35
NC	B1	–	Table 35
NC	B2	–	Table 35
NC	B4	–	Table 35
NC	B8	–	Table 35
NC	B9	–	Table 35
NC	B11	–	Table 35
NC	B12	–	Table 35
NC	B15	–	Table 35
NC	B16	–	Table 35
NC	B17	–	Table 35
NC	C4	–	Table 35
NC	C6	–	Table 35
NC	C7	–	Table 35

Signal	Ball	Type[1]	Reference for Full Description
NC	C8	–	Table 35
NC	C10	–	Table 35
NC	C12	–	Table 35
NC	C14	–	Table 35
NC	D4	–	Table 35
NC	D11	–	Table 35
NC	D12	–	Table 35
NC	D16	–	Table 35
NC	D17	–	Table 35
NC	E3	–	Table 35
NC	E4	–	Table 35
NC	E15	–	Table 35
NC	F4	–	Table 35
NC	F14	–	Table 35
NC	F15	–	Table 35
NC	G2	–	Table 35
NC	G5	–	Table 35
NC	G14	–	Table 35
NC	G16	–	Table 35
NC	H4	–	Table 35
NC	H14	–	Table 35
NC	J2	–	Table 35
NC	J13	–	Table 35
NC	K4	–	Table 35
NC	K15	–	Table 35
NC/ LINKHOLD	A17	I, ID, ST	Table 35 Table 32
No ball	F6	–	–
No ball	F7	–	–
No ball	F8	–	–
No Ball	E8	–	–
No Ball	E10		–
No Ball	F9	–	–
No Ball	F10	–	–
No Ball	F11	–	–
No Ball	F12	–	–
No Ball	G6	–	–
No Ball	G7	–	–

Signal	Ball	Type[1]	Reference for Full Description
No Ball	G8	–	–
No Ball	G9	–	–
No Ball	G10	–	–
No Ball	G11	–	–
No Ball	G12	–	–
No Ball	H5	–	–
No Ball	H6	–	–
No Ball	H7	–	–
No Ball	H11	–	–
No Ball	H12	–	–
No Ball	H13	–	–
No Ball	J6	–	–
No Ball	J7	–	–
No Ball	J11	–	–
No Ball	J12	–	–
No Ball	K5	–	–
No Ball	K6	–	–
No Ball	K7	–	–
No Ball	K11	–	–
No Ball	K12	–	–
No Ball	K13	–	–
No Ball	L6	–	–
No Ball	L7	–	–
No Ball	L8	–	–
No Ball	L9	–	–
No Ball	L10	–	–
No Ball	L11	–	–
No Ball	L11	–	–
No Ball	M6	–	–
No Ball	M7	–	–
No Ball	M8	–	–
No Ball	M9	–	–
No Ball	M10	–	–
No Ball	M11	–	–
No Ball	M12	–	–
No Ball	N8	–	–
No Ball	N10	–	–
PAUSE	D5	O, TS, SL, ID, I, ST	Table 32
PREASEL	D7	I, ID, ST	Table 32
PWRDWN	L14	I, ID, ST	Table 32
REFCLK0	E6	I	Table 25
REFCLK1	E12	I	Table 25
RESET_L	M15	I, ST, IP	Table 32
RxData0	C2	O, TS, ID	Table 26
RxData1	A3	O, TS, ID	Table 26
RxData2	B6	O, TS, ID	Table 26
RxData3	D9	O, TS, ID	Table 26
RxData4	A13	O, TS, ID	Table 26
RxData5	B14	O, TS, ID	Table 26
RxData6	C15	O, TS, ID	Table 26
RxData7	E16	O, TS, ID	Table 26
SD_2P5V	P1	I, ST, ID	Table 29
SD0	P2	I	Table 29
SD1	N4	I	Table 29
SD2	P3	I	Table 29
SD3	N5	I	Table 29
SD4	P15	I	Table 29
SD5	P16	I	Table 29
SD6	P17	I	Table 29
SD7	N17	I	Table 29
SECTION	L15	I, ST, ID	Table 32
SGND	K14	–	Table 34
SYNC0	A6	I, ID	Table 26
SYNC1	C16	I, ID	Table 26
TCK	M16	I, ST, ID	Table 31
TDI	N14	I, ST, IP	Table 31
TDO	N15	O, TS	Table 31
TMS	N16	I, ST, IP	Table 31
TPFIN0	T1	AO/AI	Table 30
TPFIN1	T4	AO/AI	Table 30
TPFIN2	T5	AO/AI	Table 30
TPFIN3	R8	AO/AI	Table 30

Signal	Ball	Type[1]	Reference for Full Description
TPFIN4	U9	AO/AI	Table 30
TPFIN5	T12	AO/AI	Table 30
TPFIN6	T13	AO/AI	Table 30
TPFIN7	T16	AO/AI	Table 30
TPFIP0	R2	AO/AI	Table 30
TPFIP1	U3	AO/AI	Table 30
TPFIP2	R6	AO/AI	Table 30
TPFIP3	T8	AO/AI	Table 30
TPFIP4	T9	AO/AI	Table 30
TPFIP5	U13	AO/AI	Table 30
TPFIP6	R12	AO/AI	Table 30
TPFIP7	R16	AO/AI	Table 30
TPFON0	U1	AO/AI	Table 30
TPFON1	R4	AO/AI	Table 30
TPFON2	U5	AO/AI	Table 30
TPFON3	T7	AO/AI	Table 30
TPFON4	R10	AO/AI	Table 30
TPFON5	U11	AO/AI	Table 30
TPFON6	U15	AO/AI	Table 30
TPFON7	T15	AO/AI	Table 30
TPFOP0	T2	AO/AI	Table 30
TPFOP1	T3	AO/AI	Table 30
TPFOP2	T6	AO/AI	Table 30
TPFOP3	U7	AO/AI	Table 30
TPFOP4	T10	AO/AI	Table 30
TPFOP5	T11	AO/AI	Table 30
TPFOP6	T14	AO/AI	Table 30
TPFOP7	R14	AO/AI	Table 30
TRST_L	M17	I, ST, IP	Table 31
TxData0	E2	I, ID	Table 25
TxData1	C3	I, ID	Table 25
TxData2	B5	I, ID	Table 25
TxData3	D8	I, ID	Table 25
TxData4	A11	I, ID	Table 25
TxData5	B13	I, ID	Table 25
TxData6	D13	I, ID	Table 25
TxData7	E14	I, ID	Table 25

Signal	Ball	Type[1]	Reference for Full Description
TxSLEW_0	N3	I, ST, ID	Table 32
TxSLEW_1	M4	I, ST, ID	Table 32
VCCD	F5	–	Table 34
VCCD	G13	–	Table 34
VCCD	J5	–	Table 34
VCCD	J14	–	Table 34
VCCIO	A2	–	Table 34
VCCIO	A8	–	Table 34
VCCIO	C1	–	Table 34
VCCIO	C11	–	Table 34
VCCIO	D14	–	Table 34
VCCPECL	L5	–	Table 34
VCCPECL	L13	–	Table 34
VCCR	N13	–	Table 34
VCCR	P4	–	Table 34
VCCR	P7	–	Table 34
VCCR	P8	–	Table 34
VCCR	P9	–	Table 34
VCCR	P10	–	Table 34
VCCR	P11	–	Table 34
VCCR	P12	–	Table 34
VCCT	N6	–	Table 34
VCCT	N7	–	Table 34
VCCT	N9	–	Table 34
VCCT	N11	–	Table 34
VCCT	N12	–	Table 34

Table 21 SMII BGA23 Ball List in Alphanumeric Order by Ball Location

Ball	Signal	Type[1]	Reference for Full Description
A1	GNDD	–	Table 34
A2	VCCIO	–	Table 34
A3	RxData1	O, TS, ID	Table 26
A4	NC	–	Table 35
A5	NC	–	Table 35
A6	SYNC0	I, ID	Table 26
A7	NC	–	Table 35
A8	VCCIO	–	Table 34
A9	GNDD	–	Table 34
A10	MDIO1	I/O, TS, SL, IP	Table 28
A11	TxData4	I, ID	Table 25
A12	FIFOSEL0	O, TS, SL, ID, I, ST	Table 32
A13	RxData4	O, TS, ID	Table 26
A14	NC	–	Table 35
A15	FIFOSEL1	O, TS, SL, ID, I, ST	Table 32
A16	NC	–	Table 35
A17	NC/ LINKHOLD	I, ID, ST	Table 35 Table 32
B1	NC	–	Table 35
B2	NC	–	Table 35
B3	GNDD	–	Table 34
B4	NC	–	Table 35
B5	TxData2	I, ID	Table 25
B6	RxData2	O, TS, ID	Table 26
B7	GNDD	–	Table 34
B8	NC	–	Table 35
B9	NC	–	Table 35
B10	MDC1	I, ST, ID	Table 28
B11	NC	–	Table 35
B12	NC	–	Table 35
B13	TxData5	I, ID	Table 25
B14	RxData5	O, TS, ID	Table 26
B15	NC	–	Table 35
B16	NC	–	Table 35
B17	NC	–	Table 35

Ball	Signal	Type[1]	Reference for Full Description
C1	VCCIO	–	Table 34
C2	RxData0	O, TS, ID	Table 26
C3	TxData1	I, ID	Table 25
C4	NC	–	Table 35
C5	GNDD	–	Table 34
C6	NC	–	Table 35
C7	NC	–	Table 35
C8	NC	–	Table 35
C9	MDINT1_L	OD, TS, SL, IP	Table 28
C10	NC	–	Table 35
C11	VCCIO	–	Table 34
C12	NC	–	Table 35
C13	GNDD	–	Table 34
C14	NC	–	Table 35
C15	RxData6	O, TS, ID	Table 26
C16	SYNC1	I, ID	Table 26
C17	GNDD	–	Table 34
D1	GNDD	–	Table 34
D2	MDIX	I, ID, ST	Table 32
D3	GNDD	–	Table 34
D4	NC	–	Table 35
D5	PAUSE	O, TS, SL, ID, I, ST	Table 32
D6	GNDD	–	Table 34
D7	PREASEL	I, ID, ST	Table 32
D8	TxData3	I, ID	Table 25
D9	RxData3	O, TS, ID	Table 26
D10	GNDD	–	Table 34
D11	NC	–	Table 35
D12	NC	–	Table 35
D13	TxData6	I, ID	Table 25
D14	VCCIO	–	Table 34
D15	GNDD	–	Table 34
D16	NC	–	Table 35
D17	NC	–	Table 35
E1	MDC0	I, ST, ID	Table 28
E2	TxData0	I, ID	Table 25

Ball	Signal	Type[1]	Reference for Full Description
E3	NC	–	Table 35
E4	NC	–	Table 35
E5	GNDD	–	Table 34
E6	REFCLK0	I	Table 25
E7	GNDD	–	Table 34
E8	No Ball	–	–
E9	GNDD	–	Table 34
E10	No Ball		–
E11	GNDD	–	Table 34
E12	REFCLK1	I	Table 25
E13	GNDD	–	Table 34
E14	TxData7	I, ID	Table 25
E15	NC	–	Table 35
E16	RxData7	O, TS, ID	Table 26
E17	GNDD	–	Table 34
F1	MDINT0_L	OD, TS, SL, IP	Table 28
F2	LED3_1_L	OD, TS, SL, IP	Table 33
F3	MDIO0	I/O, TS, SL, IP	Table 28
F4	NC	–	Table 35
F5	VCCD	–	Table 34
F6	No ball	–	–
F7	No ball	–	–
F8	No ball	–	–
F9	No Ball	–	–
F10	No Ball	–	–
F11	No Ball	–	–
F12	No Ball	–	–
F13	GNDD	–	Table 34
F14	NC	–	Table 35
F15	NC	–	Table 35
F16	LED7_3_L	OD, TS, SL, IP	Table 33
F17	LED7_2_L	OD, TS, SL, IP	Table 33
G1	LED2_3_L	OD, TS, SL, IP	Table 33
G2	NC	–	Table 35

Ball	Signal	Type[1]	Reference for Full Description
G3	LED3_2_L	OD, TS, SL, IP	Table 33
G4	LED3_3_L	OD, TS, SO, IP	Table 33
G5	NC	–	Table 35
G6	No Ball	–	–
G7	No Ball	–	–
G8	No Ball	–	–
G9	No Ball	–	–
G10	No Ball	–	–
G11	No Ball	–	–
G12	No Ball	–	–
G13	VCCD	–	Table 34
G14	NC	–	Table 35
G15	LED7_1_L	OD, TS, SL, IP	Table 33
G16	NC	–	Table 35
G17	LED6_3_L	OD, TS, SL, IP	Table 33
H1	LED1_3_L	OD, TS, SL, IP	Table 33
H2	LED2_1_L	OD, TS, SL, IP	Table 33
H3	LED2_2_L	OD, TS, SL, IP	Table 33
H4	NC	–	Table 35
H5	No Ball	–	–
H6	No Ball	–	–
H7	No Ball	–	–
H8	GNDD	–	Table 34
H9	GNDD	–	Table 34
H10	GNDD	–	Table 34
H11	No Ball	–	–
H12	No Ball	–	–
H13	No Ball	–	–
H14	NC	–	Table 35
H15	LED6_1_L	OD, TS, SL, IP	Table 33
H16	LED6_2_L	OD, TS, SL, IP	Table 33
H17	LED5_3_L	OD, TS, SL, IP	Table 33

Ball	Signal	Type[1]	Reference for Full Description
J1	LED0_3_L	OD, TS, SL, IP	Table 33
J2	NC	–	Table 35
J3	LED1_2_L	OD, TS, SL, IP	Table 33
J4	LED1_1_L	OD, TS, SL, IP	Table 33
J5	VCCD	–	Table 34
J6	No Ball	–	–
J7	No Ball	–	–
J8	GNDD	–	Table 34
J9	GNDD	–	Table 34
J10	GNDD	–	Table 34
J11	No Ball	–	–
J12	No Ball	–	–
J13	NC	–	Table 35
J14	VCCD	–	Table 34
J15	LED5_1_L	OD, TS, SL, IP	Table 33
J16	LED5_2_L	OD, TS, SL, IP	Table 33
J17	LED4_3_L	OD, TS, SL, IP	Table 33
K1	AMDIX_EN	I, ST, IP	Table 32
K2	LED0_2_L	OD, TS, SL, IP	Table 33
K3	LED0_1_L	OD, TS, SL, IP	Table 33
K4	NC	–	Table 35
K5	No Ball	–	–
K6	No Ball	–	–
K7	No Ball	–	–
K8	GNDD	–	Table 34
K9	GNDD	–	Table 34
K10	GNDD	–	Table 34
K11	No Ball	–	–
K12	No Ball	–	–
K13	No Ball	–	–
K14	SGND	–	Table 34
K15	NC	–	Table 35
K16	LED4_1_L	OD, TS, SL, IP	Table 33

Ball	Signal	Type[1]	Reference for Full Description
K17	LED4_2_L	OD, TS, SL, IP	Table 33
L1	MDDIS	I, ST, ID	Table 28
L2	CFG_3	I, ST, ID	Table 32
L3	CFG_2	I, ST, ID	Table 32
L4	ADD_4	I, ST, ID	Table 32
L5	VCCPECL	–	Table 34
L6	No Ball	–	–
L7	No Ball	–	–
L8	No Ball	–	–
L9	No Ball	–	–
L10	No Ball	–	–
L11	No Ball	–	–
L11	No Ball	–	–
L13	VCCPECL	–	Table 34
L14	PWRDWN	I, ID, ST	Table 32
L15	SECTION	I, ST, ID	Table 32
L16	ModeSel0	I, ST, ID	Table 32
L17	ModeSel1	I, ST, ID	Table 32
M1	CFG_1	I, ST, ID	Table 32
M2	ADD_3	I, ST, ID	Table 32
M3	ADD_2	I, ST, ID	Table 32
M4	TxSLEW_1	I, ST, ID	Table 32
M5	GNDPECL	–	Table 34
M6	No Ball	–	–
M7	No Ball	–	–
M8	No Ball	–	–
M9	No Ball	–	–
M10	No Ball	–	–
M11	No Ball	–	–
M12	No Ball	–	–
M13	GNDPECL	–	Table 34
M14	G_FX/TP_L	I, ST, ID	Table 32
M15	RESET_L	I, ST, IP	Table 32
M16	TCK	I, ST, ID	Table 31
M17	TRST_L	I, ST, IP	Table 31
N1	ADD_1	I, ST, ID	Table 32
N2	ADD_0	I, ST, ID	Table 32

Ball	Signal	Type[1]	Reference for Full Description
N3	TxSLEW_0	I, ST, ID	Table 32
N4	SD1	I	Table 29
N5	SD3	I	Table 29
N6	VCCT	–	Table 34
N7	VCCT	–	Table 34
N8	No Ball	–	–
N9	VCCT	–	Table 34
N10	No Ball	–	–
N11	VCCT	–	Table 34
N12	VCCT	–	Table 34
N13	VCCR	–	Table 34
N14	TDI	I, ST, IP	Table 31
N15	TDO	O, TS	Table 31
N16	TMS	I, ST, IP	Table 31
N17	SD7	I	Table 29
P1	SD_2P5V	I, ST, ID	Table 29
P2	SD0	I	Table 29
P3	SD2	I	Table 29
P4	VCCR	–	Table 34
P5	GNDR	–	Table 34
P6	GNDR	–	Table 34
P7	VCCR	–	Table 34
P8	VCCR	–	Table 34
P9	VCCR	–	Table 34
P10	VCCR	–	Table 34
P11	VCCR	–	Table 34
P12	VCCR	–	Table 34
P13	GNDR	–	Table 34
P14	GNDT	–	Table 34
P15	SD4	I	Table 29
P16	SD5	I	Table 29
P17	SD6	I	Table 29
R1	GNDT	–	Table 34
R2	TPFIP0	AO/AI	Table 30
R3	GNDT	–	Table 34
R4	TPFON1	AO/AI	Table 30
R5	GNDT	–	Table 34
R6	TPFIP2	AO/AI	Table 30

Ball	Signal	Type[1]	Reference for Full Description
R7	GNDR	–	Table 34
R8	TPFIN3	AO/AI	Table 30
R9	GNDR	–	Table 34
R10	TPFON4	AO/AI	Table 30
R11	GNDR	–	Table 34
R12	TPFIP6	AO/AI	Table 30
R13	GNDR	–	Table 34
R14	TPFOP7	AO/AI	Table 30
R15	GNDT	–	Table 34
R16	TPFIP7	AO/AI	Table 30
R17	GNDT	–	Table 34
T1	TPFIN0	AO/AI	Table 30
T2	TPFOP0	AO/AI	Table 30
T3	TPFOP1	AO/AI	Table 30
T4	TPFIN1	AO/AI	Table 30
T5	TPFIN2	AO/AI	Table 30
T6	TPFOP2	AO/AI	Table 30
T7	TPFON3	AO/AI	Table 30
T8	TPFIP3	AO/AI	Table 30
T9	TPFIP4	AO/AI	Table 30
T10	TPFOP4	AO/AI	Table 30
T11	TPFOP5	AO/AI	Table 30
T12	TPFIN5	AO/AI	Table 30
T13	TPFIN6	AO/AI	Table 30
T14	TPFOP6	AO/AI	Table 30
T15	TPFON7	AO/AI	Table 30
T16	TPFIN7	AO/AI	Table 30
T17	GNDT	–	Table 34
U1	TPFON0	AO/AI	Table 30
U2	GNDT	–	Table 34
U3	TPFIP1	AO/AI	Table 30
U4	GNDT	–	Table 34
U5	TPFON2	AO/AI	Table 30
U6	GNDT	–	Table 34
U7	TPFOP3	AO/AI	Table 30
U8	GNDR	–	Table 34
U9	TPFIN4	AO/AI	Table 30
U10	GNDT	–	Table 34

Ball	Signal	Type[1]	Reference for Full Description
U11	TPFON5	AO/AI	Table 30
U12	GNDT	–	Table 34
U13	TPFIP5	AO/AI	Table 30
U14	GNDT	–	Table 34
U15	TPFON6	AO/AI	Table 30
U16	GNDT	–	Table 34
U17	GNDT	–	Table 34

3.3.3 SS-SMII BGA23 Ball List

The following tables provide the SS-SMII ball locations and signal names arranged in alphanumeric order as follows:

- Table 22, *SS-SMII BGA23 Ball List in Alphanumeric Order by Signal Name*
- Table 23, *SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location*, on page 75

Table 22 SS-SMII BGA23 Ball List in Alphanumeric Order by Signal Name

Signal	Ball	Type[1]	Reference for Full Description
ADD_0	N2	I, ST, ID	Table 32
ADD_1	N1	I, ST, ID	Table 32
ADD_2	M3	I, ST, ID	Table 32
ADD_3	M2	I, ST, ID	Table 32
ADD_4	L4	I, ST, ID	Table 32
AMDIX_EN	K1	I, ST, IP	Table 32
CFG_1	M1	I, ST, ID	Table 32
CFG_2	L3	I, ST, ID	Table 32
CFG_3	L2	I, ST, ID	Table 32
FIFOSEL0	A12	I, ID, ST	Table 32
FIFOSEL1	A15	I, ID, ST	Table 32
G_FX/TP_L	M14	I, ID, ST	Table 32
GNDD	A1	–	Table 34
GNDD	A9	–	Table 34
GNDD	B3	–	Table 34
GNDD	B7	–	Table 34
GNDD	C5	–	Table 34
GNDD	C13	–	Table 34
GNDD	C17	–	Table 34
GNDD	D1	–	Table 34
GNDD	D3	–	Table 34
GNDD	D6	–	Table 34
GNDD	D10	–	Table 34
GNDD	D15	–	Table 34
GNDD	E5	–	Table 34
GNDD	E7	–	Table 34
GNDD	E9	–	Table 34
GNDD	E11	–	Table 34
GNDD	E13	–	Table 34
GNDD	E17	–	Table 34
GNDD	F13	–	Table 34
GNDD	H8	–	Table 34
GNDD	H9	–	Table 34
GNDD	H10	–	Table 34
GNDD	J8	–	Table 34
GNDD	J9	–	Table 34
GNDD	J10	–	Table 34
GNDD	K8	–	Table 34
GNDD	K9	–	Table 34
GNDD	K10	–	Table 34

Signal	Ball	Type[1]	Reference for Full Description
GNDPECL	M5	–	Table 34
GNDPECL	M13	–	Table 34
GNDR	P5	–	Table 34
GNDR	P6	–	Table 34
GNDR	P13	–	Table 34
GNDR	R7	–	Table 34
GNDR	R9	–	Table 34
GNDR	R11	–	Table 34
GNDR	R13	–	Table 34
GNDR	U8	–	Table 34
GNDT	P14	–	Table 34
GNDT	R1	–	Table 34
GNDT	R3	–	Table 34
GNDT	R5	–	Table 34
GNDT	R15	–	Table 34
GNDT	R17	–	Table 34
GNDT	T17	–	Table 34
GNDT	U2	–	Table 34
GNDT	U4	–	Table 34
GNDT	U6	–	Table 34
GNDT	U10	–	Table 34
GNDT	U12	–	Table 34
GNDT	U14	–	Table 34
GNDT	U16	–	Table 34
GNDT	U17	–	Table 34
LED0_1_L	K3	OD, TS, SL, IP	Table 33
LED0_2_L	K2	OD, TS, SL, IP	Table 33
LED0_3_L	J1	OD, TS, SL, IP	Table 33
LED1_1_L	J4	OD, TS, SL, IP	Table 33
LED1_2_L	J3	OD, TS, SL, IP	Table 33
LED1_3_L	H1	OD, TS, SL, IP	Table 33
LED2_1_L	H2	OD, TS, SL, IP	Table 33
LED2_2_L	H3	OD, TS, SL, IP	Table 33

Signal	Ball	Type[1]	Reference for Full Description
LED2_3_L	G1	OD, TS, SL, IP	Table 33
LED3_1_L	F2	OD, TS, SL, IP	Table 33
LED3_2_L	G3	OD, TS, SL, IP	Table 33
LED3_3_L	G4	OD, TS, SL, IP	Table 33
LED4_1_L	K16	OD, TS, SL, IP	Table 33
LED4_2_L	K17	OD, TS, SL, IP	Table 33
LED4_3_L	J17	OD, TS, SL, IP	Table 33
LED5_1_L	J15	OD, TS, SL, IP	Table 33
LED5_2_L	J16	OD, TS, SL, IP	Table 33
LED5_3_L	H17	OD, TS, SL, IP	Table 33
LED6_1_L	H15	OD, TS, SL, IP	Table 33
LED6_2_L	H16	OD, TS, SL, IP	Table 33
LED6_3_L	G17	OD, TS, SL, IP	Table 33
LED7_1_L	G15	OD, TS, SL, IP	Table 33
LED7_2_L	F17	OD, TS, SL, IP	Table 33
LED7_3_L	F16	OD, TS, SL, IP	Table 33
MDC0	E1	I, ST, ID	Table 28
MDC1	B10	I, ST, ID	Table 28
MDDIS	L1	I, ST, ID	Table 28
MDINT0_L	F1	OD, TS, SL, IP	Table 28
MDINT1_L	C9	OD, TS, SL, IP	Table 28
MDIO0	F3	I/O, TS, SL, IP	Table 28
MDIO1	A10	I/O, TS, SL, IP	Table 28
MDIX	D2	I, ID, ST	Table 32
ModeSel0	L16	I, ST, ID	Table 32
ModeSel1	L17	I, ST, ID	Table 32

Signal	Ball	Type[1]	Reference for Full Description
NC	A3	–	Table 35
NC	A4	–	Table 35
NC	A5	–	Table 35
NC	A7	–	Table 35
NC	A13	–	Table 35
NC	A14	–	Table 35
NC	A16	–	Table 35
NC	B2	–	Table 35
NC	B6	–	Table 35
NC	B8	–	Table 35
NC	B14	–	Table 35
NC	B16	–	Table 35
NC	C2	–	Table 35
NC	C4	–	Table 35
NC	C6	–	Table 35
NC	C10	–	Table 35
NC	C14	–	Table 35
NC	C15	–	Table 35
NC	D4	–	Table 35
NC	D9	–	Table 35
NC	D11	–	Table 35
NC	D12	–	Table 35
NC	D16	–	Table 35
NC	E15	–	Table 35
NC	E16	–	Table 35
NC	F4	–	Table 35
NC	F15	–	Table 35
NC	G2	–	Table 35
NC	G5	–	Table 35
NC	G14	–	Table 35
NC	G16	–	Table 35
NC	H4	–	Table 35
NC	H14	–	Table 35
NC	J2	–	Table 35
NC	J13	–	Table 35
NC	K4	–	Table 35
NC	K15	–	Table 35

Signal	Ball	Type[1]	Reference for Full Description
NC/ LINKHOLD	A17	I, ID, ST	Table 35 Table 32
No ball	F6	–	–
No ball	F7	–	–
No ball	F8	–	–
No Ball	E8	–	–
No Ball	E10	–	–
No Ball	F9	–	–
No Ball	F10	–	–
No Ball	F11	–	–
No Ball	F12	–	–
No Ball	G6	–	–
No Ball	G7	–	–
No Ball	G8	–	–
No Ball	G9	–	–
No Ball	G10	–	–
No Ball	G11	–	–
No Ball	G12	–	–
No Ball	H5	–	–
No Ball	H6	–	–
No Ball	H7	–	–
No Ball	H11	–	–
No Ball	H12	–	–
No Ball	H13	–	–
No Ball	J6	–	–
No Ball	J7	–	–
No Ball	J11		–
No Ball	J12	–	–
No Ball	K5	–	–
No Ball	K6	–	–
No Ball	K7	–	–
No Ball	K11	–	–
No Ball	K12	–	–
No Ball	K13	–	–
No Ball	L6	–	–
No Ball	L7	–	–
No Ball	L8	–	–
No Ball	L9	–	–

Signal	Ball	Type[1]	Reference for Full Description
No Ball	L10	–	–
No Ball	L11	–	–
No Ball	L11	–	–
No Ball	M6	–	–
No Ball	M7	–	–
No Ball	M8	–	–
No Ball	M9	–	–
No Ball	M10	–	–
No Ball	M11	–	–
No Ball	M12	–	–
No Ball	N8	–	–
No Ball	N10	–	–
PAUSE	D5	ID, I, ST	Table 32
PREASEL	D7	I, ID, ST	Table 32
PWRDWN	L14	I, ST, ID	Table 32
REFCLK0	E6	I	Table 25
REFCLK1	E12	I	Table 25
RESET_L	M15	I, ST, IP	Table 32
RxCLK0	E3	O, TS, ID	Table 27
RxCLK1	B11	O, TS, ID	Table 27
RxData0	B1	O, TS, ID	Table 27
RxData1	B4	O, TS, ID	Table 27
RxData2	C7	O, TS, ID	Table 27
RxData3	B9	O, TS, ID	Table 27
RxData4	C12	O, TS, ID	Table 27
RxData5	B15	O, TS, ID	Table 27
RxData6	B17	O, TS, ID	Table 27
RxData7	F14	O, TS, ID	Table 27
RxSYNC0	E4	O, TS, ID	Table 27
RxSYNC1	B12	O, TS, ID	Table 27
SD_2P5V	P1	I, ST, ID	Table 29
SD0	P2	I	Table 29
SD1	N4	I	Table 29
SD2	P3	I	Table 29
SD3	N5	I	Table 29
SD4	P15	I	Table 29

Signal	Ball	Type[1]	Reference for Full Description
SD5	P16	I	Table 29
SD6	P17	I	Table 29
SD7	N17	I	Table 29
SECTION	L15	I, ID, ST	Table 32
SGND	K14	–	Table 34
TCK	M16	I, ST, ID	Table 31
TDI	N14	I, ST, IP	Table 31
TDO	N15	O, TS	Table 31
TMS	N16	I, ST, IP	Table 31
TPFIN0	T1	AO/AI	Table 30
TPFIN1	T4	AO/AI	Table 30
TPFIN2	T5	AO/AI	Table 30
TPFIN3	R8	AO/AI	Table 30
TPFIN4	U9	AO/AI	Table 30
TPFIN5	T12	AO/AI	Table 30
TPFIN6	T13	AO/AI	Table 30
TPFIN7	T16	AO/AI	Table 30
TPFIP0	R2	AO/AI	Table 30
TPFIP1	U3	AO/AI	Table 30
TPFIP2	R6	AO/AI	Table 30
TPFIP3	T8	AO/AI	Table 30
TPFIP4	T9	AO/AI	Table 30
TPFIP5	U13	AO/AI	Table 30
TPFIP6	R12	AO/AI	Table 30
TPFIP7	R16	AO/AI	Table 30
TPFON0	U1	AO/AI	Table 30
TPFON1	R4	AO/AI	Table 30
TPFON2	U5	AO/AI	Table 30
TPFON3	T7	AO/AI	Table 30
TPFON4	R10	AO/AI	Table 30
TPFON5	U11	AO/AI	Table 30
TPFON6	U15	AO/AI	Table 30
TPFON7	T15	AO/AI	Table 30
TPFOP0	T2	AO/AI	Table 30
TPFOP1	T3	AO/AI	Table 30
TPFOP2	T6	AO/AI	Table 30
TPFOP3	U7	AO/AI	Table 30

Signal	Ball	Type[1]	Reference for Full Description
TPFOP4	T10	AO/AI	Table 30
TPFOP5	T11	AO/AI	Table 30
TPFOP6	T14	AO/AI	Table 30
TPFOP7	R14	AO/AI	Table 30
TRST_L	M17	I, IP, ST	Table 31
TxCLK0	C8	I, ID	Table 27
TxCLK1	D17	I, ID	Table 27
TxData0	E2	I, ID	Table 25
TxData1	C3	I, ID	Table 25
TxData2	B5	I, ID	Table 25
TxData3	D8	I, ID	Table 25
TxData4	A11	I, ID	Table 25
TxData5	B13	I, ID	Table 25
TxData6	D13	I, ID	Table 25
TxData7	E14	I, ID	Table 25
TxSLEW_0	N3	I, ST, ID	Table 32
TxSLEW_1	M4	I, ST, ID	Table 32
TxSYNC0	A6	I, ID	Table 27
TxSYNC1	C16	I, ID	Table 27
VCCD	F5	–	Table 34
VCCD	G13	–	Table 34
VCCD	J5	–	Table 34
VCCD	J14	–	Table 34
VCCIO	A2	–	Table 34
VCCIO	A8	–	Table 34
VCCIO	C1	–	Table 34
VCCIO	C11	–	Table 34
VCCIO	D14	–	Table 34
VCCPECL	L5	–	Table 34
VCCPECL	L13	–	Table 34
VCCR	N13	–	Table 34
VCCR	P4	–	Table 34
VCCR	P7	–	Table 34
VCCR	P8	–	Table 34
VCCR	P9	–	Table 34
VCCR	P10	–	Table 34
VCCR	P11	–	Table 34
VCCR	P12	–	Table 34
VCCT	N6	–	Table 34
VCCT	N7	–	Table 34
VCCT	N9	–	Table 34
VCCT	N11	–	Table 34
VCCT	N12	–	Table 34

Table 23 SS-SMII BGA23 Ball List in Alphanumeric Order by Ball Location

Ball	Signal	Type[1]	Reference for Full Description
A1	GNDD	–	Table 34
A2	VCCIO	–	Table 34
A3	NC	–	Table 35
A4	NC	–	Table 35
A5	NC	–	Table 35
A6	TxSYNC0	I, ID	Table 27
A7	NC	–	Table 35
A8	VCCIO	–	Table 34
A9	GNDD	–	Table 34
A10	MDIO1	I/O, TS, SL, IP	Table 28
A11	TxData4	I, ID	Table 25
A12	FIFOSEL0	I, ID, ST	Table 32
A13	NC	–	Table 35
A14	NC	–	Table 35
A15	FIFOSEL1	I, ID, ST	Table 32
A16	NC	–	Table 35
A17	NC/ LINKHOLD	I, ID, ST	Table 35 Table 32
B1	RxData0	O, TS, ID	Table 27
B2	NC	–	Table 35
B3	GNDD	–	Table 34
B4	RxData1	O, TS, ID	Table 27
B5	TxData2	I, ID	Table 25
B6	NC	–	Table 35
B7	GNDD	–	Table 34
B8	NC	–	Table 35
B9	RxData3	O, TS, ID	Table 27
B10	MDC1	I, ST, ID	Table 28
B11	RxCLK1	O, TS, ID	Table 27
B12	RxSYNC1	O, TS, ID	Table 27
B13	TxData5	I, ID	Table 25
B14	NC	–	Table 35
B15	RxData5	O, TS, ID	Table 27
B16	NC	–	Table 35
B17	RxData6	O, TS, ID	Table 27
C1	VCCIO	–	Table 34
C2	NC	–	Table 35
C3	TxData1	I, ID	Table 25
C4	NC	–	Table 35
C5	GNDD	–	Table 34
C6	NC	–	Table 35
C7	RxData2	O, TS, ID	Table 27
C8	TxCLK0	I, ID	Table 27
C9	MDINT1_L	OD, TS, SL, IP	Table 28
C10	NC	–	Table 35
C11	VCCIO	–	Table 34
C12	RxData4	O, TS, ID	Table 27
C13	GNDD	–	Table 34
C14	NC	–	Table 35
C15	NC	–	Table 35
C16	TxSYNC1	I, ID	Table 27
C17	GNDD	–	Table 34
D1	GNDD	–	Table 34
D2	MDIX	I, ID, ST	Table 32
D3	GNDD	–	Table 34
D4	NC	–	Table 35
D5	PAUSE	ID, I, ST	Table 32
D6	GNDD	–	Table 34
D7	PREASEL	I, ID, ST	Table 32
D8	TxData3	I, ID	Table 25
D9	NC	–	Table 35
D10	GNDD	–	Table 34
D11	NC	–	Table 35
D12	NC	–	Table 35
D13	TxData6	I, ID	Table 25
D14	VCCIO	–	Table 34
D15	GNDD	–	Table 34
D16	NC	–	Table 35
D17	TxCLK1	I, ID	Table 27
E1	MDC0	I, ST, ID	Table 28
E2	TxData0	I, ID	Table 25
E3	RxCLK0	O, TS, ID	Table 27
E4	RxSYNC0	O, TS, ID	Table 27
E5	GNDD	–	Table 34

Ball	Signal	Type[1]	Reference for Full Description
E6	REFCLK0	I	Table 25
E7	GNDD	–	Table 34
E8	No Ball	–	–
E9	GNDD	–	Table 34
E10	No Ball	–	–
E11	GNDD	–	Table 34
E12	REFCLK1	I	Table 25
E13	GNDD	–	Table 34
E14	TxData7	I, ID	Table 25
E15	NC	–	Table 35
E16	NC	–	Table 35
E17	GNDD	–	Table 34
F1	MDINT0_L	OD, TS, SL, IP	Table 28
F2	LED3_1_L	OD, TS, SL, IP	Table 33
F3	MDIO0	I/O, TS, SL, IP	Table 28
F4	NC	–	Table 35
F5	VCCD	–	Table 34
F6	No ball	–	–
F7	No ball	–	–
F8	No ball	–	–
F9	No Ball	–	–
F10	No Ball	–	–
F11	No Ball	–	–
F12	No Ball	–	–
F13	GNDD	–	Table 34
F14	RxData7	O, TS, ID	Table 27
F15	NC	–	Table 35
F16	LED7_3_L	OD, TS, SL, IP	Table 33
F17	LED7_2_L	OD, TS, SL, IP	Table 33
G1	LED2_3_L	OD, TS, SL, IP	Table 33
G2	NC	–	Table 35
G3	LED3_2_L	OD, TS, SL, IP	Table 33
G4	LED3_3_L	OD, TS, SL, IP	Table 33

Ball	Signal	Type[1]	Reference for Full Description
G5	NC	–	Table 35
G6	No Ball	–	–
G7	No Ball	–	–
G8	No Ball	–	–
G9	No Ball	–	–
G10	No Ball	–	–
G11	No Ball	–	–
G12	No Ball	–	–
G13	VCCD	–	Table 34
G14	NC	–	Table 35
G15	LED7_1_L	OD, TS, SL, IP	Table 33
G16	NC	–	Table 35
G17	LED6_3_L	OD, TS, SL, IP	Table 33
H1	LED1_3_L	OD, TS, SL, IP	Table 33
H2	LED2_1_L	OD, TS, SL, IP	Table 33
H3	LED2_2_L	OD, TS, SL, IP	Table 33
H4	NC	–	Table 35
H5	No Ball	–	–
H6	No Ball	–	–
H7	No Ball	–	–
H8	GNDD	–	Table 34
H9	GNDD	–	Table 34
H10	GNDD	–	Table 34
H11	No Ball	–	–
H12	No Ball	–	–
H13	No Ball	–	–
H14	NC	–	Table 35
H15	LED6_1_L	OD, TS, SL, IP	Table 33
H16	LED6_2_L	OD, TS, SL, IP	Table 33
H17	LED5_3_L	OD, TS, SL, IP	Table 33
J1	LED0_3_L	OD, TS, SL, IP	Table 33
J2	NC	–	Table 35

Ball	Signal	Type[1]	Reference for Full Description
J3	LED1_2_L	OD, TS, SL, IP	Table 33
J4	LED1_1_L	OD, TS, SL, IP	Table 33
J5	VCCD	–	Table 34
J6	No Ball	–	–
J7	No Ball	–	–
J8	GNDD	–	Table 34
J9	GNDD	–	Table 34
J10	GNDD	–	Table 34
J11	No Ball		–
J12	No Ball	–	–
J13	NC	–	Table 35
J14	VCCD	–	Table 34
J15	LED5_1_L	OD, TS, SL, IP	Table 33
J16	LED5_2_L	OD, TS, SL, IP	Table 33
J17	LED4_3_L	OD, TS, SL, IP	Table 33
K1	AMDIX_EN	I, ST, IP	Table 32
K2	LED0_2_L	OD, TS, SL, IP	Table 33
K3	LED0_1_L	OD, TS, SL, IP	Table 33
K4	NC	–	Table 35
K5	No Ball	–	–
K6	No Ball	–	–
K7	No Ball	–	–
K8	GNDD	–	Table 34
K9	GNDD	–	Table 34
K10	GNDD	–	Table 34
K11	No Ball	–	–
K12	No Ball	–	–
K13	No Ball	–	–
K14	SGND	–	Table 34
K15	NC	–	Table 35
K16	LED4_1_L	OD, TS, SL, IP	Table 33
K17	LED4_2_L	OD, TS, SL, IP	Table 33
L1	MDDIS	I, ST, ID	Table 28

Ball	Signal	Type[1]	Reference for Full Description
L2	CFG_3	I, ST, ID	Table 32
L3	CFG_2	I, ST, ID	Table 32
L4	ADD_4	I, ST, ID	Table 32
L5	VCCPECL	–	Table 34
L6	No Ball	–	–
L7	No Ball	–	–
L8	No Ball	–	–
L9	No Ball	–	–
L10	No Ball	–	–
L11	No Ball	–	–
L11	No Ball	–	–
L13	VCCPECL	–	Table 34
L14	PWRDWN	I, ST, ID	Table 32
L15	SECTION	I, ID, ST	Table 32
L16	ModeSel0	I, ST, ID	Table 32
L17	ModeSel1	I, ST, ID	Table 32
M1	CFG_1	I, ST, ID	Table 32
M2	ADD_3	I, ST, ID	Table 32
M3	ADD_2	I, ST, ID	Table 32
M4	TxSLEW_1	I, ST, ID	Table 32
M5	GNDPECL	–	Table 34
M6	No Ball	–	–
M7	No Ball	–	–
M8	No Ball	–	–
M9	No Ball	–	–
M10	No Ball	–	–
M11	No Ball	–	–
M12	No Ball	–	–
M13	GNDPECL	–	Table 34
M14	G_FX/TP_L	I, ID, ST	Table 32
M15	RESET_L	I, IP, ST	Table 32
M16	TCK	I, ST, ID	Table 31
M17	TRST_L	I, IP, ST	Table 31
N1	ADD_1	I, ID, ST	Table 32
N2	ADD_0	I, ID, ST	Table 32
N3	TxSLEW_0	I, ID, ST	Table 32
N4	SD1	I	Table 29
N5	SD3	I	Table 29

Ball	Signal	Type[1]	Reference for Full Description
N6	VCCT	–	Table 34
N7	VCCT	–	Table 34
N8	No Ball	–	–
N9	VCCT	–	Table 34
N10	No Ball	–	–
N11	VCCT	–	Table 34
N12	VCCT	–	Table 34
N13	VCCR	–	Table 34
N14	TDI	I, ST, IP	Table 31
N15	TDO	O, TS	Table 31
N16	TMS	I, ST, IP	Table 31
N17	SD7	I	Table 29
P1	SD_2P5V	I, ST, ID	Table 29
P2	SD0	I	Table 29
P3	SD2	I	Table 29
P4	VCCR	–	Table 34
P5	GNDR	–	Table 34
P6	GNDR	–	Table 34
P7	VCCR	–	Table 34
P8	VCCR	–	Table 34
P9	VCCR	–	Table 34
P10	VCCR	–	Table 34
P11	VCCR	–	Table 34
P12	VCCR	–	Table 34
P13	GNDR	–	Table 34
P14	GNDT	–	Table 34
P15	SD4	I	Table 29
P16	SD5	I	Table 29
P17	SD6	I	Table 29
R1	GNDT	–	Table 34
R2	TPFIP0	AO/AI	Table 30
R3	GNDT	–	Table 34
R4	TPFON1	AO/AI	Table 30
R5	GNDT	–	Table 34
R6	TPFIP2	AO/AI	Table 30
R7	GNDR	–	Table 34
R8	TPFIN3	AO/AI	Table 30
R9	GNDR	–	Table 34

Ball	Signal	Type[1]	Reference for Full Description
R10	TPFON4	AO/AI	Table 30
R11	GNDR	–	Table 34
R12	TPFIP6	AO/AI	Table 30
R13	GNDR	–	Table 34
R14	TPFOP7	AO/AI	Table 30
R15	GNDT	–	Table 34
R16	TPFIP7	AO/AI	Table 30
R17	GNDT	–	Table 34
T1	TPFIN0	AO/AI	Table 30
T2	TPFOP0	AO/AI	Table 30
T3	TPFOP1	AO/AI	Table 30
T4	TPFIN1	AO/AI	Table 30
T5	TPFIN2	AO/AI	Table 30
T6	TPFOP2	AO/AI	Table 30
T7	TPFON3	AO/AI	Table 30
T8	TPFIP3	AO/AI	Table 30
T9	TPFIP4	AO/AI	Table 30
T10	TPFOP4	AO/AI	Table 30
T11	TPFOP5	AO/AI	Table 30
T12	TPFIN5	AO/AI	Table 30
T13	TPFIN6	AO/AI	Table 30
T14	TPFOP6	AO/AI	Table 30
T15	TPFON7	AO/AI	Table 30
T16	TPFIN7	AO/AI	Table 30
T17	GNDT	–	Table 34
U1	TPFON0	AO/AI	Table 30
U2	GNDT	–	Table 34
U3	TPFIP1	AO/AI	Table 30
U4	GNDT	–	Table 34
U5	TPFON2	AO/AI	Table 30
U6	GNDT	–	Table 34
U7	TPFOP3	AO/AI	Table 30
U8	GNDR	–	Table 34
U9	TPFIN4	AO/AI	Table 30
U10	GNDT	–	Table 34
U11	TPFON5	AO/AI	Table 30
U12	GNDT	–	Table 34
U13	TPFIP5	AO/AI	Table 30

Ball	Signal	Type[1]	Reference for Full Description
U14	GNDT	–	Table 34
U15	TPFON6	AO/AI	Table 30
U16	GNDT	–	Table 34
U17	GNDT	–	Table 34

3.4 BGA23 Signal Descriptions

3.4.1 Signal Name Conventions

Signal names may contain either a port designation or a serial designation, or a combination of the two designations. Signal naming conventions are as follows:

- **Port Number Only.** Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by the Port Designation. For example, Transmit Enable signals would be identified as TxEN0, TxEN1, and TxEN2.
- **Serial Number Only.** A set of signals which are not tied to any specific port are designated by the Signal Mnemonic, followed by an underscore and a serial designation. For example, a set of three Global Configuration signals would be identified as CFG_1, CFG_2, and CFG_3.
- **Port and Serial Number.** In cases where each port is assigned a set of multiple signals, each signal is designated in the following order: Signal Mnemonic, Port Designation, an underscore, and the serial designation. For example, a set of three Port Configuration signals would be identified as RxData0_0 and RxData0_1, RxData1_0 and RxData1_1, and RxData2_0 and RxData2_1.

3.4.2 Signal Descriptions – RMII, SMII, and SS-SMII Configurations

Table 24 RMII Signal Descriptions – BGA23 (Sheet 1 of 3)

Ball/Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
E6, E12	44 6	REFCLK0 REFCLK1	I	**Reference Clock.** 50 MHz RMII reference clock is always required. RMII inputs are sampled on the rising edge of REFCLK, RMII outputs are sourced on the falling edge.
E2, F4	61 62	TxData0_0 TxData0_1	I, ID	**Transmit Data - Port 0.** Inputs containing 2-bit parallel di-bits to be transmitted from port 0 are clocked in synchronously to REFCLK.
C3, D4	52 53	TxData1_0 TxData1_1	I, ID	**Transmit Data - Port 1.** Inputs containing 2-bit parallel di-bits to be transmitted from port 1 are clocked in synchronously to REFCLK
B5 A4	42 43	TxData2_0 TxData2_1	I, ID	**Transmit Data - Port 2.** Inputs containing 2-bit parallel di-bits to be transmitted from port 2 are clocked in synchronously to REFCLK.
D8, A6	34 35	TxData3_0 TxData3_1	I, ID	**Transmit Data - Port 3.** Inputs containing 2-bit parallel di-bits to be transmitted from port 3 are clocked in synchronously to REFCLK.
A11, C10	22 23	TxData4_0 TxData4_1	I, ID	**Transmit Data - Port 4.** Inputs containing 2-bit parallel di-bits to be transmitted from port 4 are clocked in synchronously to REFCLK.
B13, D11	13 14	TxData5_0 TxData5_1	I, ID	**Transmit Data - Port 5.** Inputs containing 2-bit parallel di-bits to be transmitted from port 5 are clocked in synchronously to REFCLK.
D13, A16	4 5	TxData6_0 TxData6_1	I, ID	**Transmit Data - Port 6.** Inputs containing 2-bit parallel di-bits to be transmitted from port 6 are clocked in synchronously to REFCLK.
E14, C16	203 204	TxData7_0 TxData7_1	I, ID	**Transmit Data - Port 7.** Inputs containing 2-bit parallel di-bits to be transmitted from port 7 are clocked in synchronously to REFCLK.
E3, B2, C6, A7, B11, A14, C14, D16	60 51 41 33 21 12 3 202	TxEN0 TxEN1 TxEN2 TxEN3 TxEN4 TxEN5 TxEN6 TxEN7	I, ID	**Transmit Enable - Ports 0-7.** Active High input enables respective port transmitter. This signal must be synchronous to the REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 24 RMII Signal Descriptions – BGA23 (Sheet 2 of 3)

Ball/Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
C2, B1	55 54	RxData0_0 RxData0_1	O, TS O, TS, ID	**Receive Data - Port 0.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
A3, B4	46 45	RxData1_0 RxData1_1	O, TS O, TS, ID	**Receive Data - Port 1.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
B6, C7	37 36	RxData2_0 RxData2_1	O, TS O, TS, ID	**Receive Data - Port 2.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
D9, B9	28 27	RxData3_0 RxData3_1	O, TS O, TS, ID	**Receive Data - Port 3.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
A13, C12	16 15	RxData4_0 RxData4_1	O, TS O, TS, ID	**Receive Data - Port 4.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
B14, B15	8 7	RxData5_0 RxData5_1	O, TS O, TS, ID	**Receive Data - Port 5.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
C15, B17	206 205	RxData6_0 RxData6_1	O, TS O, TS, ID	**Receive Data - Port 6.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 24 RMII Signal Descriptions – BGA23 (Sheet 3 of 3)

Ball/Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
E16, F14	198 197	RxData7_0 RxData7_1	O, TS O, TS, ID	**Receive Data - Port 7.** Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
E4, C4, A5, B8, B12, D12, B16, E15	58 49 39 31 17 10 1 200	CRS_DV0 CRS_DV1 CRS_DV2 CRS_DV3 CRS_DV4 CRS_DV5 CRS_DV6 CRS_DV7	O, TS, SL, ID	**Carrier Sense/Receive Data Valid - Ports 0-7.** On detection of valid carrier, these signals are asserted asynchronously with respect to REFCLK. CRS_DVn is de-asserted on loss of carrier, synchronous to REFCLK.
D2, D5, D7, C8, A12, A15, A17, D17	59 50 40 32 20 11 2 201	RxER0 RxER1 RxER2 RxER3 RxER4 RxER5 RxER6 RxER7	O, TS, SL, ID, I, ST	**Receive Error - Ports 0-7.** These signals are synchronous to the respective REFCLK. Active High indicates that received code group is invalid, or that PLL is not locked. The RxER signals have the following additional function pins: RxER0 (MDIX) RxER1 (PAUSE) RxER2 (PREASEL) RxER4 (FIFOSEL0) RxER5 (FIFOSEL1) RxER6 {LINKHOLD)

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7]_0, RxData[0:7]_1, CRS_DV[0:7] and RxER[0:7] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 25 SMII/SS-SMII Common Signal Descriptions – BGA23

Ball/Pin Designation		Symbol	Type[1]	Signal Description[2]
BGA23	PQFP			
E2, C3, B5, D8, A11, B13, D13, E14	61, 52, 42, 34, 22, 13, 4, 203	TxData0, TxData1, TxData2, TxData3, TxData4, TxData5, TxData6, TxData7	I, ID	**Transmit Data - Ports 0-7.** These serial input streams provide data to be transmitted to the network. The LXT9785/LXT9785E clocks the data in synchronously to REFCLK.
E6, E12	44, 6	REFCLK0, REFCLK1	I	**Reference Clock.** The LXT9785/LXT9785E always requires a 125 MHz reference clock input. Refer to Functional Description for detailed clock requirements. REFCLK0 and REFCLK1 are always connected regardless of sectionalization mode.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.

Table 26 SMII Specific Signal Descriptions – BGA23

Pin/Ball Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
A6, C16	35, 204	SYNC0, SYNC1	I, ID	**SMII Synchronization.** The MAC must generate a SYNC pulse every 10 REFCLK cycles to synchronize the SMII. SYNC0 is used when 1x8 port sectionalization is selected. SYNC0 and SYNC1 are to be used when 2x4 port sectionalization is chosen.
C2, A3, B6, D9, A13, B14, C15, E16	55, 46, 37, 28, 16, 8, 206, 198	RxData0, RxData1, RxData2, RxData3, RxData4, RxData5, RxData6, RxData7	O, TS	**Receive Data - Ports 0-7**. These serial output streams provide data received from the network. The LXT9785/LXT9785E drives the data out synchronously to RXCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.
3. RxData[0:7] outputs are three-stated in Isolation and hardware power-down modes and during hardware reset.

Table 27 SS-SMII Specific Signal Descriptions – BGA23

Ball / Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
A6, C16	35, 204	TxSYNC0, TxSYNC1	I, ID	**SS-SMII Transmit Synchronization.** The MAC must generate a TxSYNC pulse every 10 TxCLK cycles to mark the start of TxData segments. TxSYNC0 is used when 1x8 port sectionalization is selected.
E4, B12	58, 17	RxSYNC0, RxSYNC1	O, TS, ID	**SS-SMII Receive Synchronization.** The LXT9785/LXT9785E generates these pulses every 10 RxCLK cycles to mark the start of RxData segments for the MAC. RxSYNC1 is used when 1x8 port sectionalization is selected. RxSYNC0 may not be used. These outputs are only enabled when SS-SMII mode is enabled.
C8, D17	32, 201	TxCLK0, TxCLK1	I, ID	**SS-SMII Transmit Clock.** The MAC sources this 125 MHz clock as the timing reference for TxData and TxSYNC. Only TxCLK0 is used when 1x8 port sectionalization is selected.
E3, B11	60, 21	RxCLK0, RxCLK1	O, TS, ID	**SS-SMII Receive Clock.** The LXT9785/LXT9785E generates these clocks, based on REFCLK, to provide a timing reference for RxData and RxSYNC to the MAC. RxCLK1 is used when 1x8 port sectionalization is selected. RxCLK0 may not be used.
B1, B4, C7, B9, C12, B15, B17, F14	54, 45, 36, 27, 15, 7, 205, 197	RxData0, RxData1, RxData2, RxData3, RxData4, RxData5, RxData6, RxData7	O, TS, ID	**Receive Data - Ports 0-7.** These serial output streams provide data received from the network. The LXT9785/LXT9785E drives the data out synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. RxData[0:7], RxSYNC[0:1], and RxCLK[0:1] outputs are three-stated in Isolation and H/W Power-Down modes and during H/W reset.

Table 28 MDIO Control Interface Signals – BGA23

Ball/Pin Designation		Symbol	Type[1]	Signal Description[2,3,4]
BGA23	PQFP			
F3, A10	64 25	MDIO0 MDIO1	I/O, TS, SL, IP	**Management Data Input/Output.** Bidirectional serial data channel for communication between the PHY and MAC or switch ASIC. Only MDIO0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDIO0 accesses ports 0-3 and MDIO1 accesses ports 4-7. Refer to Figure 21, *Typical SS-SMII Quad Sectionalization*, on page 136.
F1, C9	67 26	MDINT0_L MDINT1_L	OD, TS, SL, IP	**Management Data Interrupt.** When Register bit 18.1 = 1, an active Low output on this Pin indicates status change. Only MDINT0_L is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDINT0_L is associated with ports 0-3 and MDINT1_L is associated with ports 4-7. Refer to Figure 21, *Typical SS-SMII Quad Sectionalization*, on page 136.
E1, B10	63 24	MDC0 MDC1	I, ST, ID	**Management Data Clock.** Clock for the MDIO serial data channel. Maximum frequency is 20 MHz. Only MDC0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDC0 clocks ports 0-3 register accesses and MDC1 clocks ports 4-7 register accesses. Refer to Figure 21, *Typical SS-SMII Quad Sectionalization*, on page 136.
L1	84	MDDIS	I, ST, ID	**Management Disable.** When MDDIS is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power up and reset. When MDDIS is pulled Low at power up or reset, via the internal pull-down resistor or by tying it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a Pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. MDIO[0:1] and MDINT[0:1]_L outputs are three-stated in H/W Power-Down mode and during H/W reset.
4. Supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 29 Signal Detect – BGA23

Ball/Pin Designation		Symbol	Type[1]	Signal Description2,3
BGA23	PQFP			
P1	95	SD_2P5V	I, ST, ID	**Signal Detect 2.5 Volt Interface.** SD input threshold voltage select. **Tie to VCCPECL =** Select 2.5 V LVPECL input levels **Float or Tie to GNDPECL =** Select 3.3 V LVPECL input levels
P2, N4, P3, N5, P15, P16, P17, N17	96 97 100 101 161 162 165 166	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	I	**Signal Detect - Ports 0-7.** Signal Detect input from the fiber transceiver (these inputs are only active for ports operating in fiber mode). **Logic High =** Normal operation (the process of searching for receive idles for the purpose of bringing link up is initiated) **Logic Low =** Link is declared lost

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode.
3. Tie SD[0:7] inputs to GNDPECL if unused.

Table 30 Network Interface Signal Descriptions – BGA23

Ball/Pin Designation		Symbol	Type[1]	Signal Description
BGA23	PQFP			
T2, U1, T3, R4, T6, U5, U7, T7, T10, R10, T11, U11, T14,U15, R14, T15	107, 108 111, 110 121, 122 125, 124 136, 137 140, 139 150, 151 154, 153	TPFOP0, TPFON0 TPFOP1, TPFON1 TPFOP2, TPFON2 TPFOP3, TPFON3 TPFOP4, TPFON4 TPFOP5, TPFON5 TPFOP6, TPFON6 TPFOP7, TPFON7	AO/AI	**Twisted-Pair/Fiber Outputs[2], Positive & Negative, Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPFO pins drive 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFO pins produce differential LVPECL outputs for fiber transceivers.
R2, T1, U3, T4, R6, T5, T8, R8, T9, U9, U13, T12, R12, T13, R16, T16	104, 105 115, 114 118, 119 129, 128 132, 133 143, 142 146, 147 157, 156	TPFIP0, TPFIN0 TPFIP1, TPFIN1 TPFIP2, TPFIN2 TPFIP3, TPFIN3 TPFIP4, TPFIN4 TPFIP5, TPFIN5 TPFIP6, TPFIN6 TPFIP7, TPFIN7	AI/AO	**Twisted-Pair/Fiber Inputs[3], Positive & Negative, Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPFI pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFI pins receive differential LVPECL inputs from fiber transceivers.

1. Type Column Coding: AI = Analog Input, AO = Analog Output.
2. Switched to Inputs (see TPFIP/N description) when not in fiber mode and MDIX is not active [that is, twisted-pair, non-crossover MDI mode].
3. Switched to Outputs (see TPFOP/N description) when not in fiber mode and MDIX is not active [that is, twisted-pair, non-crossover MDI mode].

Table 31 JTAG Test Signal Descriptions – BGA23

Ball / Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
N14	167	TDI	I, ST, IP	**Test Data Input.** Test data sampled with respect to the rising edge of TCK.
N15	168	TDO	O, TS	**Test Data Output.** Test data driven with respect to the falling edge of TCK.
N16	169	TMS	I, ST, IP	**Test Mode Select.**
M16	170	TCK	I, ST, ID	**Test Clock.** Clock input for JTAG test.
M17	171	TRST_L	I, ST, IP	**Test Reset.** Reset input for JTAG test.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain, TS = Three-State-able output, SMT = Schmitt Triggered input, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. TDO output is three-stated in H/W Power-Down mode and during H/W reset.

Table 32 Miscellaneous Signal Descriptions – BGA23 (Sheet 1 of 4)

<table>
<tr><th colspan="2">Ball / Pin Designation</th><th rowspan="2">Symbol</th><th rowspan="2">Type[1]</th><th rowspan="2">Signal Description[2]</th></tr>
<tr><th>BGA23</th><th>PQFP</th></tr>
<tr><td>N3,
M4</td><td>94
93</td><td>TxSLEW_0
TxSLEW_1</td><td>I, ST, ID</td><td>Tx Output Slew Controls 0 and 1 Defaults.
These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 27.11:10 for all ports. These register bits can be read and overwritten after startup / reset.
These pins select the TX output slew rate for all ports (rise and fall time) as follows:
<table><tr><th>TxSLEW_1</th><th>TxSLEW_0</th><th>Slew Rate (Rise and Fall Time)</th></tr><tr><td>0</td><td>0</td><td>3.3 ns</td></tr><tr><td>0</td><td>1</td><td>3.6 ns</td></tr><tr><td>1</td><td>0</td><td>3.9 ns</td></tr><tr><td>1</td><td>1</td><td>4.2 ns</td></tr></table></td></tr>
<tr><td>D5</td><td>50</td><td>PAUSE</td><td>ID, I, ST</td><td>Pause Default.
This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 4.10 for all ports. This register bit can be read and overwritten after startup / reset.
When High, the LXT9785/LXT9785E advertises Pause capabilities on all ports during auto-negotiation.
This pin is shared with RMII-RxER1. An external pull-up resistor (see applications section for value) can be used to set Pause active while RxER1 is three-stated during H/W reset. If no pull-up is used, the default Pause state is set inactive via the internal pull-down resistor.</td></tr>
<tr><td>L14</td><td>174</td><td>PWRDWN</td><td>I, ST, ID</td><td>Power-Down.
When High, forces the LXT9785/LXT9785E into global power-down mode.
Pin is not on JTAG chain.</td></tr>
<tr><td>M15</td><td>175</td><td>RESET_L</td><td>I, ST, IP</td><td>Reset.
This active low input is ORed with the control register Reset Register bit 0.15. When held Low, all outputs are forced to inactive state.
Pin is not on JTAG chain.</td></tr>
<tr><td colspan="5">1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).</td></tr>
</table>

Table 32 Miscellaneous Signal Descriptions – BGA23 (Sheet 2 of 4)

Ball / Pin Designation		Symbol	Type[1]	Signal Description[2]
BGA23	PQFP			
L4, M2, M3, N1, N2	88 89 90 91 92	ADD_4 ADD_3 ADD_2 ADD_1 ADD_0	I, ST, ID	**Address <4:0>.** Sets base address. Each port adds its port number (starting with 0) to this address to determine its PHY address. Port 0 Address = Base Port 1 Address = Base + 1 Port 2 Address = Base + 2 Port 3 Address = Base + 3 Port 4 Address = Base + 4 Port 5 Address = Base + 5 Port 6 Address = Base + 6 Port 7 Address = Base + 7
L17, L16	178 177	MODESEL_1 MODESEL_0	I, ST, ID	**Mode Select[1:0].** 00 = RMII 01 = SMII 10 = SS-SMII 11 = Reserved All ports are configured the same. Interfaces cannot be mixed and must be all RMII, SMII, or SS-SMII.
L15	176	SECTION	I, ST, ID	**Sectionalization Select.** This pin selects sectionalization into separate ports. 0 = 1x8 ports, 1 = 2x4 ports
K1	83	AMDIX_EN	I, ST, IP	**Auto MDI/MDIX Enable Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.9 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 40, *MDIX Selection*, on page 116. When active (High), automatic MDI crossover (MDIX) (regardless of segmentation) is selected for all ports. When inactive (Low) MDIX is selected according to the MDIX pin.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 32 Miscellaneous Signal Descriptions – BGA23 (Sheet 3 of 4)

Ball / Pin Designation		Symbol	Type[1]	Signal Description[2]
BGA23	PQFP			
D2	59	MDIX	I, ID, ST	**MDIX Select Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.8 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 40, *MDIX Selection*, on page 116. When AMDIX_EN is active this pin is ignored. When AMDIX_EN is inactive, all ports are forced to the MDI or the MDIX function regardless of segmentation. If this pin is active (high), MDI crossover (MDIX) is selected. If this pin is inactive, non-crossover MDI mode is set. This pin is shared with RMII-RxER0. An external pull-up resistor (see applications section for value) can be used to set MDIX active while RxER0 is three-stated during H/W reset. If no pull-up is used, the default MDIX state is set inactive via the internal pull-down resistor. Do not tie this pin directly to VCCIO (vs. using a pull-up) in non-RMII modes.
L2, L3, M1	85 86 87	CFG_3 CFG_2 CFG_1	I, ST, ID	**Global Port Configuration Defaults 1-3.** These pins are read at startup or reset. Their value at that time is used to set the default state of register bits shown in Table 42, *Global Hardware Configuration Settings*, on page 126 for all ports. These register bits can be read and overwritten after startup / reset. When operating in Hardware Control Mode, these pins provide configuration control options for all the ports (refer to Table 42, *Global Hardware Configuration Settings*, on page 126 for details).
M14	173	G_FX/TP_L	I, ST, ID	**Global FX/TP_L Enable Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 16.0 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 93, *Port Configuration Register (Address 16, Hex 10)*, on page 199. This input selects whether all the ports are defaulted to TP vs. FX mode.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 32 Miscellaneous Signal Descriptions – BGA23 (Sheet 4 of 4)

Ball / Pin Designation		Symbol	Type[1]	Signal Description[2]
BGA23	PQFP			
A15 A12	11 20	FIFOSEL1 FIFOSEL0	I, ID, ST	**FIFO Select <1:0>.** These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 18.15:14 for all ports. These register bits can be read and overwritten after startup/reset. These pins are shared with RMII-RxER<5:4>. An external pull-up resistor (see applications section for value) can be used to set FIFO Select<1:0> to active while RxER<5:4> are three-stated during hardware reset. If no pull-up is used, the default FIFO select state is set via the internal pull-down resistors. See Table 36, *Receive FIFO Depth Configurations*, on page 96.
D7	40	PREASEL	I, ID, ST	**Preamble Select.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 16.5 for all ports. This register bit can be read and overwritten after startup/reset. This pin is shared with RMII-RxER2. An external pull-up resistor (see applications section for value) can be used to set Preamble Select to active while RxER2 is three-stated during hardware reset. If no pull-up is used, the default Preamble Select state is set via the internal pull-down resistors. **Note:** Preamble select has no effect in 100 Mbps operation.
A17	2	LINKHOLD[3]	I, ID, ST	**LINKHOLD Defaul**t. This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 0.11 for all ports. This register bit can be read and overwritten after startup / reset. When High, the LXT9785/LXT9785E powers down all ports. This pin is shared with RMII-RxER6. An external pull-up resistor (see applications section for value) can be used to set LINKHOLD active while RxER6 is tri-stated during H/W reset. If no pull-up is used, the default LINKHOLD state is set inactive via the internal pull-down resistor.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain Output, ST = Schmitt Triggered Input, TS = Three-State-able Output, SL = Slew-rate Limited Output, IP = Weak Internal Pull-Up, ID = Weak Internal Pull-Down.
2. The IP/ID resistors are disabled during hardware power-down mode.
3. The LINKHOLD ability is available only for stepping 4 (Revision D0).

Table 33 LED Signal Descriptions – BGA23 (Sheet 1 of 2)

Ball / Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
K3, K2, J1	82 81 80	LED0_1_L LED0_2_L LED0_3_L	OD, TS, SL, IP	**Port 0 LED Drivers 1-3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
J4, J3, H1	77 76 75	LED1_1_L LED1_2_L LED1_3_L	OD, TS, SL, IP	**Port 1 LED Drivers 1-3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
H2, H3, G1	73 72 71	LED2_1_L LED2_2_L LED2_3_L	OD, TS, SL, IP	**Port 2 LED Drivers 1-3.** These pins drive LED indicators for Port 2. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
F2, G3, G4	70 69 68	LED3_1_L LED3_2_L LED3_3_L	OD, TS, SL, IP	**Port 3 LED Drivers 1-3.** These pins drive LED indicators for Port 3. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
K16, K17, J17	180 181 182	LED4_1_L LED4_2_L LED4_3_L	OD, TS, SL, IP	**Port 4 LED Drivers 1-3.** These pins drive LED indicators for Port 4. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. The LED outputs are three-stated in H/W Power-Down mode and during H/W reset.

Table 33 LED Signal Descriptions – BGA23 (Sheet 2 of 2)

Ball/Pin Designation		Symbol	Type[1]	Signal Description[2,3]
BGA23	PQFP			
J15, J16, H17	185 186 187	LED5_1_L LED5_2_L LED5_3_L	OD, TS, SL, IP	**Port 5 LED Drivers 1-3.** These pins drive LED indicators for Port 5. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
H15, H16, G17	189 190 191	LED6_1_L LED6_2_L LED6_3_L	OD, TS, SL, IP	**Port 6 LED Drivers 1-3.** These pins drive LED indicators for Port 6. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
G15, F17, F16	192 193 194	LED7_1_L LED7_2_L LED7_3_L	OD, TS, SL, IP	**Port 7 LED Drivers 1-3.** These pins drive LED indicators for Port 7. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. The IP/ID resistors are disabled during H/W Power-Down mode. If a pin is an output or an I/O, the IP/ID resistors are also disabled when the output is enabled.
3. The LED outputs are three-stated in H/W Power-Down mode and during H/W reset.

Table 34 Power Supply Signal Descriptions – BGA23 (Sheet 1 of 2)

Ball/Pin Designation		Symbol	Type	Signal Description
BGA23	PQFP			
F5, G13, J14, J5	65, 78, 184, 196	VCCD	–	**Digital Power Supply - Core.** +2.5 V supply for core digital circuits.
A2, A8, C1, C11, D14	18, 29, 47, 56, 208	VCCIO	–	**Digital Power Supply - I/O Ring.** +2.5/3.3 V supply for digital I/O circuits. The digital input circuits running off of this rail, having a TTL-level threshold and over-voltage protection, may be interfaced with 3.3/5.0 V, when the IO supply is 3.3 V, and 2.5/3.3/5.0 V when 2.5 V.
L5, L13	98, 164	VCCPECL	–	**Digital Power Supply - PECL Signal Detect Inputs.** +2.5/3.3 V supply for PECL Signal Detect input circuits. If Fiber Mode is not used (that is, G_FX/TP_L is pulled Low), the VCCPECL pins may be tied to GNDPECL to save power.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 34 Power Supply Signal Descriptions – BGA23 (Sheet 2 of 2)

Ball/Pin Designation		Symbol	Type	Signal Description
BGA23	PQFP			
N13, P4, P7, P8, P9, P10, P11, P12	103, 116, 117, 130, 131, 144, 145, 158	VCCR	–	**Analog Power Supply - Receive.** +2.5 V supply for all analog receive circuits.
N6, N7, N9, N11, N12	109, 123, 138, 152	VCCT	–	**Analog Power Supply - Transmit.** +2.5 V supply for all analog transmit circuits.
A1, A9, B3, B7, C5, C13, C17, D1, D3, D6, D10, D15, E5, E7, E9, E11, E13, E17, F13, H8, H9, H10, J8, J9, J10, K8, K9, K10	66, 79, 183, 195	GNDD	–	**Digital Ground.** Ground return for core digital supplies (VCCD). All ground pins can be tied together using a single ground plane.
–	9, 19, 30, 38, 48, 57, 74, 188, 199, 207	GNDIO	–	**Digital GND - I/O Ring.** Ground return for digital I/O circuits (VCCIO).
M5, M13	99, 163	GNDPECL	–	**Digital GND - PECL Signal Detect Inputs.** Ground return for PECL Signal Detect input circuits.
P5, P6, P13, R7, R9, R11, R13, U8	106, 112, 120, 126, 135, 141, 149, 155	GNDR	–	**Analog Ground - Receive.** Ground return for receive analog supply. All ground pins can be tied together using a single ground plane.
P14, R1, R3, R5, R15, R17, T17, U2, U4, U6, U10, U12, U14, U16, U17	113, 127, 134, 148	GNDT	–	**Analog Ground - Transmit.** Ground return for transmit analog supply. All ground pins can be tied together using a single ground plane.
K14	179	SGND	–	**Substrate Ground.** Ground for chip substrate. All ground pins can be tied together using a single ground plane.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 35 Unused/Reserved Pins – BGA23

Pin/Ball Designation		Symbol	Type[1]	Signal Description
BGA23	PQFP			
RMII - No Connection				
F15, G2, G5, G14, G16, H4, H14, J2, J13, K4, K15	NC	NC	–	No Connection.
SMII - No Connection				
A4, A5, A7, A14, A16, B1, B2, B4, B8, B9, B11, B12, B15, B16, B17, C4, C6, C7, C8, C10, C12, C14, D4, D11, D12, D16, D17, E3, E4, E15, F4, F14, F15, G2, G5, G14, G16, H4, H14, J2, J13, K4, K15	NC	NC	–	No Connection
SS-SMII - No Connection				
A3, A4, A5, A7, A13, A14, A16, B2, B6, B8, B14, B16, C2, C4, C6, C10, C14, C15, D4, D9, D11, D12, D16, E15, E16, F4, F15, G2, G5, G14, G16, H4, H14, J2, J13, K4, K15	NC	NC	–	No Connection

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 36 Receive FIFO Depth Configurations

FIFOSEL1	FIFOSEL0	Register 18.15 Value	Register 18.14 Value
0	0	1	0
0	1	1	1
1	0	0	0
1	1	0	1

3.5 BGA15 Ball Assignments

The following figure and tables provide the BGA15 ball locations and signal names arranged in alphanumeric order as follows:

- Figure 6, *196-Ball BGA15 Assignments (Top View)*
- Table 37, *LXT9785MBC BGA15 Ball List in Alphanumeric Order by Signal Name*, on page 98
- Table 38, *LXT9785MBC BGA15 Ball List in Alphanumeric Order by Ball Location (SMII/SS-SMII)*, on page 102

Figure 6 196-Ball BGA15 Assignments (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A
B	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B
C	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C
D	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D
E	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E
F	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F
G	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G
H	H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H
J	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J
K	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K
L	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L
M	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M
N	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N
P	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

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3.5.1 BGA15 Ball List

The following tables provide the RMII BGA23 ball locations and signal names arranged in alphanumeric order as follows:

- Table 37, *LXT9785MBC BGA15 Ball List in Alphanumeric Order by Signal Name*, on page 98
- Table 38, *LXT9785MBC BGA15 Ball List in Alphanumeric Order by Ball Location (SMII/SS-SMII)*, on page 102

Table 37 LXT9785MBC BGA15 Ball List in Alphanumeric Order by Signal Name

Signal Name	Ball	Type	Reference for Full Description
ADD_3	P10	I, ST, ID	Table 39
ADD_4	N10	I, ST, ID	Table 39
AMDIX_EN	K8	I, ST, IP	Table 39
AVCC	D12	–	Table 39
AVCC	E12	–	Table 39
AVCC	F12	–	Table 39
AVCC	G12	–	Table 39
AVCC	H12	–	Table 39
AVCC	J12	–	Table 39
AVCC	K12	–	Table 39
AVCC	L12	–	Table 39
AVSS	E11	–	Table 39
AVSS	F9	–	Table 39
AVSS	F10	–	Table 39
AVSS	F11	–	Table 39
AVSS	G9	–	Table 39
AVSS	G10	–	Table 39
AVSS	G11	–	Table 39
AVSS	H9	–	Table 39
AVSS	H10	–	Table 39
AVSS	H11	–	Table 39
AVSS	J9	–	Table 39
AVSS	J10	–	Table 39
AVSS	J11	–	Table 39
AVSS	K11	–	Table 39
AVSS	L11	–	Table 39
CFG_1	M10	I, ST, ID	Table 39
CFG_2	L9	I, ST, ID	Table 39
CFG_3	M9	I, ST, ID	Table 39
FIFOSEL0	F1	I, ID	Table 39
FIFOSEL1	C1	I, ID	Table 39
GNDD	A1	–	Table 39
GNDD	A2	–	Table 39
GNDD	A3	–	Table 39
GNDD	B1	–	Table 39
GNDD	B2	–	Table 39
GNDD	B5	–	Table 39
GNDD	B10	–	Table 39
GNDD	D9	–	Table 39
GNDD	D11	–	Table 39
GNDD	E5	–	Table 39
GNDD	E6	–	Table 39
GNDD	E9	–	Table 39
GNDD	E10	–	Table 39
GNDD	F5	–	Table 39
GNDD	F6	–	Table 39
GNDD	F7	–	Table 39
GNDD	F8	–	Table 39
GNDD	G4	–	Table 39
GNDD	G6	–	Table 39
GNDD	G7	–	Table 39
GNDD	G8	–	Table 39
GNDD	H6	–	Table 39
GNDD	H7	–	Table 39
GNDD	H8	–	Table 39
GNDD	J5	–	Table 39

Signal Name	Ball	Type	Reference for Full Description
GNDD	J6	–	Table 39
GNDD	J7	–	Table 39
GNDD	J8	–	Table 39
GNDD	K5	–	Table 39
GNDD	K6	–	Table 39
GNDD	K9	–	Table 39
GNDD	K10	–	Table 39
GNDD	L2	–	Table 39
GNDD	N1	–	Table 39
GNDD	N11	–	Table 39
GNDD	P1	–	Table 39
GNDD	P11	–	Table 39
LED0_1_L	N9	OD, TS, SL, IP	Table 39
LED0_2_L	P9	OD, TS, SL, IP	Table 39
LED0_3_L	M8	OD, TS, SL, IP	Table 39
LED1_1_L	N8	OD, TS, SL, IP	Table 39
LED1_2_L	P8	OD, TS, SL, IP	Table 39
LED1_3_L	L8	OD, TS, SL, IP	Table 39
LED2_1_L	P7	OD, TS, SL, IP	Table 39
LED2_2_L	N7	OD, TS, SL, IP	Table 39
LED2_3_L	M7	OD, TS, SL, IP	Table 39
LED3_1_L	P6	OD, TS, SL, IP	Table 39
LED3_2_L	N6	OD, TS, SL, IP	Table 39
LED3_3_L	M6	OD, TS, SL, IP	Table 39
LED4_1_L	B9	OD, TS, SL, IP	Table 39
LED4_2_L	A9	OD, TS, SL, IP	Table 39
LED4_3_L	D8	OD, TS, SL, IP	Table 39
LED5_1_L	B8	OD, TS, SL, IP	Table 39
LED5_2_L	A8	OD, TS, SL, IP	Table 39
LED5_3_L	C7	OD, TS, SL, IP	Table 39
LED6_1_L	A7	OD, TS, SL, IP	Table 39
LED6_2_L	B7	OD, TS, SL, IP	Table 39
LED6_3_L	D6	OD, TS, SL, IP	Table 39
LED7_1_L	B6	OD, TS, SL, IP	Table 39
LED7_2_L	A6	OD, TS, SL, IP	Table 39
LED7_3_L	D5	OD, TS, SL, IP	Table 39
LINKHOLD	B3	ID	Table 39
MDC	P4	I, ST, ID	Table 39
MDINT_L	P5	OD, TS, SL, IP	Table 39
MDIO	N5	IO, TS, SL, IP	Table 39
ModeSel_0	C9	I, ST, ID	Table 39
ModeSel_1	E8	I, ST, ID	Table 39
NC	C4	–	Table 39

Signal Name	Ball	Type	Reference for Full Description
NC	D1	–	Table 39
NC	D2	–	Table 39
NC	D10	–	Table 39
NC	E4	–	Table 39
NC	E7	–	Table 39
NC	G2	–	Table 39
NC	G5	–	Table 39
NC	H1	–	Table 39
NC	H5	–	Table 39
NC	J4	–	Table 39
NC	K4	–	Table 39
NC	K7	–	Table 39
NC	L1	–	Table 39
NC	L6	–	Table 39
NC	L10	–	Table 39
NC	M4	–	Table 39
NC	M5	–	Table 39
NC	P2	–	Table 39
NC	P3	–	Table 39
REFCLK0	L4	I	Table 39
REFCLK1	C3	I	Table 39
RESET_L	C10	I, ST, IP	Table 39
RXCLK	G1	O, TS, ID	Table 39
RxData0_S	N3	O, TS	Table 39
RxData0_SS	M3	O, TS, ID	Table 39
RxData1_S	M2	O, TS	Table 39
RxData1_SS	M1	O, TS, ID	Table 39
RxData2_S	K2	O, TS	Table 39
RxData2_SS	J2	O, TS, ID	Table 39
RxData3_S	H3	O, TS	Table 39
RxData3_SS	H2	O, TS, ID	Table 39
RxData4_S	F2	O, TS	Table 39
RxData4_SS	F3	O, TS, ID	Table 39
RxData5_S	E3	O, TS	Table 39

Signal Name	Ball	Type	Reference for Full Description
RxData5_SS	C2	O, TS	Table 39
RxData6_S	B4	O, TS	Table 39
RxData6_SS	A4	O, TS, ID	Table 39
RxData7_S	C5	O, TS	Table 39
RxData7_SS	C6	O, TS, ID	Table 39
RxSYNC	E1	O, TS, ID	Table 39
SGND	C8	–	Table 39
SYNC/ TXSYNC	K1	I, ID	Table 39
TCK	A11	I, ST, ID	Table 39
TDI	C12	I, ST, IP	Table 39
TDO	C11	O, TS	Table 39
TMS	B11	I, ST, IP	Table 39
TPIN0	N12	AI/AO	Table 39
TPIN1	M13	AI/AO	Table 39
TPIN2	L14	AI/AO	Table 39
TPIN3	H13	AI/AO	Table 39
TPIN4	G13	AI/AO	Table 39
TPIN5	D14	AI/AO	Table 39
TPIN6	C13	AI/AO	Table 39
TPIN7	B12	AI/AO	Table 39
TPIP0	P12	AI/AO	Table 39
TPIP1	M14	AI/AO	Table 39
TPIP2	L13	AI/AO	Table 39
TPIP3	H14	AI/AO	Table 39
TPIP4	G14	AI/AO	Table 39
TPIP5	D13	AI/AO	Table 39
TPIP6	C14	AI/AO	Table 39
TPIP7	A12	AI/AO	Table 39
TPON0	N13	AO/AI	Table 39
TPON1	P14	AO/AI	Table 39
TPON2	K14	AO/AI	Table 39
TPON3	J13	AO/AI	Table 39
TPON4	F13	AO/AI	Table 39

Signal Name	Ball	Type	Reference for Full Description
TPON5	E14	AO/AI	Table 39
TPON6	A14	AO/AI	Table 39
TPON7	B13	AO/AI	Table 39
TPOP0	P13	AO/AI	Table 39
TPOP1	N14	AO/AI	Table 39
TPOP2	K13	AO/AI	Table 39
TPOP3	J14	AO/AI	Table 39
TPOP4	F14	AO, AI	Table 39
TPOP5	E13	AO/AI	Table 39
TPOP6	B14	AO/AI	Table 39
TPOP7	A13	AO/AI	Table 39
TRST_L	A10	I, ST, IP	Table 39
TXCLK	J3	I, ID	Table 39
TxData0	N4	I, ID	Table 39
TxData1	N2	I, ID	Table 39
TxData2	K3	I, ID	Table 39
TxData3	J1	I, ID	Table 39
TxData4	G3	I, ID	Table 39
TxData5	E2	I, ID	Table 39
TxData6	D3	I, ID	Table 39
TxData7	A5	I, ID	Table 39
TXSLEW_0	M11	I, ST, ID	Table 39
TXSLEW_1	M12	I,ST, ID	Table 39
VCCD	D7	–	Table 39
VCCD	L7	–	Table 39
VCCIO	D4	–	Table 39
VCCIO	F4	–	Table 39
VCCIO	H4	–	Table 39
VCCIO	L3	–	Table 39
VCCIO	L5	–	Table 39

Table 38 shows the ball locations and signal names arranged in order by ball location.

Table 38 LXT9785MBC BGA15 Ball List in Alphanumeric Order by Ball Location (SMII/SS-SMII)

Ball	Signal Name	Type	Reference for Full Description
A1	GNDD	–	Table 39
A2	GNDD	–	Table 39
A3	GNDD	–	Table 39
A4	RxData6_SS	O, TS, ID	Table 39
A5	TxData7	I, ID	Table 39
A6	LED7_2_L	OD, TS, SL, IP	Table 39
A7	LED6_1_L	OD, TS, SL, IP	Table 39
A8	LED5_2_L	OD, TS, SL, IP	Table 39
A9	LED4_2_L	OD, TS, SL, IP	Table 39
A10	TRST_L	I, ST, IP	Table 39
A11	TCK	I, ST, ID	Table 39
A12	TPIP7	AI/AO	Table 39
A13	TPOP7	AO/AI	Table 39
A14	TPON6	AO/AI	Table 39
B1	GNDD	–	Table 39
B2	GNDD	–	Table 39
B3	LINKHOLD	ID	Table 39
B4	RxData6_S	O, TS	Table 39
B5	GNDD	–	Table 39
B6	LED7_1_L	OD, TS, SL, IP	Table 39
B7	LED6_2_L	OD, TS, SL, IP	Table 39
B8	LED5_1_L	OD, TS, SL, IP	Table 39
B9	LED4_1_L	OD, TS, SL, IP	Table 39
B10	GNDD	–	Table 39
B11	TMS	I, ST, IP	Table 39
B12	TPIN7	AI/AO	Table 39
B13	TPON7	AO/AI	Table 39
B14	TPOP6	AO/AI	Table 39
C1	FIFOSEL1	I, ID	Table 39
C2	RxData5_SS	O, TS, ID	Table 39
C3	REFCLK1	I	Table 39
C4	NC	–	Table 39
C5	RxData7_S	O, TS	Table 39
C6	RxData7_SS	O, TS, ID	Table 39
C7	LED5_3_L	OD, TS, SL, IP	Table 39
C8	SGND	–	Table 39
C9	ModeSel_0	I, ST, ID	Table 39
C10	RESET_L	I, ST, IP	Table 39
C11	TDO	O, TS	Table 39
C12	TDI	I, ST, IP	Table 39
C13	TPIN6	AI/AO	Table 39
C14	TPIP6	AI/AO	Table 39
D1	NC	–	Table 39
D2	NC	–	Table 39
D3	TxData6	I, ID	Table 39
D4	VCCIO	–	Table 39
D5	LED7_3_L	OD, TS, SL, IP	Table 39
D6	LED6_3_L	OD, TS, SL, IP	Table 39
D7	VCCD	–	Table 39
D8	LED4_3_L	OD, TS, SL, IP	Table 39
D9	GNDD	–	Table 39

Ball	Signal Name	Type	Reference for Full Description
D10	NC	–	Table 39
D11	GNDD	–	Table 39
D12	AVCC	–	Table 39
D13	TPIP5	AI/AO	Table 39
D14	TPIN5	AI/AO	Table 39
E1	RxSYNC	O, TS, ID	Table 39
E2	TxData5	I, ID	Table 39
E3	RxData5_S	O, TS	Table 39
E4	NC	–	Table 39
E5	GNDD	–	Table 39
E6	GNDD	–	Table 39
E7	NC	–	Table 39
E8	ModeSel_1	I, ST, ID	Table 39
E9	GNDD	–	Table 39
E10	GNDD	–	Table 39
E11	AVSS	–	Table 39
E12	AVCC	–	Table 39
E13	TPOP5	AO/AI	Table 39
E14	TPON5	AO/AI	Table 39
F1	FIFOSEL0	I, ID	Table 39
F2	RxData4_S	O, TS	Table 39
F3	RxData4_SS	O, TS, ID	Table 39
F4	VCCIO	–	Table 39
F5	GNDD	–	Table 39
F6	GNDD	–	Table 39
F7	GNDD	–	Table 39
F8	GNDD	–	Table 39
F9	AVSS	–	Table 39
F10	AVSS	–	Table 39
F11	AVSS	–	Table 39
F12	AVCC	–	Table 39
F13	TPON4	AO/AI	Table 39
F14	TPOP4	AO, AI	Table 39
G1	RXCLK	O, TS, ID	Table 39
G2	NC	–	Table 39

Ball	Signal Name	Type	Reference for Full Description
G3	TxData4	I, ID	Table 39
G4	GNDD	–	Table 39
G5	NC	–	Table 39
G6	GNDD	–	Table 39
G7	GNDD	–	Table 39
G8	GNDD	–	Table 39
G9	AVSS	–	Table 39
G10	AVSS	–	Table 39
G11	AVSS	–	Table 39
G12	AVCC	–	Table 39
G13	TPIN4	AI/AO	Table 39
G14	TPIP4	AI/AO	Table 39
H1	NC	–	Table 39
H2	RxData3_SS	O, TS, ID	Table 39
H3	RxData3_S	O, TS	Table 39
H4	VCCIO	–	Table 39
H5	NC	–	Table 39
H6	GNDD	–	Table 39
H7	GNDD	–	Table 39
H8	GNDD	–	Table 39
H9	AVSS	–	Table 39
H10	AVSS	–	Table 39
H11	AVSS	–	Table 39
H12	AVCC	–	Table 39
H13	TPIN3	AI/AO	Table 39
H14	TPIP3	AI/AO	Table 39
J1	TxData3	I, ID	Table 39
J2	RxData2_SS	O, TS, ID	Table 39
J3	TXCLK	I, ID	Table 39
J4	NC	–	Table 39
J5	GNDD	–	Table 39
J6	GNDD	–	Table 39
J7	GNDD	–	Table 39
J8	GNDD	–	Table 39
J9	AVSS	–	Table 39
J10	AVSS	–	Table 39
J11	AVSS	–	Table 39

Ball	Signal Name	Type	Reference for Full Description
J12	AVCC	–	Table 39
J13	TPON3	AO/AI	Table 39
J14	TPOP3	AO/AI	Table 39
K1	SYNC/ TXSYNC	I, ID	Table 39
K2	RxData2_S	O, TS	Table 39
K3	TxData2	I, ID	Table 39
K4	NC	–	Table 39
K5	GNDD	–	Table 39
K6	GNDD	–	Table 39
K7	NC	–	Table 39
K8	AMDIX_EN	I, ST, IP	Table 39
K9	GNDD	–	Table 39
K10	GNDD	–	Table 39
K11	AVSS	–	Table 39
K12	AVCC	–	Table 39
K13	TPOP2	AO/AI	Table 39
K14	TPON2	AO/AI	Table 39
L1	NC	–	Table 39
L2	GNDD	–	Table 39
L3	VCCIO	–	Table 39
L4	REFCLK0	I	Table 39
L5	VCCIO	–	Table 39
L6	NC	–	Table 39
L7	VCCD	–	Table 39
L8	LED1_3_L	OD, TS, SL, IP	Table 39
L9	CFG_2	I, ST, ID	Table 39
L10	NC	–	Table 39
L11	AVSS	–	Table 39
L12	AVCC	–	Table 39
L13	TPIP2	AI/AO	Table 39
L14	TPIN2	AI/AO	Table 39
M1	RxData1_SS	O, TS, ID	Table 39
M2	RxData1_S	O, TS	Table 39
M3	RxData0_SS	O, TS, ID	Table 39

Ball	Signal Name	Type	Reference for Full Description
M4	NC	–	Table 39
M5	NC	–	Table 39
M6	LED3_3_L	OD, TS, SL, IP	Table 39
M7	LED2_3_L	OD, TS, SL, IP	Table 39
M8	LED0_3_L	OD, TS, SL, IP	Table 39
M9	CFG_3	I, ST, ID	Table 39
M10	CFG_1	I, ST, ID	Table 39
M11	TXSLEW_0	I, ST, ID	Table 39
M12	TXSLEW_1	I,ST, ID	Table 39
M13	TPIN1	AI/AO	Table 39
M14	TPIP1	AI/AO	Table 39
N1	GNDD	–	Table 39
N2	TxData1	I, ID	Table 39
N3	RxData0_S	O, TS	Table 39
N4	TxData0	I, ID	Table 39
N5	MDIO	IO, TS, SL, IP	Table 39
N6	LED3_2_L	OD, TS, SL, IP	Table 39
N7	LED2_2_L	OD, TS, SL, IP	Table 39
N8	LED1_1_L	OD, TS, SL, IP	Table 39
N9	LED0_1_L	OD, TS, SL, IP	Table 39
N10	ADD_4	I, ST, ID	Table 39
N11	GNDD	–	Table 39
N12	TPIN0	AI/AO	Table 39
N13	TPON0	AO/AI	Table 39
N14	TPOP1	AO/AI	Table 39

Ball	Signal Name	Type	Reference for Full Description
P1	GNDD	–	Table 39
P2	NC	–	Table 39
P3	NC	–	Table 39
P4	MDC	I, ST, ID	Table 39
P5	MDINT_L	OD, TS, SL, IP	Table 39
P6	LED3_1_L	OD, TS, SL, IP	Table 39
P7	LED2_1_L	OD, TS, SL, IP	Table 39
P8	LED1_2_L	OD, TS, SL, IP	Table 39
P9	LED0_2_L	OD, TS, SL, IP	Table 39
P10	ADD_3	I, ST, ID	Table 39
P11	GNDD	–	Table 39
P12	TPIP0	AI/AO	Table 39
P13	TPOP0	AO/AI	Table 39
P14	TPON1	AO/AI	Table 39

3.6 BGA15 Signal Descriptions

3.6.1 Signal Name Conventions

Signal names may contain either a port designation or a serial designation, or a combination of the two designations. Signal naming conventions are as follows:

- **Port Number Only.** Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by the Port Designation. For example, Transmit Enable signals would be identified as TxEN0, TxEN1, and TxEN2.
- **Serial Number Only.** A set of signals which are not tied to any specific port are designated by the Signal Mnemonic, followed by an underscore and a serial designation. For example, a set of three Global Configuration signals would be identified as CFG_1, CFG_2, and CFG_3.
- **Port and Serial Number.** In cases where each port is assigned a set of multiple signals, each signal is designated in the following order: Signal Mnemonic, Port Designation, an underscore, and the serial designation. For example, a set of three Port Configuration signals would be identified as RxData0_0 and RxData0_1, RxData1_0 and RxData1_1, and RxData2_0 and RxData2_1.

3.6.2 Signal Descriptions – SMII and SS-SMII Configurations

Table 39 provides the BGA15 signal descriptions.

Table 39 BGA15 Signal Descriptions (Sheet 1 of 7)

Symbol	BGA15 Ball Designation	Type	Signal Description
SMII/SS-SMII Common Signal Descriptions			
TxData0 TxData1 TxData2 TxData3 TxData4 TxData5 TxData6 TxData7	N4, N2, K3, J1, G3, E2, D3, A5	I, ID	**Transmit Data - Ports 0-7.** These serial input streams provide data to be transmitted to the network. The LXT9785/LXT9785E clocks the data in synchronously to REFCLK.
REFCLK1 REFCLK0	C3 L4	I	**Reference Clock.** The LXT9785/LXT9785E always requires a 125 MHz reference clock input. Refer to Section 4.4.2, *Clock/SYNC Requirements*, on page 122 for detailed clock requirements.
SMII Specific Signal Descriptions			
SYNC	K1	I, ID	**SMII Synchronization.** The MAC must generate a SYNC pulse every 10 REFCLK cycles to synchronize the SMII.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).

Table 39 BGA15 Signal Descriptions (Sheet 2 of 7)

Symbol	BGA15 Ball Designation	Type	Signal Description
RxData0_S RxData1_S RxData2_S RxData3_S RxData4_S RxData5_S RxData6_S RxData7_S	N3, M2, K2, H3, F2, E3, B4, C5	O, TS	**Receive Data - Ports 0-7**. These serial output streams provide data received from the network. The LXT9785/LXT9785E drives the data out synchronously to REFCLK.
SS-SMII Specific Signal Descriptions			
TxSYNC	K1	I, ID	**SS-SMII Transmit Synchronization.** The MAC must generate a TxSYNC pulse every 10 TxCLK cycles to mark the start of TxData segments.
RxSYNC	E1	O, TS, ID	**SS-SMII Receive Synchronization.** The LXT9785/LXT9785E generates these pulses every 10 RxCLK cycles to mark the start of RxData segments for the MAC.
TxCLK	J3	I, ID	**SS-SMII Transmit Clock.** The MAC sources this 125 MHz clock as the timing reference for TxData and TxSYNC.
RxCLK	G1	O, TS, ID	**SS-SMII Receive Clock.** The LXT9785/LXT9785E generates these clocks, based on REFCLK, to provide a timing reference for RxData and RxSYNC to the MAC.
RxData0_SS RxData1_SS RxData2_SS RxData3_SS RxData4_SS RxData5_SS RxData6_SS RxData7_SS	M3, M1, J2, H2, F3, C2, A4, C6	O, TS, ID	**Receive Data - Ports 0-7.** These serial output streams provide data received from the network. The LXT9785/LXT9785E drives the data out synchronously to REFCLK.
MDIO Control Interface Signal Descriptions			
MDIO	N5	I/O, TS, SL, IP	**Management Data Input/Output.** Bidirectional serial data channel for communication between the PHY and MAC or switch ASIC. Refer to Figure 21 on page 136.
MDINT_L	P5	OD, TS, SL, IP	**Management Data Interrupt.** When Register bit 18.1 = 1, an active Low output on this Pin indicates status change. Refer to Figure 21 on page 136.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).

Table 39 BGA15 Signal Descriptions (Sheet 3 of 7)

Symbol	BGA15 Ball Designation	Type	Signal Description
MDC	P4	I, ST, ID	**Management Data Clock.** Clock for the MDIO serial data channel. Maximum frequency is 20 MHz. Only MDC0 is used when 1x8 port sectionalization is selected. In 2x4 port sectionalization mode, MDC0 clocks ports 0-3 register accesses and MDC1 clocks ports 4-7 register accesses. Refer to Figure 21 on page 136.
Network Interface Signal Description			
TPOP0, TPON0 TPOP1, TPON1 TPOP2, TPON2 TPOP3, TPON3 TPOP4, TPON4 TPOP5, TPON5 TPOP6, TPON6 TPOP7, TPON7	P13, N13, N14, P14, K13, K14, J14, J13, F14, F13, E13, E14, B14, A14, A13, B13	AO/AI	**Twisted-Pair Outputs[2], Positive & Negative, Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPO pins drive 802.3 compliant pulses onto the line.
TPIP0, TPIN0 TPIP1, TPIN1 TPIP2, TPIN2 TPIP3, TPIN3 TPIP4, TPIN4 TPIP5, TPIN5 TPIP6, TPIN6 TPIP7, TPIN7	P12, N12, M14, M13, L13, L14, H14, H13, G14, G13, D13, D14, C14, C13, A12, B12	AI/AO	**Twisted-Pair Inputs[3], Positive & Negative, Ports 0-7.** During 100BASE-TX or 10BASE-T operation, TPI pins receive differential 100BASE-TX or 10BASE-T signals from the line.
JTAG Test Signal Description			
TDI	C12	I, ST, IP	**Test Data Input.** Test data sampled with respect to the rising edge of TCK.
TDO	C11	O, TS	**Test Data Output.** Test data driven with respect to the falling edge of TCK.
TMS	B11	I, ST, IP	**Test Mode Select.**
TCK	A11	I, ST, ID	**Test Clock.** Clock input for JTAG test.
TRST_L	A10	I, ST, IP	**Test Reset.** Reset input for JTAG test.
Miscellaneous Signal Description			

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).

Table 39 BGA15 Signal Descriptions (Sheet 4 of 7)

<table>
<tr><th>Symbol</th><th>BGA15 Ball Designation</th><th>Type</th><th>Signal Description</th></tr>
<tr><td>TxSLEW_0
TxSLEW_1</td><td>M11,
M12</td><td>I, ST, ID</td><td>Tx Output Slew Controls 0 and 1 Defaults.
These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 27.11:10 for all ports. These register bits can be read and overwritten after startup / reset.
These pins select the TX output slew rate for all ports (rise and fall time) as follows:
<table>
<tr><th>TxSLEW_1</th><th>TxSLEW_0</th><th>Slew Rate (Rise and Fall Time)</th></tr>
<tr><td>0</td><td>0</td><td>3.3 ns</td></tr>
<tr><td>0</td><td>1</td><td>3.6 ns</td></tr>
<tr><td>1</td><td>0</td><td>3.9 ns</td></tr>
<tr><td>1</td><td>1</td><td>4.2 ns</td></tr>
</table></td></tr>
<tr><td>RESET_L</td><td>C10</td><td>I, ST, IP</td><td>Reset.
This active low input is ORed with the control register Reset Register bit 0.15. When held Low, all outputs are forced to inactive state.
Pin is not on JTAG chain.</td></tr>
<tr><td>ADD_4
ADD_3</td><td>N10,
P10</td><td>I, ST, ID</td><td>Address <4:3>.
Sets base address to one of the following four possible addresses:
• 00000
• 01000
• 10000
• 11000
Each port adds its port number (starting with 0) to this address to determine its PHY address.
Port 0 Address = Base
Port 1 Address = Base + 1
Port 2 Address = Base + 2
Port 3 Address = Base + 3
Port 4 Address = Base + 4
Port 5 Address = Base + 5
Port 6 Address = Base + 6
Port 7 Address = Base + 7</td></tr>
<tr><td>MODESEL_1
MODESEL_0</td><td>E8
C9,</td><td>I, ST, ID</td><td>Mode Select[1:0].
00 = Reserved
01 = SMII
10 = SS-SMII
11 = Reserved
All ports are configured the same. Interfaces cannot be mixed and must be all SMII or SS-SMII.</td></tr>
<tr><td colspan="4">1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).</td></tr>
</table>

Table 39 BGA15 Signal Descriptions (Sheet 5 of 7)

Symbol	BGA15 Ball Designation	Type	Signal Description
AMDIX_EN	K8	I, ST, IP	**Auto MDI/MDIX Enable Default.** This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 27.9 for all ports. These register bits can be read and overwritten after startup / reset. Refer to Table 40 on page 116. When active (High), automatic MDI crossover (MDIX) (regardless of segmentation) is selected for all ports. When inactive (Low) MDIX is selected according to the MDIX pin.
CFG_1 CFG_2 CFG_3	M10, L9, M9	I, ST, ID	**Global Port Configuration Defaults 1-3.** These pins are read at startup or reset. Their value at that time is used to set the default state of register bits shown in Table 42, *Global Hardware Configuration Settings*, on page 126 for all ports. These register bits can be read and overwritten after startup / reset. When operating in Hardware Control Mode, these pins provide configuration control options for all the ports (refer to page 126 for details).
FIFOSEL1 FIFOSEL0	C1, F1	I, ID, ST	**FIFO Select <1:0>.** These pins are read at startup or reset. Their value at that time is used to set the default state of Register bits 18.15:14 for all ports. These register bits can be read and overwritten after startup/reset. These pins are shared with RMII-RxER<5:4>. An external pull-up resistor (see applications section for value) can be used to set FIFO Select<1:0> to active while RxER<5:4> are three-stated during hardware reset. If no pull-up is used, the default FIFO select state is set via the internal pull-down resistors. See Table 36, *Receive FIFO Depth Configurations*, on page 96.
LINKHOLD	B3	I, ID, ST	**LINKHOLD Defaul**t. This pin is read at startup or reset. Its value at that time is used to set the default state of Register bit 0.11 for all ports. This register bit can be read and overwritten after startup / reset. When High, the LXT9785/ LXT9785E powers down all ports. This pin is shared with RMII-RxER6. An external pull-up resistor (see applications section for value) can be used to set LINKHOLD active while RxER6 is three-stated during H/W reset. If no pull-up is used, the default LINKHOLD state is set inactive via the internal pull-down resistor.
LED Signal Descriptions			
LED0_1_L LED0_2_L LED0_3_L	N9 P9 M8	OD, TS, SL, IP	**Port 0 LED Drivers 1-3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).

Table 39 BGA15 Signal Descriptions (Sheet 6 of 7)

Symbol	BGA15 Ball Designation	Type	Signal Description
LED1_1_L LED1_2_L LED1_3_L	N8 P8 L8	OD, TS, SL, IP	**Port 1 LED Drivers 1-3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
LED2_1_L LED2_2_L LED2_3_L	P7 N7 M7	OD, TS, SL, IP	**Port 2 LED Drivers 1-3.** These pins drive LED indicators for Port 2. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
LED3_1_L LED3_2_L LED3_3_L	P6 N6 M6	OD, TS, SL, IP	**Port 3 LED Drivers 1-3.** These pins drive LED indicators for Port 3. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
LED4_1_L LED4_2_L LED4_3_L	B9 A9 D8	OD, TS, SL, IP	**Port 4 LED Drivers 1-3.** These pins drive LED indicators for Port 4. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
LED5_1_L LED5_2_L LED5_3_L	B8 A8 C7	OD, TS, SL, IP	**Port 5 LED Drivers 1-3.** These pins drive LED indicators for Port 5. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
LED6_1_L LED6_2_L LED6_3_L	A7 B7 D6	OD, TS, SL, IP	**Port 6 LED Drivers 1-3.** These pins drive LED indicators for Port 6. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
LED7_1_L LED7_2_L LED7_3_L	B6 A6 D5	OD, TS, SL, IP	**Port 7 LED Drivers 1-3.** These pins drive LED indicators for Port 7. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204 for details).
Power Supply Signal Descriptions			
AVCC	D12, E12, F12, G12, H12, J12, K12, L12,	–	**Analog Power Supply.** +2.5 V supply for analog circuits.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).

Table 39 BGA15 Signal Descriptions (Sheet 7 of 7)

Symbol	BGA15 Ball Designation	Type	Signal Description
AVSS	E11, F9, F10, F11, G9, G10, G11, H9, H10, H11, J9, J10, J11, K11, L11	–	**Analog Ground.** Ground return for analog supply (AVCC). all grounds can be tied together using a single ground plane.
VCCD	D7, L7	–	**Digital Power Supply - Core.** +2.5 V supply for core digital circuits.
VCCIO	D4, F4, H4, L3, L5,	–	**Digital Power Supply - I/O Ring.** +2.5/3.3 V supply for digital I/O circuits. The digital input circuits running off of this rail, having a TTL-level threshold and over-voltage protection, may be interfaced with 3.3/5.0 V, when the IO supply is 3.3 V, and 2.5/3.3/5.0 V when 2.5 V.
GNDD	A1, A2, A3, B1, B2, B5, B10, D9, D11, E5, E6, E9, E10, F5, F6, F7, F8, G4, G6, G7, G8, H6, H7, H8, J5, J6, J7, J8, K5, K6, K9, K10, L2, N1, N11, P1, P11	–	**Digital Ground.** Ground return for core digital supplies (VCCD). All ground pins can be tied together using a single ground plane.
SGND	C8	–	**Substrate Ground.** Ground for chip substrate. All ground pins can be tied together using a single ground plane.
Unused/Reserved Balls			
NC	C4, D1, D2, D10, E4, E7, G2, G5, H1, H5, J4, K4, K7, L1, L6, L10, M4, M5, P2, P3	–	No Connection.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
2. Switched to TPIP/N Inputs when MDIX is not active (twisted-pair, non-crossover MDI mode).
3. Switched to TPOP/N Outputs when MDIX is not active (twisted-pair, non-crossover MDI mode).

4.0 Functional Description

4.1 Introduction

The Cortina Systems® LXT9785/LXT9785E is an 8-port Fast Ethernet 10/100 PHY transceiver that supports 10 Mbps and 100 Mbps networks, complying with all applicable requirements of IEEE 802.3 standards. The device incorporates a Serial Media Independent Interface (SMII), Source Synchronous-Serial Media Independent Interface (SS-SMII), and a Reduced Serial Independent Interface (RMII) to enable each individual network port to interface with multiple 10/100 MACs. Each port directly drives either a 100BASE-TX line or a 10BASE-T line. The LXT9785/LXT9785E also supports 100BASE-FX operation via an LVPECL interface. The device has a 241-ball BGA, a 208-pin QFP, or a 196-ball BGA package.

The 196-ball BGA package (BGA15) is a reduced feature-set product designated as the LXT9785MBC. The BGA15 package does not support the following features:

- RMII
- Fiber
- Sectionalization
- Hardware control pins:
  - PAUSE
  - MDIX
  - MDDIS
  - PWRDWN
  - Lower three PHY address (out of five PHY address bits)
- Extended temperature

Note: Unless otherwise noted, all information in this document applies to the LXT9785 and LXT9785E.

4.1.1 OSP™ Architecture

The LXT9785/LXT9785E incorporates high-efficiency Optimal Signal Processing™ design techniques, combining the best properties of digital and analog signal processing to produce a truly optimal device.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). The result is improved receiver noise and cross-talk performance.

The OSP architecture also requires substantially less computational logic than traditional DSP-based designs. The result is lower power consumption and reduced logic switching noise generated by DSP engines clocked at speeds up to 125 MHz. The logic switching noise can be a considerable source of EMI when generated from the device's power supplies.

The OSP-based LXT9785/LXT9785E provides improved data recovery, EMI performance and power consumption.

4.1.2 Comprehensive Functionality

The LXT9785/LXT9785E performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT9785/LXT9785E reads its configuration inputs to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/ parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT9785/LXT9785E auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT9785/LXT9785E automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating conditions accordingly.

The LXT9785/LXT9785E provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

4.1.2.1 Sectionalization

The LXT9785/LXT9785E's sectional design allows flexibility with large multiport MACs and ASICs. With the use of the Section pin, the LXT9785/LXT9785E can be configured into a single 8-port or two separate 4-port sections, each with its own MDIO (with separate MDC clock) and MII data (with separate REFCLK/TxCLK/RxCLK clocks) interfaces. See Figure 16, *Typical SMII Quad Sectionalization*, on page 131, Figure 21, *Typical SS-SMII Quad Sectionalization*, on page 136, and Figure 26, *Typical RMII Quad Sectionalization*, on page 140.

Note: The BGA15 package does not support sectionalization.

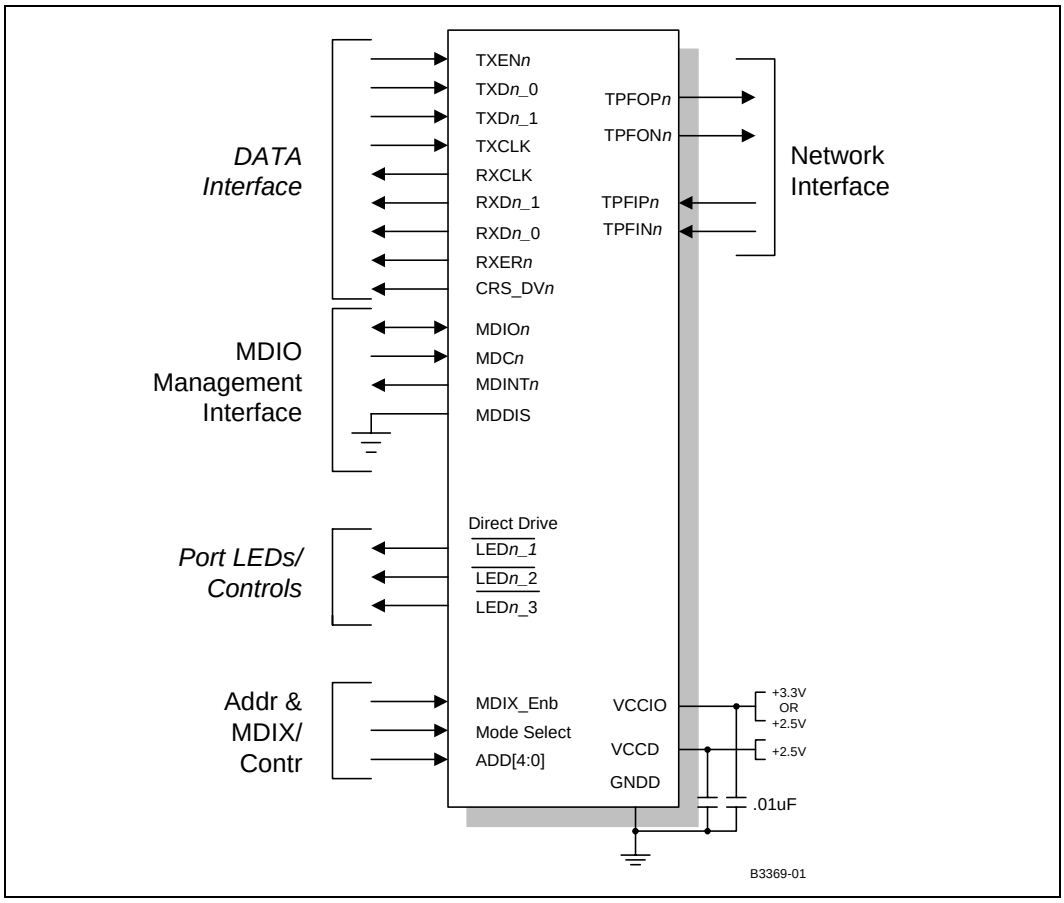
4.2 Interface Descriptions

4.2.1 10/100 Network Interface

The LXT9785/LXT9785E supports 10 Mbps and 100 Mbps (10BASE-T and 100BASE-TX) Ethernet over twisted-pair, or 100 Mbps (100BASE-FX) Ethernet over fiber media. Each network interface port consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair (TP) and fiber. The LXT9785/LXT9785E pinout is designed to interface seamlessly with dual-high stacked RJ-45 connectors. Refer to Table 11, *Network Interface Signal Descriptions – PQFP*, on page 42 for specific pin assignments.

The LXT9785/LXT9785E output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the device generates IEEE 802.3-compliant link pulses or idle code. Input signals are decoded either as a 100BASE-TX, 100BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/ parallel detection or manual control is used to determine the speed of this interface.

Figure 7 Interface Signals



4.2.1.1 Twisted-Pair Interface

The LXT9785/LXT9785E supports either 100BASE-TX or 10BASE-T connections over 100 Ω, Category 5, Unshielded Twisted-Pair (UTP). Only a transformer, RJ-45, and bypass capacitors are required to complete this interface. Using waveshaping technology, the transmitter shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 13, *Miscellaneous Signal Descriptions – PQFP*, on page 43) allow the designer to match the output waveform to the magnetic characteristics. Both transmit and receive terminations are built into the LXT9785/LXT9785E so no external components are required between the LXT9785/LXT9785E and the external transformer. The transmitter uses a transformer with a center tap to help reduce power consumption.

When operating at 100 Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT9785/LXT9785E generates “IDLE” symbols.

During 10 Mbps operation, LXT9785/LXT9785E encoded data is exchanged. When no data are being exchanged, the line is left in an idle state with NLPs transmitted to maintain link.

4.2.1.2 MDI Crossover (MDIX)

The LXT9785/LXT9785E crossover function, which is compliant to the IEEE 802.3, clause 23 standard, connects the transmit output of the device to the far-end receiver in a link segment. This function can be disabled via Register bits 27.9:8 or by using the hardware configuration pins.

Table 40 MDIX Selection

AMDIX_EN	MDIX	MDIX Mode
0	0	MDI forced
0	1	MDIX forced
1	X	Auto MDI/MDIX

Note: The BGA15 package does not support MDIX hardware configuration. Software must be used to control the function after power-up.

4.2.1.3 Fiber Interface

The LXT9785/LXT9785E fiber ports are designed to interface with common industry-standard 3.3 V and 5 V fiber transceivers. Each of the 8 ports incorporates a Low-Voltage PECL interface that complies with the ANSI X3.166 standard for seamless integration.

Note: The BGA15 package does not support the fiber interface.

Fiber mode is selected through Register bit 16.0 by the following two methods:

1. Configure Register bit 16.0 = 1 on a global basis (all 8 ports) by driving the Hardware Control pin G_FX/TP_L to a logic High value on power-up and/or reset.
2. Configure Register bit 16.0 = 1 on a per-port basis through the MDIO interface.

The fiber interface is capable of full-duplex or half-duplex operation. In half duplex, operation collisions must be managed by external Layer 2 logic (MAC). Auto negotiation is not supported for fiber mode.

4.3 Media Independent Interface (MII) Interfaces

The LXT9785/LXT9785E supports Reduced MII or Serial MII, but not concurrently. The interface mode selection pins configures the device for either RMII or SMII/SS-SMII on all eight ports. Refer to Table 41 for the mode select settings.

Note: The BGA15 package does not support the RMII interface.

4.3.1 Global MII Mode Select

The mode select pins are used for MII interface configuration settings upon power-up sequencing. All ports are configured the same and cannot be intermixed.

Table 41 MII Mode Select

Configuration	ModeSel1	ModeSel0
RMII[1]	0	0
SMII	0	1
SS-SMII	1	0
Reserved	1	1

1. Invalid for the BGA15 package.

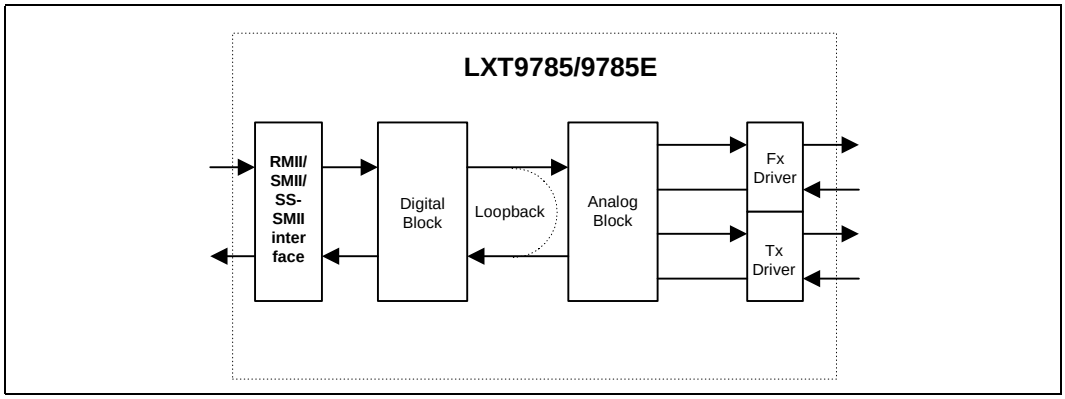
4.3.2 Internal Loopback

Register bit 0.14 must be set to enable internal loopback operation. Register bits 16.14 and 0.8 must be set for 10 Mbps operation. Cortina recommends that auto-negotiation be disabled while internal loopback is enabled. The normal auto-negotiation process code word exchange cannot be completed.The following two-step sequence is recommended for the most efficient mode change when enabling forced 100 Mbps internal loopback mode directly from auto-negotiation mode:

1. Write Register 0 with 0x2100h (forced 100 Mbps), and
2. Write Register 0 with 0x6100h (enable internal loopback with forced 100 Mbps)

This two-step process ensures the 100 Mbps link comes up quickly. If the one-write process of writing 0x6100h is followed, it may take up to 1.5 seconds before link is established and data is received on the port. The 1.5 second delay is due to the IEEE auto-negotiation Break Link Timer (BLT) requirement. The timer must expire before link is established when changing modes directly from auto-negotiation to internal loopback forced 100 Mbps mode. Use the above two-step process to eliminate the auto-negotiation BLT timer requirement.

Figure 8 Internal Loopback



4.3.3 RMII Data Interface

The LXT9785/LXT9785E provides a separate RMII for each network port, each complying with the RMII Specification, Revision 1.2. The RMII includes both a data interface and an MDIO management interface. The RMII Data Interface exchanges data between the LXT9785/LXT9785E and up to eight Media Access Controllers (MACs).

4.3.4 Serial Media Independent Interface (SMII) and Source Synchronous- Serial Media Independent Interface (SS-SMII)

4.3.4.1 SMII Interface

The LXT9785/LXT9785E provides an independent serial interface for each network port, complying with the Serial-MII Specification, Revision 1.2. All SMII ports use a common reference clock and SYNC signal. The SMII Data Interface exchanges data between the LXT9785/LXT9785E and multiple Media Access Controllers (MACs). All signals are synchronous to the reference clock. One SYNC control stream is sourced by the MAC to the PHY. Both the transmit and receive data streams are segmented into boundaries delimited by the SYNC pulses. This interface is expected to drive up to 6 inches of trace lengths.

4.3.4.2 Source Synchronous-Serial Media Independent Interface

The new revision to the SMII interface, SS-SMII, allows for a longer trace length and helps to relieve timing constraints, requiring the addition of four new signals, TxCLK, TxSYNC, RxCLK, and RxSYNC. The transmit TxCLK and TxSYNC are sourced from the MAC to the PHY and referenced to the REFCLK input. The receive RxCLK and RxSYNC are sourced by the PHY to the MAC and in reference to the REFCLK.

4.3.5 Configuration Management Interface

The LXT9785/LXT9785E provides an MDIO Management Interface and a Hardware Control Interface (via the CFG pins) for device configuration and management. Mode control selection is provided via the MDDIS pin as shown in Table 9, *MDIO Control Interface Signals – PQFP*, on page 41. When sectionalization (2x4) is selected, separate MDIO interfaces are enabled (see Figure 13 on page 124).

4.3.6 MII Isolate

In applications where the MII must be isolated from the bus, the RMII and the SMII/SS-SMII configurations can be three-stated using Register 0.10. On each individual port, Register bit 0.10 controls the isolation of the transmit and receive data signals for that port. Register bit 0.10 on ports 0 and 4 isolate the RxCLK*n*/TxCLK*n* and SYNC signals.

When 1x8 sectionalization is selected, TxCLK0, TxSYNC0, RxCLK1, and RxSYNC1 are used for the clocking and synchronization interface. Port 4 controls the isolation of RxCLK0, RxCLK1, RxSYNC0, and RxSYNC1, and must be used to isolate the receive clock and synchronization interface.

When 2x4 sectionalization is selected, TxCLK0, TxSNC0, RxCLK0, and TxCLK0 are used for Port 0 through Port 3 and TxCLK1, TxSYNC1, RxCLK1, and RxSYNC1 are used for Port 4 through Port 7. Port 0 must be isolated to isolate the receive clock and synchronization interface for Port 0 through Port 3. Port 4 must be isolated to isolate Port 4 through Port 7.

4.3.7 MDIO Management Interface

The LXT9785/LXT9785E supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT9785/LXT9785E. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers. Some registers are required and their functions are defined by the IEEE 802.3 specification. Additional registers allow for expanded functionality. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, all the MDIOs are completely disabled. The Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used.

Note: The BGA15 package does not support the MDDIS pin.

The timing for the MDIO Interface is shown in Table 80, *MDIO Timing Parameters*, on page 189. MDIO read and write cycles are shown in Figure 9, *Management Interface Read Frame Structure*, on page 119 and Figure 10, *Management Interface Write Frame Structure*, on page 119.

Figure 9 Management Interface Read Frame Structure

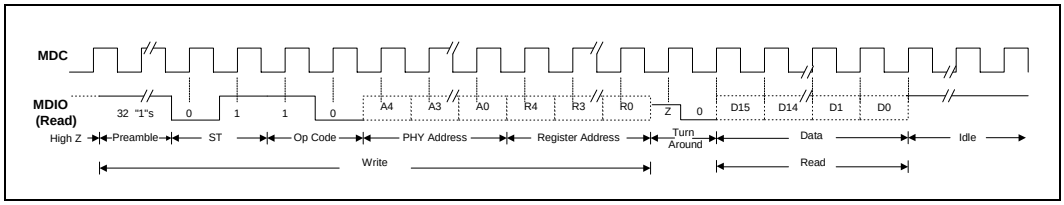
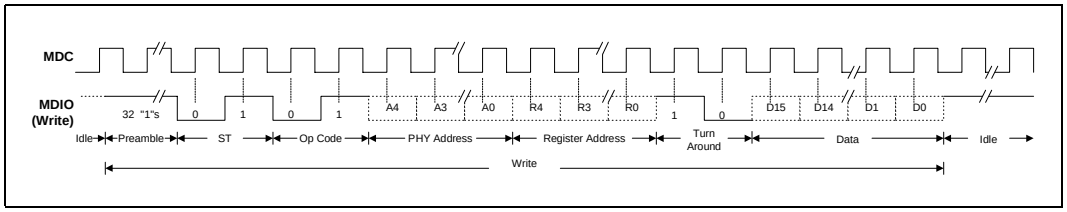


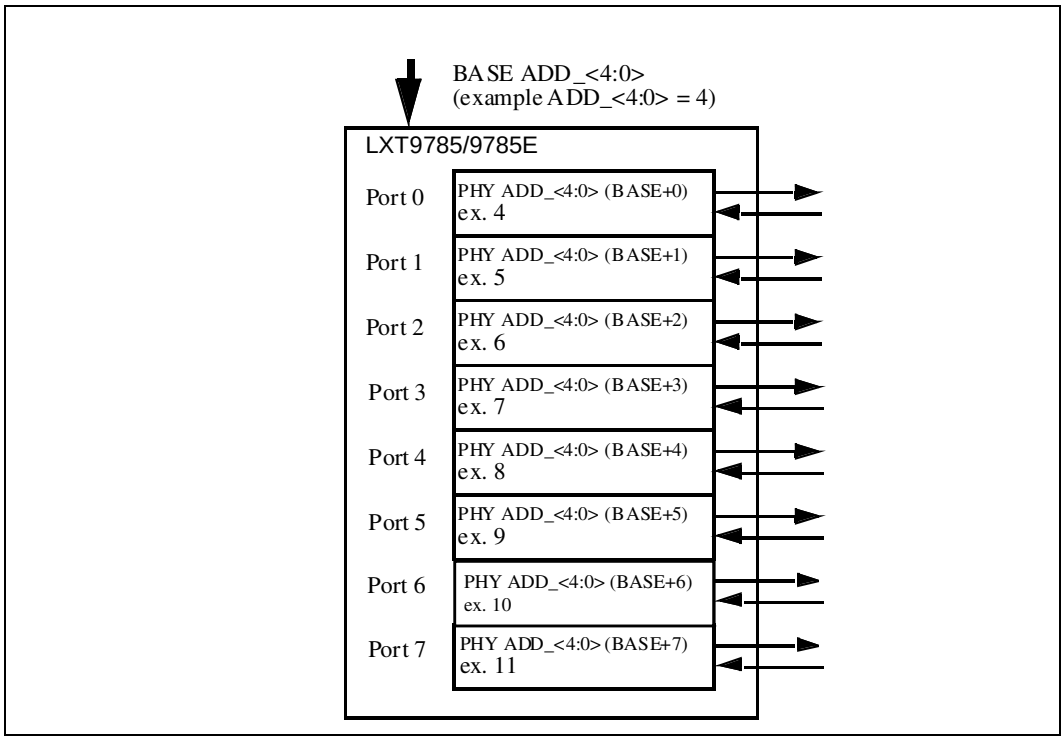
Figure 10 Management Interface Write Frame Structure



The protocol allows one controller to communicate with multiple LXT9785/LXT9785E devices. Pins ADD_<4:0> determine the base address. Each port adds its port number to the base address to obtain its port address as shown in Figure 11.

The BGA15 package uses a similar scheme where the ADD_[2:0] bits internally set to 0 and the ADD_[4:3] bits are used to select from four base addresses (0x00000b, 0x01000b, 0x10000b, or 0x11000b.

Figure 11 Port Address Scheme



4.3.8 MII Sectionalization

When sectionalized into two quad sections, the MDIO bus splits into two separate PHY access ports. Ports 0-3 of the MDIO section operate independently of ports 4-7. The MII isolate function is unaffected and operates normally. Sectionalization is selected by pulling pin 176 (Section) High on the initial power-up sequence (refer to Figure 13). In applications that need sectionalization, such as 1x8 and 2x4 and have a single MDIO bus structure, it is necessary that the addressing scheme be contiguous. For example, the first eight ports are addressed 0-7, so the next four ports must be addressed 8-11.

Note: The BGA15 package does not support the MII sectionalization feature.

4.3.9 MII Interrupts

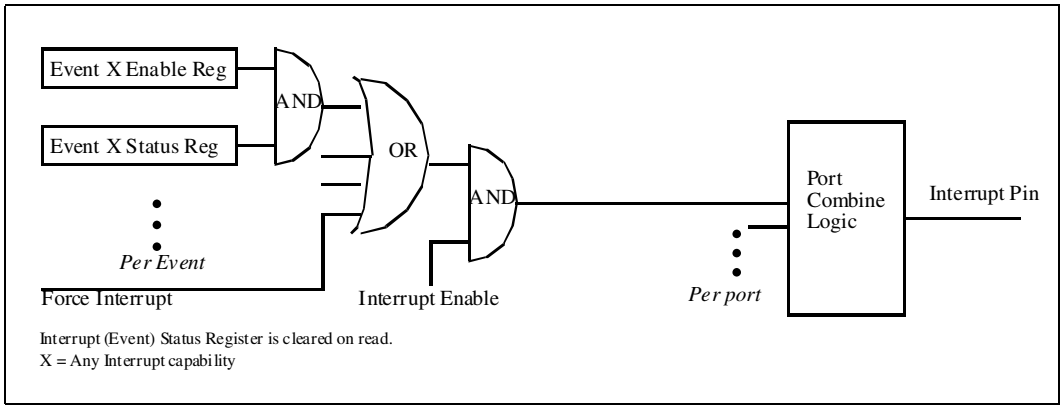
The LXT9785/LXT9785E provides a single per-section interrupt pin that is available to all ports. Interrupt logic is shown in Figure 12. The LXT9785/LXT9785E also provides two dedicated interrupt registers for each port. Register 18 provides interrupt enable and mask functions and Register 19 provides interrupt status. Setting Register bit 18.1 = 1 enables a port to request interrupt via the MDINT_L pin. An active Low on this pin indicates a status change on the device. Because it is a shared interrupt, there is no indication which port is requesting interrupt service (see Figure 12).

There are five conditions that may cause an interrupt:

- Auto-negotiation complete.
- Speed status change.

- Duplex status change.
- Link status change.
- Isolate status change.

Figure 12 Interrupt Logic



4.3.10 Global Hardware Control Interface

The LXT9785/LXT9785E provides a Hardware Control Interface for applications where the MDIO is not desired. Refer to Section 4.5, *Initialization*, on page 123 for additional details.

4.3.11 FIFO Initial Fill Values

The FIFO initial fill value sets the number of bits required to be written into the FIFO before the process of reading the packet out of the FIFO is started. The read operation is aligned on nibble boundaries because the FIFO is one nibble wide. The read clock on the RMII and SMII interfaces may occur any time within the next available nibble. Therefore, the effective size of the FIFO is one nibble less than the selected size.

Large initial fill FIFO settings alter both the data-path latency and the InterFrame Gap (IFG) output on the RMII and SMII interfaces. The latency values are increased or decreased depending on the number of bits the FIFO size is increased or decreased. The IFG may decrease up to twice the size of the initial fill FIFO setting. When the following three conditions are met, the IPG on the RMII and SMII interfaces may become nonexistent between packets, effectively concatenating the packets into one long corrupted packet:

- The frequency difference between the link partner and the local LXT9785/LXT9785E device exceed 200 ppm (the IEEE standard requirement).
- Jumbo packets (8192 byte packets or longer) are used.
- Packets on the wire occur with minimum Inter-Packet Gap (IPG) of 96 bit times.

The concatenation of the packets is flagged by the MAC as a CRC error and possibly an oversized packet depending upon the length indication capabilities of the MAC. The possibility of packet concatenation can be minimized on the RMII interface by setting the initial fill FIFO Register bits 18.15:14 to 01. The FIFO setting bits should be set to 10 for the SMII interfaces.

4.4 Operating Requirements

4.4.1 Power Requirements

The LXT9785/LXT9785E requires four power supply inputs: VCCD, VCCA, VCCPECL and VCCIO. The digital and analog circuits require 2.5 V supplies (VCCD, VCCR, and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground. The fiber VCCPECL supply can be connected to either 2.5 V or 3.3 V.

A separate power supply may be used for the MII, JTAG and MDIO (VCCIO) interfaces. The power supply may be either +2.5 V or +3.3 V. VCCIO should be supplied from the same power source used to supply the controller on the other side of the interface. Refer to Table 54, *Digital I/O DC Electrical Characteristics (VCCIO = 2.5 V +/- 5%)*, on page 171, Table 55, *Digital I/O DC Electrical Characteristics (VCCIO = 3.3 V +/- 5%)*, on page 172, and Table 56, *Digital I/O DC Electrical Characteristics – SD Pins*, on page 172 for I/O characteristics.

As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in Figure 34 on page 165. The power supplies should be brought up as close to the same time as possible. However, there are no specific timing requirements.

4.4.2 Clock / SYNC Requirements

4.4.2.1 Reference Clock

The LXT9785/LXT9785E requires a constant enabled reference clock (REFCLK). REFCLK's frequency must be 50 MHz for RMII or 125 MHz for SMII/SS-SMII. The reference clock is used to generate transmit signals and recover receive signals. A crystal-based clock is recommended over a derived clock (that is, PLL-based) to minimize transmit jitter. Refer to Table 57, *Required Clock Characteristics*, on page 172 for clock timing requirements.

For applications that use a single 8-port sectionalization, REFCLK0 and REFCLK1 must always be tied together and to the source. In 2x4 applications, REFCLK0 and REFCLK1 are not tied together.

4.4.2.2 TxCLK Signal (SS-SMII only)

The LXT9785/LXT9785E requires a 125 MHz input transmit clock synchronous with TxData*n* and frequency locked to REFCLK. See Figure 22 on page 137.

4.4.2.3 TxSYNC Signal (SMII / SS-SMII)

The LXT9785/LXT9785E requires a 12.5 MHz input pulse for SMII synchronization. See Figure 22 on page 137.

4.4.2.4 RxSYNC Signal (SS-SMII only)

The LXT9785/LXT9785E provides a 12.5 MHz output pulse synchronous with the RxData*n* outputs. See Figure 23 on page 137.

4.4.2.5 RxCLK Signal (SS-SMII Only)

In SS-SMII mode, the LXT9785/LXT9785E provides a 125 MHz clock output in reference to the output RxData*n*. RxCLK is referenced and synchronized to the REFCLK. See Figure 23 on page 137.

Note: Although RXCLK is referenced to REFCLK, the RXCLK may vary in cumulative phase by up to four bit-times relative to REFCLK.

4.5 Initialization

When the LXT9785/LXT9785E is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control or MDIO interface as shown in Figure 13 on page 124.

4.5.1 MDIO Control Mode

In the MDIO Control mode, the LXT9785/LXT9785E reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

4.5.2 Hardware Control Mode

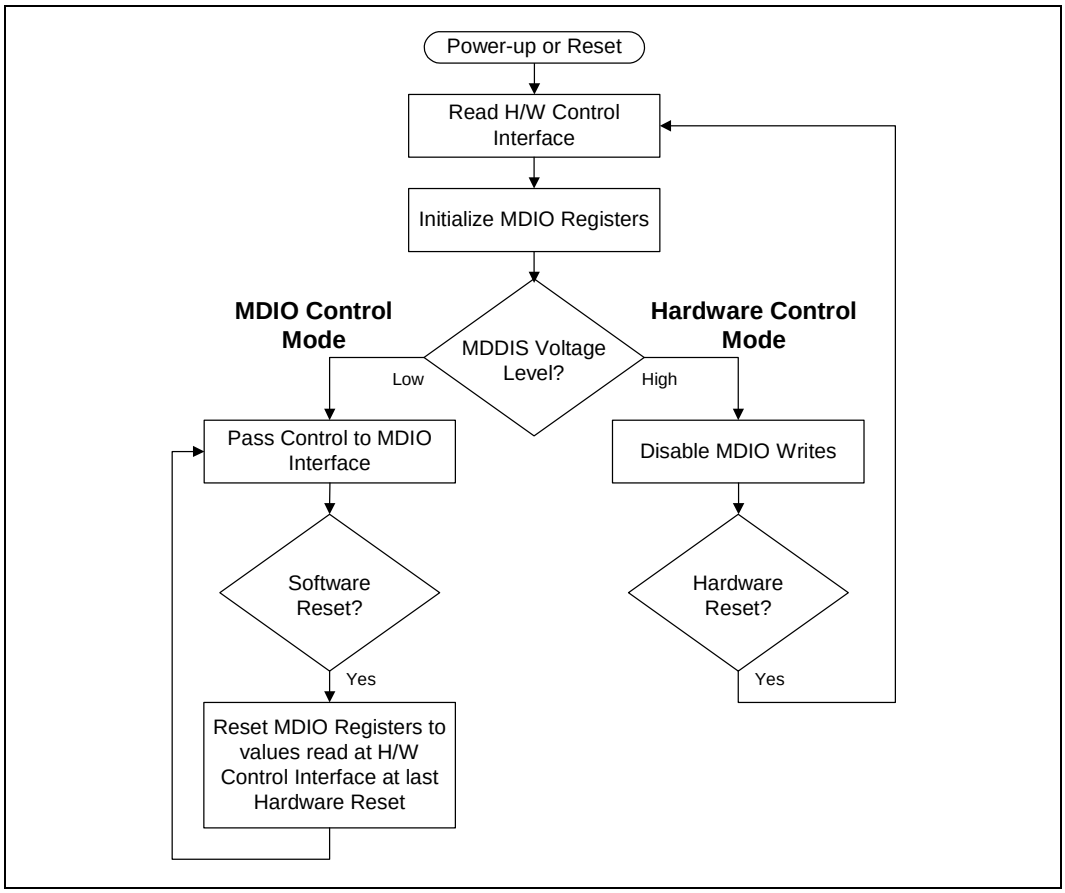
In the Hardware Control Mode, the LXT9785/LXT9785E disables direct write operations to the MDIO registers via the MDIO Interface. On power-up or hardware reset, the LXT9785/LXT9785E reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

The following modes are available using either Hardware Control or MDIO Control:

- Force network link to 100BASE-FX (Fiber).
- Force network link operation to:
  - 100BASE-TX, Full-Duplex
  - 100BASE-TX, Half-Duplex
  - 10BASE-T, Full-Duplex
  - 10BASE-T, Half-Duplex
- Allow auto-negotiation/parallel-detection.
- Auto/Manual MDIX enable/disable.
- Pause for full-duplex links operation.
- Global Output Slew Rate Control.

When the network link is forced to a specific configuration, the LXT9785/LXT9785E immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT9785/LXT9785E begins the auto-negotiation/ parallel-detection operation.

Figure 13 Initialization Sequence



4.5.3 Power-Down Mode

The LXT9785/LXT9785E incorporates numerous features to maintain the lowest power possible. The device can be put into a low-power state via Register 0 as well as a near-zero power state with the power down pin. When in power-down mode, the device is not capable of receiving or transmitting packets.

The lowest power operation is achieved using the Global power-down pin, which is active High. This pin powers down every circuit in the device, including all clocks. All registers are unaltered and maintained when the Global PWRDWN pin is released.

Note: The BGA15 package does not support the PWRDWN pin feature.

Individual ports (software power down) can be powered down using Register bit 0.11. This bit powers down a significant portion of the port, but clocks to the register section remain active. This allows the management interface to remain active during register power-down. The power-down bit is active High.

Note: Cortina recommends that a minimum recovery time be allowed after bringing up a port from software or hardware power-down or link hold-off modes. The recovery times are specified in Table 81, *Power-Up Timing Parameters*, on page 190

4.5.3.1 Global (Hardware) Power Down

The global power-down mode is controlled by the PWRDWN pin. When PWRDWN is High, the following conditions are true:

- All LXT9785/LXT9785E ports and the clock are shut down.
- All outputs are three-stated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.
- Configuration pins are read upon release of the PWRDWN pin, and registers are loaded with the current values of the hardware configuration pins.

4.5.3.2 Port (Software) Power Down

Individual port power-down control is provided by Register bit 0.11 in the respective port Control Registers (refer to Table 84, *Control Register (Address 0)*, on page 192). During individual port power-down, the following conditions are true:

- The individual port is shut down.
- The MDIO registers remain accessible.
- Pull-up and pull-down resisters are not affected and the outputs are not three-stated.
- The register remains unchanged.

4.5.4 Reset

The LXT9785/LXT9785E provides both hardware and software resets. Configuration control of Auto-Negotiation, speed, and duplex mode selection is handled differently for each. During a hardware reset, settings for bits 0.13, 0.12, 0.8, and 4.8:5 are read in from the pins (refer to Table 42, *Global Hardware Configuration Settings*, on page 126 for pin settings, and Table 84, *Control Register (Address 0)*, on page 192 and Table 88, *Auto-Negotiation Advertisement Register (Address 4)*, on page 195 for register bit definitions).

During a software reset (Register bit 0.15 = 1), the bit settings are not re-read from the pins and revert back to the values that were read in during the last hardware reset. Any changes to pin values from the last hardware reset are not detected during a software reset.

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. All MII interface pins are disabled during a hardware reset and released to the bus on de-assertion of reset.

During a software reset (0.15 = 1) the registers are available for reading. The reset bit should be polled to see when the part has completed reset (0.15 = 0). Pull up and pull down resisters are not affected.

Cortina recommends that a minimum recovery time be allowed after bringing up a port from software or hardware reset. The recovery times are specified in Table 81, *Power-Up Timing Parameters*, on page 190

4.5.5 Hardware Configuration Settings

The LXT9785/LXT9785E provides a hardware option to set the initial device configuration. The hardware option uses three Global CFG pins that provide control for all ports (see Table 42).

Table 42 Global Hardware Configuration Settings

Desired Mode			CFG Pin Settings[1]			Resulting Register Bit Values						
AutoNeg	Speed	Duplex	1	2	3	0.12	0.13	0.8	4.8	4.7	4.6	4.5
Disabled	10	Half	Low	Low	Low	0	0	0	N/A Auto-Negotiation Advertisement			
		Full	High	Low	High			1				
	100	Half	Low	High	Low		1	0				
		Full	High	High	High			1				
Enabled	100	Half	High	Low	Low	1	1	0	0	1	0	0
		Full/Half	High	Low	High		1	0	1	1		
	10/100	Half	High	High	Low		1	0	0	1	0	1
		Full/Half	High	High	High		1	0	1	1	1	1

1. Refer to Table 5, *RMII Signal Descriptions – PQFP*, on page 36 through Table 17, *Receive FIFO Depth Considerations*, on page 50 Table 24, *RMII Signal Descriptions – BGA23*, on page 80 through Table 36, *Receive FIFO Depth Configurations*, on page 96, and Table 39, *BGA15 Signal Descriptions*, on page 106 for CFG pin assignments.

4.6 Link Establishment

4.6.1 Auto-Negotiation

The LXT9785/LXT9785E attempts to auto-negotiate with its link partner by sending Fast Link Pulse (FLP) bursts. Each burst consists of 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may also be present or absent to indicate a “1” or a “0”. Each FLP burst exchanges 16 bits of data, referred to as a “page”. All devices that support auto-negotiation must implement the “Base Page”, defined by IEEE 802.3 (registers 4 and 5). The LXT9785/LXT9785E also supports the optional “Next Page” function (registers 7 and 8).

4.6.1.1 Base Page Exchange

By exchanging Base Pages, the LXT9785/LXT9785E and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to proceed. Each side finds their highest common capabilities, exchange more pages, and agree on the operating state of the line.

4.6.1.2 Manual Next Page Exchange

Additional information, exceeding that required by base page exchange, is also sent via “Next Pages.” The LXT9785/LXT9785E fully supports the IEEE 802.3 method of negotiation via Next Page exchange. The Next Page exchange uses Register 7 to send information and Register 8 to receive it. Next Page exchange occurs only if both ends of the link partners advertise their ability to exchange Next Pages. A special mode has been added to make manual next page exchange easier for software. When Register 6 “page”

is received, it stays set until read. This bit is cleared when a new negotiation occurs, preventing the user from reading an old value in Register 6 and assuming there is valid information in Registers 5 and 8. The page received bit is cleared upon reading the Section Table 90, *Auto-Negotiation Expansion Register (Address 6)*, on page 197.

4.6.1.3 Controlling Auto-Negotiation

The following steps are recommended when auto-negotiation is controlled by software:

- After power-up, power-down, or reset, the power-down recovery time, as specified in Table 81, *Power-Up Timing Parameters*, on page 190, must be exhausted before proceeding.
- Set the auto-negotiation advertisement register bits in Register 4 as desired.
- Enable auto-negotiation (set MDIO Register bit 0.12 = 1).
- Enable or restart auto-negotiation as soon as possible after writing to Register 4 to ensure proper operation.

4.6.1.4 Link Criteria

In 100 Mbps mode, link is established when the descrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the descrambler receives less than 16 consecutive idle symbols in any 2 ms period. This provides a robust operation, filtering out any small noise hits that may disrupt the link.

MLT-3 idle waveforms, for short periods, meet all the criteria for 10BASE-T start delimiters. A working 10BASE-T receive may temporarily indicate link to 100BASE-TX waveforms. However, the PHY will not bring up a permanent 10 Mbps link.

According to the IEEE standard 10 Mbps link state machine, the last condition that must be met before 10 Mbps link can come up is a period of transmit and receive idle time. TXEN and RXDV are inactive at the same time. This ensures that link is not brought up in the middle of transmitting or receiving a packet. To ensure link establishment, Cortina recommends no packet transmission into the MII interface until link is established.

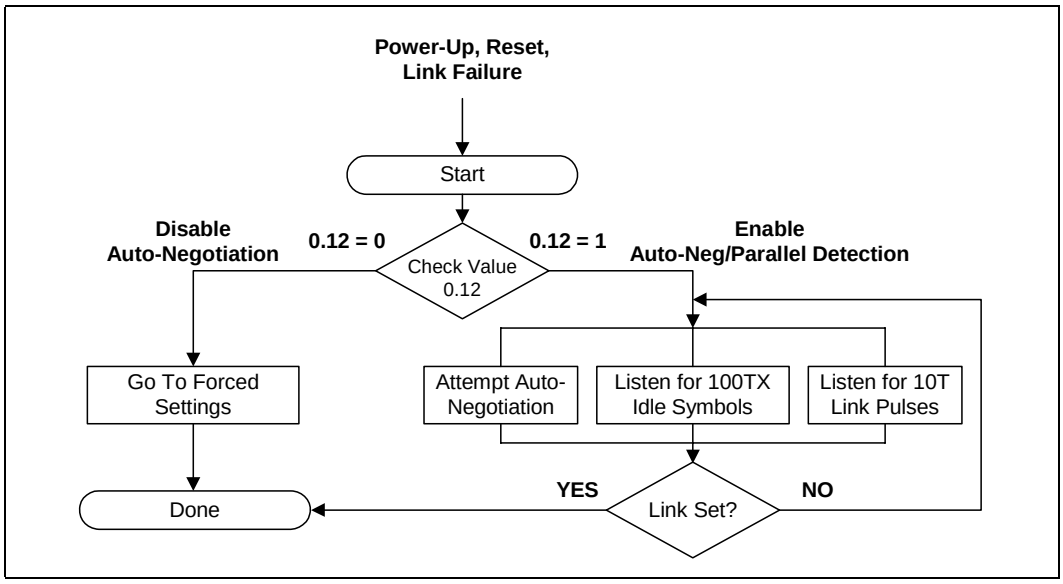
The IEEE Standard references this requirement in Section 14.2.3 State Diagrams, Figure 14-6-Link Integrity Test Function State Diagram and in Section 28.3.4 State Diagrams, Figure 28-17-NLP Receive Link Integrity Test State Diagram. These diagrams illustrate that while the PHY is in the Link Test Fail Extend state, the last state before Link Pass state) Packet receive activity (RD) and Transmit Activity (DO) must be idle (RD = idle * D0 = idle) for link to establish.

4.6.1.5 Parallel Detection

In parallel with auto-negotiation, the LXT9785/LXT9785E also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either symbol is detected, the device automatically reverts to the corresponding operating speed in half-duplex mode. Parallel detection allows the LXT9785/LXT9785E to communicate with devices that do not support auto-negotiation.

When parallel detection resolves a link, the link must be established in half-duplex mode. According to IEEE standards, the forced link partner cannot be configured to full-duplex. If the auto-negotiation link partner does not advertise half-duplex capability at the speed of the forced link partner, link is not established. The IEEE Standard prevents forced full-duplex-to-half-duplex link connections.

Figure 14 Auto-Negotiation Operation



4.6.1.6 Reliable Link Establishment While Auto MDI/MDIX is Enabled in Forced Speed Mode

With auto MDI/MDIX hardware enabled, end users experience reliable link establishment under all settings of auto MDI/MDIX and speed between the LXT9785/LXT9785E and its link partners. As stated in the IEEE clauses 40.4.5.1 (Auto MDI/MDIX) and 28.3.2 (Parallel Detect), when ports are forced to 10 Mbps or 100 Mbps and auto MDI/MDIX is enabled, and the port is connected to a partner with auto-negotiation enabled, an undefined condition exists between the IEEE auto MDIX and Parallel Detect specifications. Link may not occur according to the IEEE specification.

During this undefined condition, when the LXT9785/LXT9785E is set to 10 Mbps or 100 Mbps and auto MDI/MDIX is enabled, the LXT9785/LXT9785E and the link partner auto-negotiation processes are expected to be skewed enough to establish link in all but the rarest cases. Auto MDI/MDIX is configured through hardware and software. If auto MDI/MDIX operation is desired in forced modes, disabling auto MDI/MDIX using the software programming can aid link establishment.

4.7 Serial MII Operation

The LXT9785/LXT9785E exchanges transmit and receive data with the controller via the Serial MII (SMII). The SMII performs the following functions:

- Conveys complete MII information between a 10/100 PHY and MAC with two pins per port.
- Allows a multi-port MAC/PHY communication with one system clock.
- Operates in both half and full-duplex.
- Supports per-packet switching between 10 Mbps and 100 Mbps data rates.

The Serial MII operates at 125 MHz using a global reference clock and frame synchronization signal (REFCLK and SYNC). Each port has an individual two-line data interface (TxData*n* and RxData*n*). All signals are synchronous to REFCLK. Table 43 summarizes the SMII signals.

Data is exchanged in 10-bit serial words. Each word contains one data byte (two nibbles of 4B coded data) and two status bits. When the port is operating at 100 Mbps, each word contains a new data byte. When the port is operating at 10 Mbps, each data byte is repeated 10 times.

Table 43 SMII Signal Summary

Signal	To	From	Purpose
TxData	PHY	MAC	Transmit data & control
SYNC	PHY	MAC	Synchronization
RxData	MAC	PHY	Receive data & control
REFCLK	MAC & PHY	System	Synchronization

1. Refer to Table 7, *SMII Specific Signal Descriptions – PQFP*, on page 39 for detailed signal descriptions.

Figure 15 Typical SMII Interface

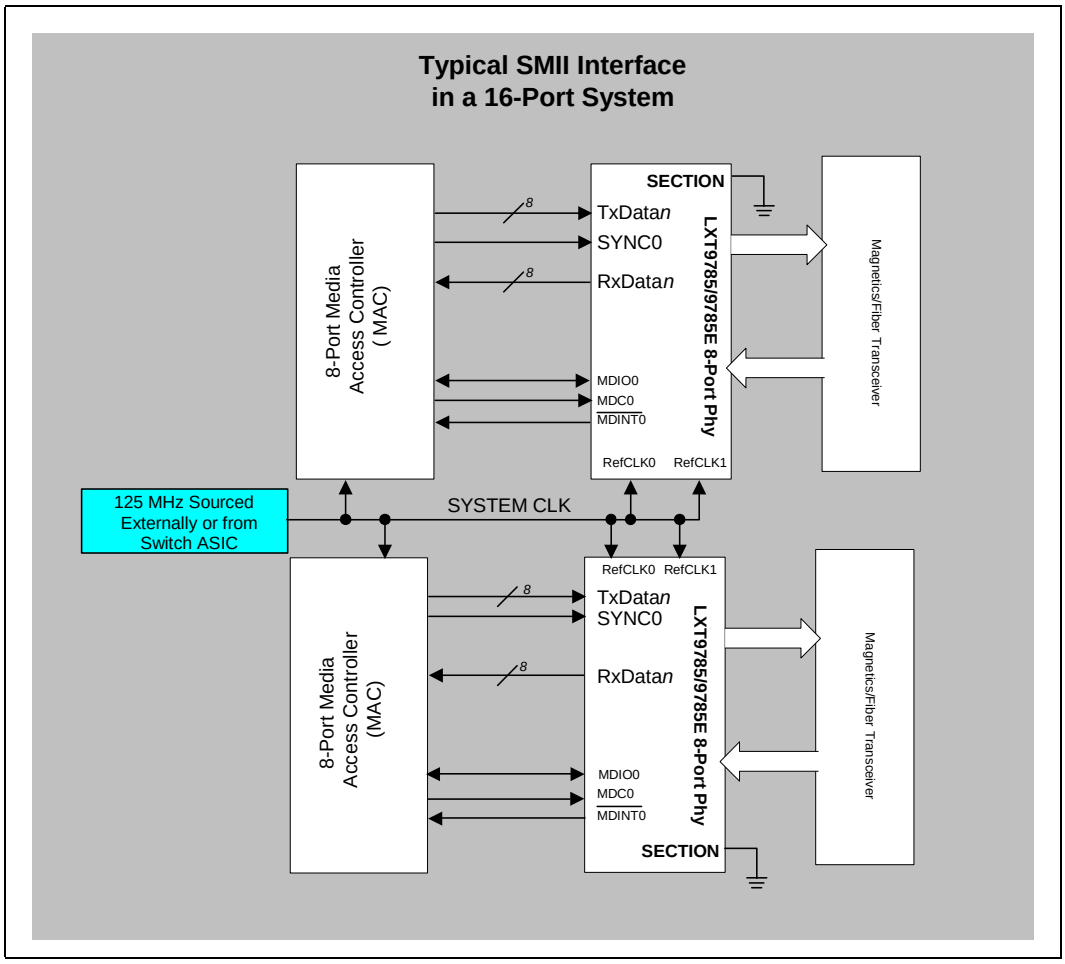


Figure 16 Typical SMII Quad Sectionalization

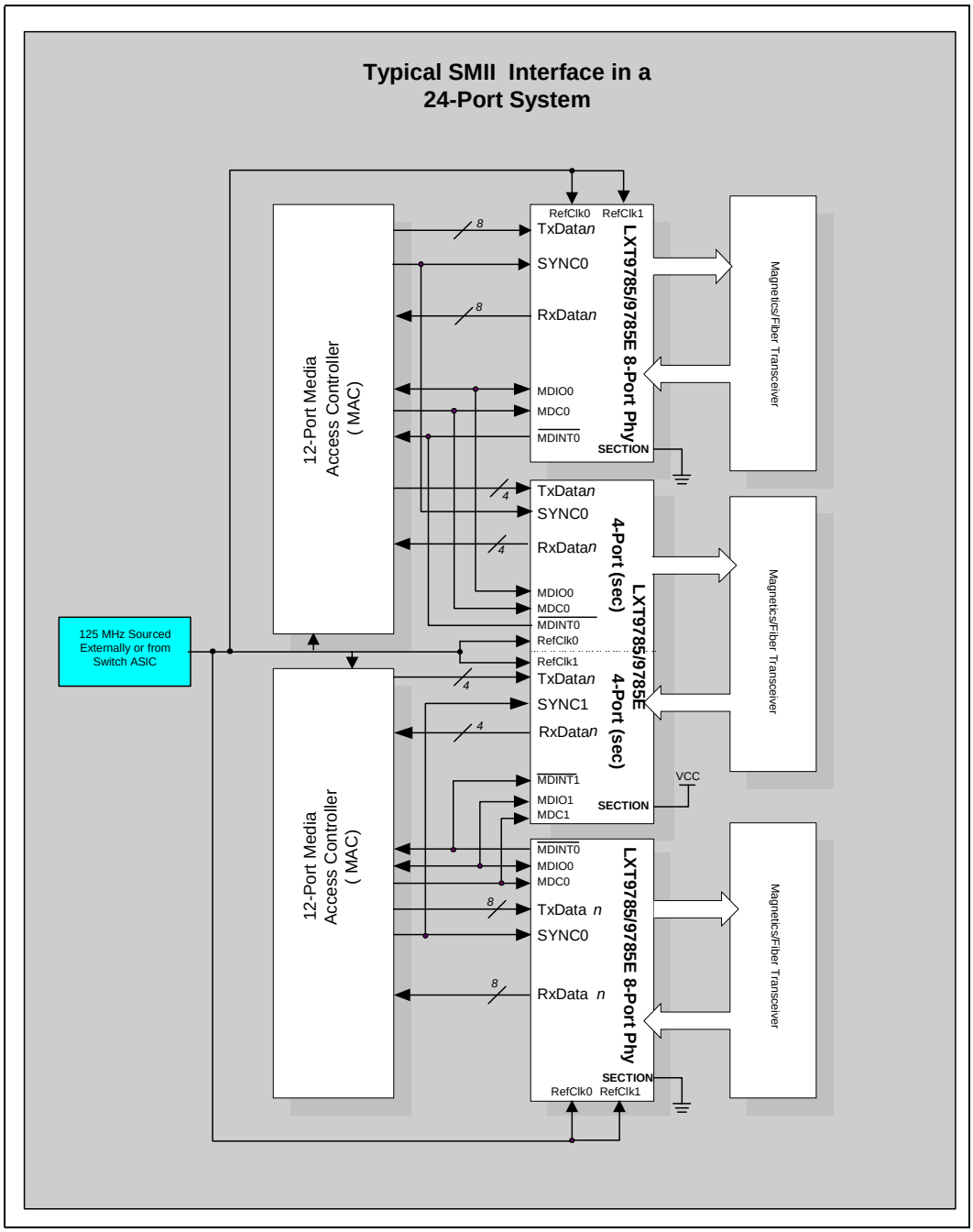
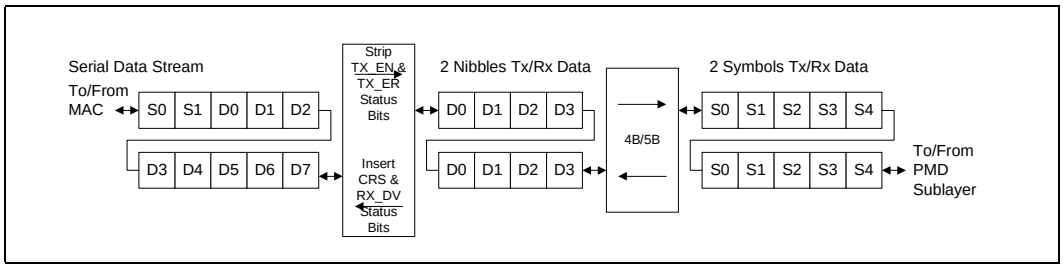


Figure 17 100 Mbps Serial MII Data Flow



4.7.1 SMII Reference Clock

The REFCLK operates at 125 MHz. The transmit and receive data and control streams must always be synchronized to the REFCLK by the MAC and PHY. The LXT9785/LXT9785E samples these signals on the rising edge of the REFCLK.

4.7.2 TxSYNC Pulse (SMII/SS-SMII)

The TxSYNC pulse delimits segment boundaries and synchronizes with REFCLK. The MAC must continuously generate a TxSYNC pulse once every 10 REFCLK cycles. The TxSYNC pulse signals the start of each new segment (see Figure 21 on page 136).

4.7.3 Transmit Data Stream

Transmit data and control information are signaled in ten- bit segments. In 100 Mbps mode, each segment contains a new byte of data. In 10 Mbps mode, the MAC must repeat a 10M serial word ten times on TxData. The LXT9785/LXT9785E may sample that serial word at any point.

The TxSYNC pulse signals the start of a new segment as shown in Figure 18.

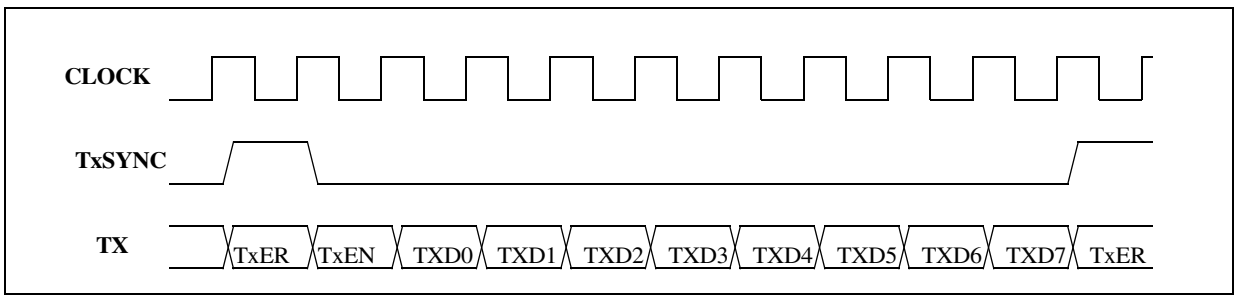
4.7.3.1 Transmit Enable

The MAC must assert the TxEN bit in each segment of TxData, and de-assert TxEN*n* after the last segment of the packet.

4.7.3.2 Transmit Error

When the MAC asserts the TxER bit in 100BASE-X mode, the LXT9785/LXT9785E drives “H” symbols onto the network interface. TxER does not have any function in 10M operation.

Figure 18 Serial MII Transmit Synchronization



4.7.4 Receive Data Stream

Receive data and control information are signalled in ten-bit segments. In 100 Mbps mode, each segment contains a new byte of data. In 10 Mbps mode, each segment is repeated ten times (except for the CRS bit), and the MAC can sample any of the ten segments.

4.7.4.1 Carrier Sense

The CRS bit (slot 0) is generated when a packet is received from the network interface. The CRS bit is set in real time, even in 10 Mbps mode (all other bits are repeated in 10 sequential segments).

4.7.4.2 Receive Data Valid

The LXT9785/LXT9785E asserts the RX_DV bit (slot 1) when it receives a valid packet. The assertion timing changes depending on line operating speed:

- For 100BASE-TX and 100BASE-FX links, the RX_DV bit is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. The RX_DV bit is asserted with the first nibble of the Start-of-Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

4.7.4.3 Receive Error

When the LXT9785/LXT9785E receives an invalid symbol from the network in 100BASE-TX mode, it drives “0101” on the associated RxData signals.

4.7.4.4 Receive Status Encoding

The LXT9785/LXT9785E encodes status information onto the RxData line during IPG as seen in Table 44 on page 134. Status bit RxData<5> indicates the validity of the upper nibble (RxData<7:4> of the last byte of the previous frame). RxData and RX_DV are passed through the internal elasticity FIFO to smooth any clock rate differences between the recovered clock and the 125 MHz reference clock.

4.7.5 Collision

The SMII interface does not provide a collision output and relies on the MAC to interpret COL conditions using CRS and TxEN. CRS is unaffected by the transmit path.

Figure 19 Serial MII Receive Synchronization

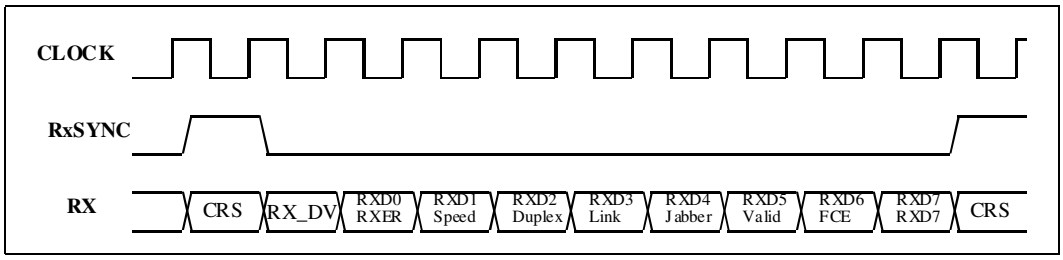


Table 44 RX Status Encoding Bit Definitions

Signal	Definition	
CRS	Carrier Sense - identical to MII, except that it is not an asynchronous signal.	
RxDV	Receive Data Valid - identical to MII. When RX_DV = 0, status information is transmitted to the MAC. When RX_DV = 1, received data is transmitted to the MAC.	0 = Status Byte 1 = Valid Data Byte
RxER (RxData0)	Inter-frame status bit RxData0 indicates whether or not the PHY detected an error somewhere in the previous frame.	0 = No Error 1 = Error
SPEED (RxData1)	Inter-frame status bit RxData1 indicates port operating speed.	0 = 10 Mbps 1 = 100 Mbps
DUPLEX (RxData2)	Inter-frame status bit RxData2 indicates port duplex condition.	0 = Half-duplex 1 = Full-duplex
LINK (RxData3)	Inter-frame status bit RxData3 indicates port link status.	0 = Down 1 = Up
JABBER (RxData4)	Inter-frame status bit RxData4 indicates port jabber status.	0 = OK 1 = Error
VALID (RxData5)	Inter-frame status bit RxData5 conveys the validity of the upper nibble of the last byte of the previous frame	0 = Invalid 1 = Valid
False Carrier (RxData6)	Inter-frame status bit RxData6 indicates whether or not the PHY has detected a false carrier event.	0 = No FC detected 1 = FC detected
RxData7	This bit is set to 1.	1 = Always

1. Both RxData0 and RxData5 bits are valid in the segment immediately following a frame, and remain valid until the first data segment of the next frame begins.

4.7.6 Source Synchronous-Serial Media Independent Interface

Some system designs require the PHY to be placed between 3 to 12 inches away from the MAC. A new Source Synchronous-Serial Media Independent Interface (SS-SMII) definition has been added because of this requirement. To provide a source synchronous interface between the PHY and MAC, the PHY must drive the RxCLK and the RxSYNC signals to the MAC. Also, the MAC must drive the TxCLK and the TxSYNC signal to the PHY. The REFCLK is also needed to synchronize the data to the PHY's core clock domain. TxData is clocked in using TxCLK and then synchronized to REFCLK and transmitted to the twisted-pair. The RxData is synchronized to the RxCLK. See Figure 23 on page 137.

Table 45 SS-SMII

Signal	To	From	Purpose
TxData	PHY	MAC	Transmit data & control
TxCLK	PHY	MAC	Transmit clock
TxSYNC	PHY	MAC	Synchronization pulses
RxData	MAC	PHY	Receive data & control
RxCLK	MAC	PHY	Receive clock
RxSYNC	MAC	PHY	Receive Synchronization
REFCLK	MAC	System	Synchronization

Figure 20 Typical SS-SMII Interface

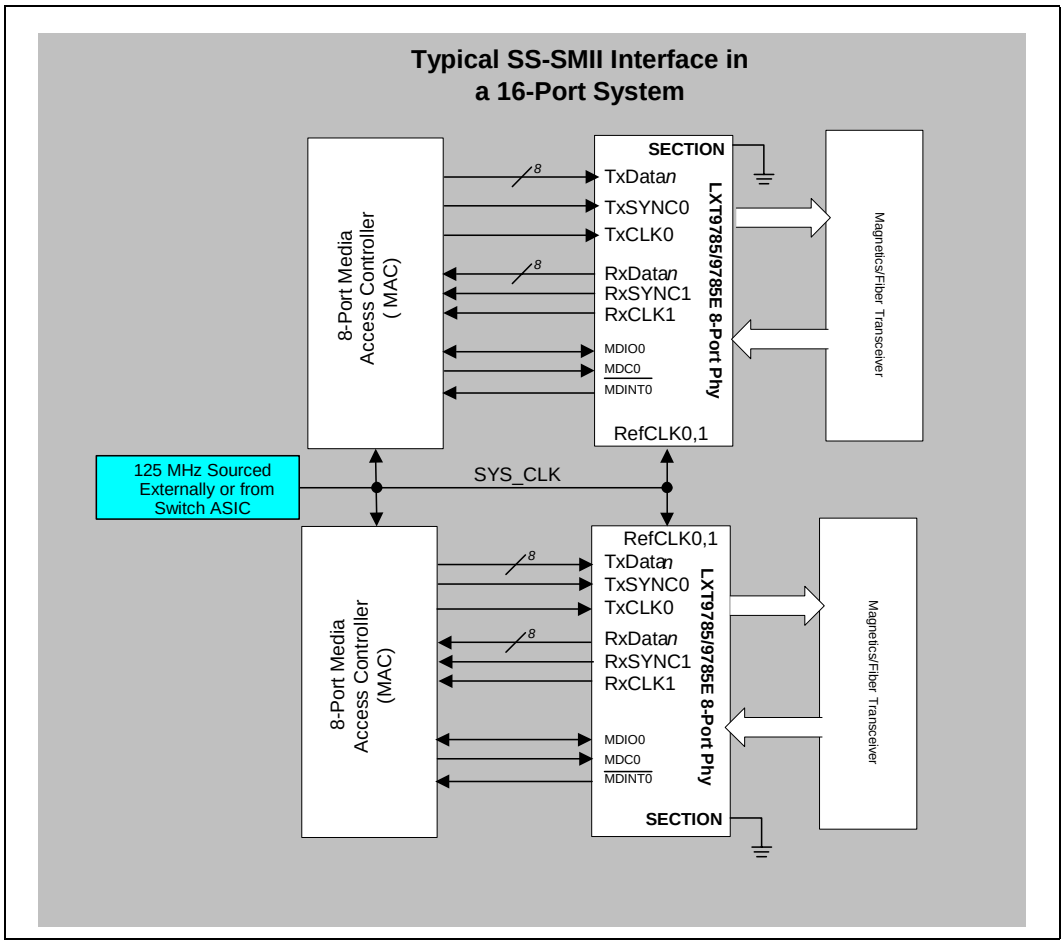


Figure 21 Typical SS-SMII Quad Sectionalization

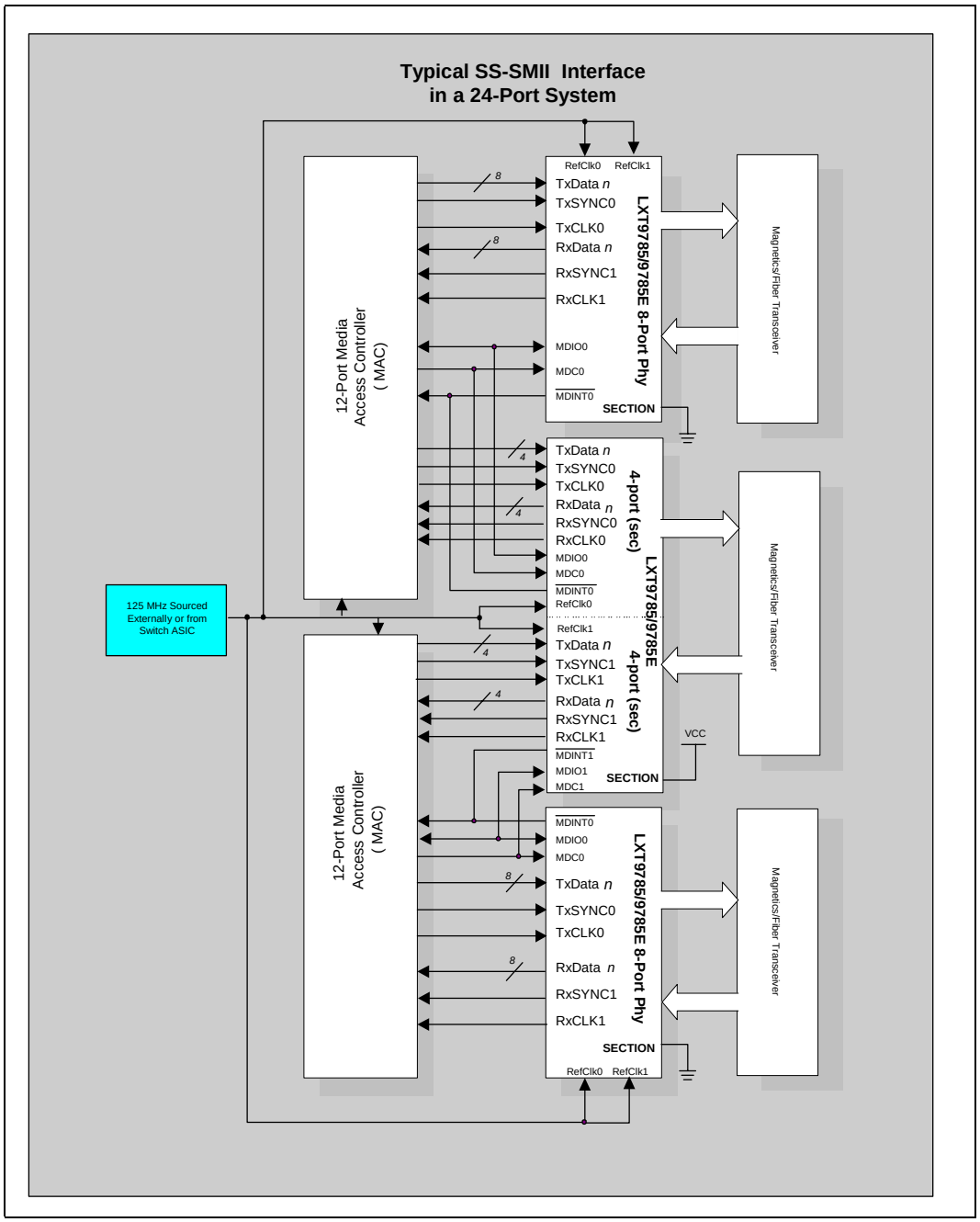


Figure 22 SS-SMII Transmit Timing

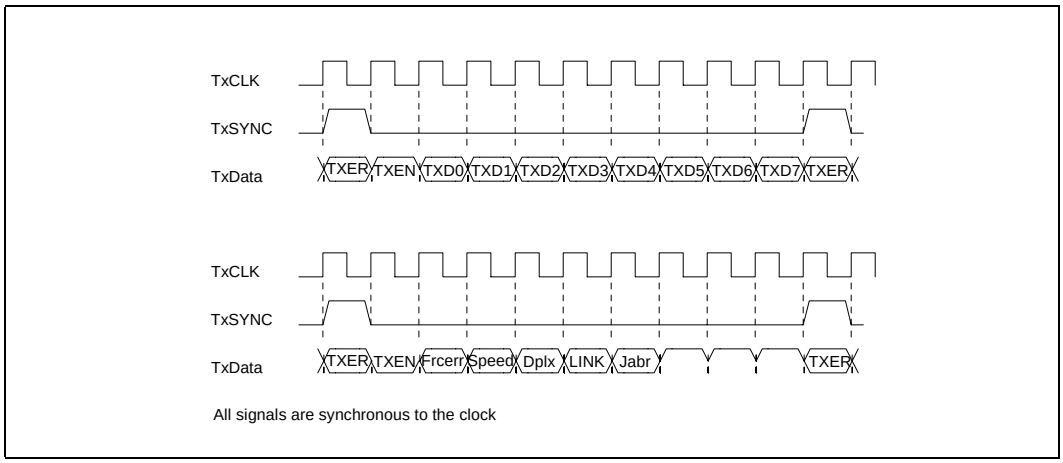
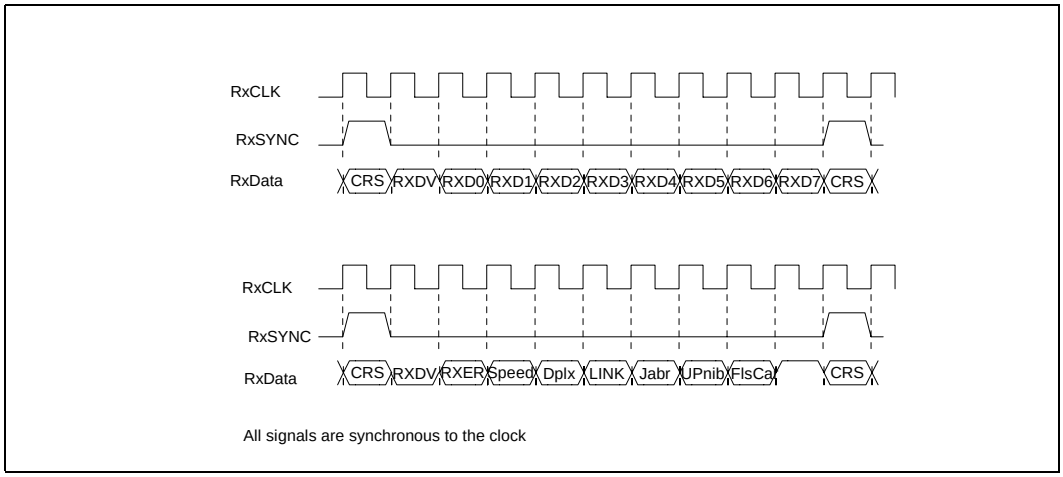


Figure 23 SS-SMII Receive Timing



4.8 RMII Operation

The LXT9785/LXT9785E provides an independent Reduced MII port for each network port. Each RMII uses four signals to pass received data to the MAC: RxData*n*<1:0>, RxER*n*, and CRS_DV*n* (where *n* reflects the port number). Three signals are used to transmit data from the MAC: TxData*n*_<1:0> and TxEN*n*. Both receive and transmit signals are clocked by REFCLK. Data transmission across the RMII is implemented in di-bit pairs which equal a 4-bit wide nibble.

Note: The BGA15 package does not support the RMII interface.

4.8.1 RMII Reference Clock

The LXT9785/LXT9785E requires a 50 MHz reference clock (REFCLK). The device samples the RMII input signals on the rising edge of REFCLK and drives RMII output signals on the falling edge.

4.8.2 Transmit Enable

TxEN*n* must be asserted and de-asserted synchronously with REFCLK. The MAC must assert TxEN*n* at the same time as the first nibble of preamble. TxEN*n* must be de-asserted after the last bit of the packet.

4.8.3 Carrier Sense & Data Valid

The LXT9785/LXT9785E asserts CRS_DV*n* when it detects activity on the line. However, RxData*n* outputs zeros until the received data is decoded and available for transfer to the controller.

4.8.4 Receive Error

Whenever the LXT9785/LXT9785E receives an error symbol from the network, it asserts RxER*n*. When it detects a bad Start-of-Stream Delimiter (SSD) it drives a “10” jam pattern on the RxData pins to indicate a false carrier event.

4.8.5 Out-of-Band Signaling

The LXT9785/LXT9785E has the capability of encoding status information in the RxData stream during IPG. See 4B/5B Coding Operations

The 100BASE-X protocol specifies the use of a 5-bit symbol code on the network media. However, data is normally transmitted across the RMII interface in 2-bit nibblets or “di-bits”. The LXT9785/LXT9785E incorporates a parallel/serial converter that translates between di-bit pairs and 4-bit nibbles, and a 4B/5B encoder/decoder circuit that translates between 4-bit nibbles and 5-bit symbols for the 100BASE-X connection. Figure 24 shows the data conversion flow from nibbles to symbols. Table 46 on page 142 shows 4B/5B symbol coding (not all symbols are valid).

Figure 24 RMII Data Flow

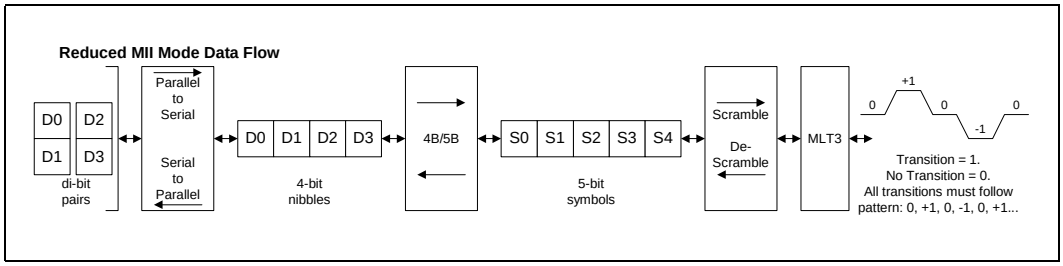


Figure 25 Typical RMII Interface

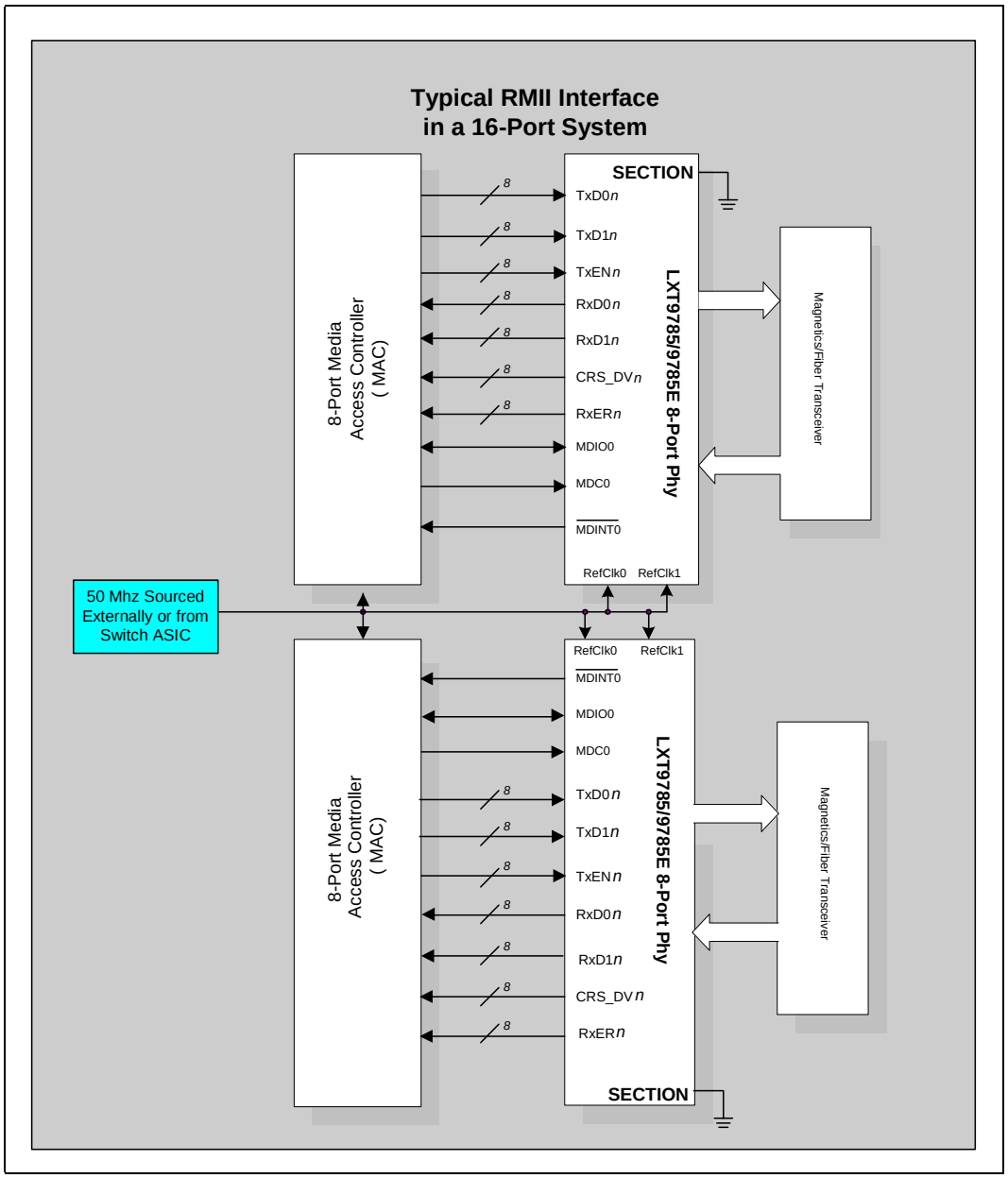
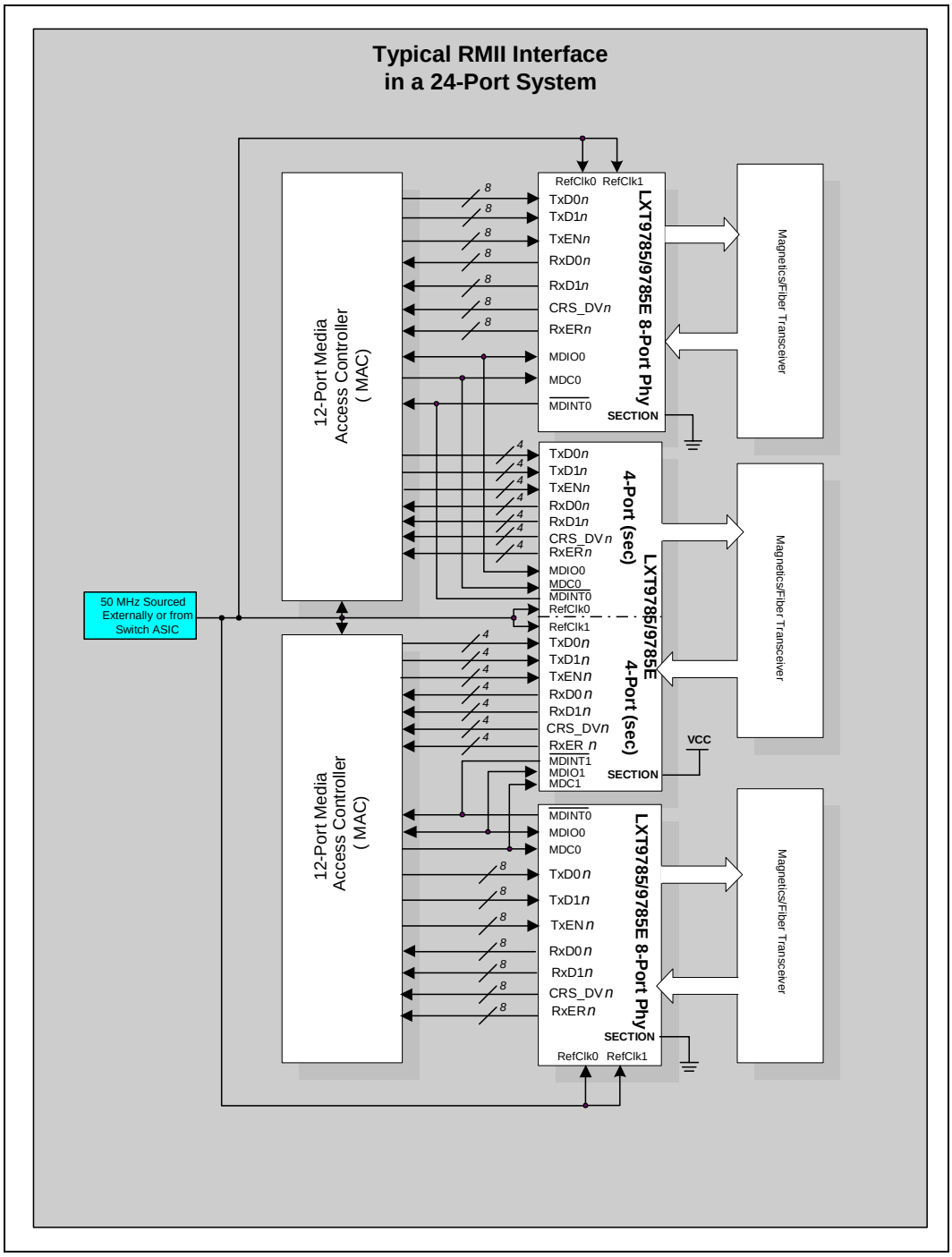


Figure 26 Typical RMII Quad Sectionalization



4.9 100 Mbps Operation

4.9.1 100BASE-X Network Operations

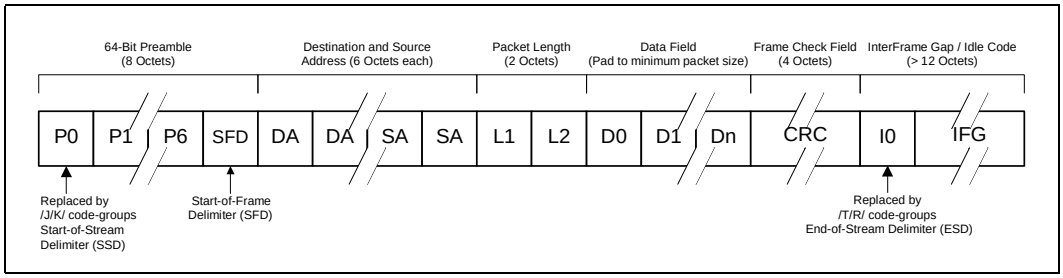
During 100BASE-X operation, the LXT9785/LXT9785E transmits and receives 5-bit symbols across the network link. Figure 27 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT9785/LXT9785E sends out Idle symbols on the line.

In 100BASE-TX mode, the device scrambles the data and transmits it to the network using MLT-3 line code. The MLT-3 signals received from the network are de-scrambled and decoded, and sent across the RMII to the MAC.

In 100BASE-FX mode, the LXT9785/LXT9785E transmits and receives NRZI signals across the LVPECL interface. An external 100BASE-FX transceiver module is required to complete the fiber connection.

As shown in Figure 27, the MAC starts each transmission with a preamble pattern. As soon as the LXT9785/LXT9785E detects the start of preamble, it transmits a J/K Start-of-Stream Delimiter (SSD) symbol to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the Start-of-Frame Delimiter (SFD), packet data, and CRC. Once the packet ends, the LXT9785/LXT9785E transmits the T/R End-of-Stream Delimiter (ESD) symbol and then returns to transmitting Idle symbols.

Figure 27 100BASE-X Frame Format



4.9.2 100BASE-X Protocol Sublayer Operations

In a 7-layer communications model, the LXT9785/LXT9785E is a Physical Layer 1 (PHY) device. The LXT9785/LXT9785E implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u specification. The following paragraphs discuss the LXT9785/LXT9785E operation from the reference model point of view.

4.9.2.1 PCS Sublayer

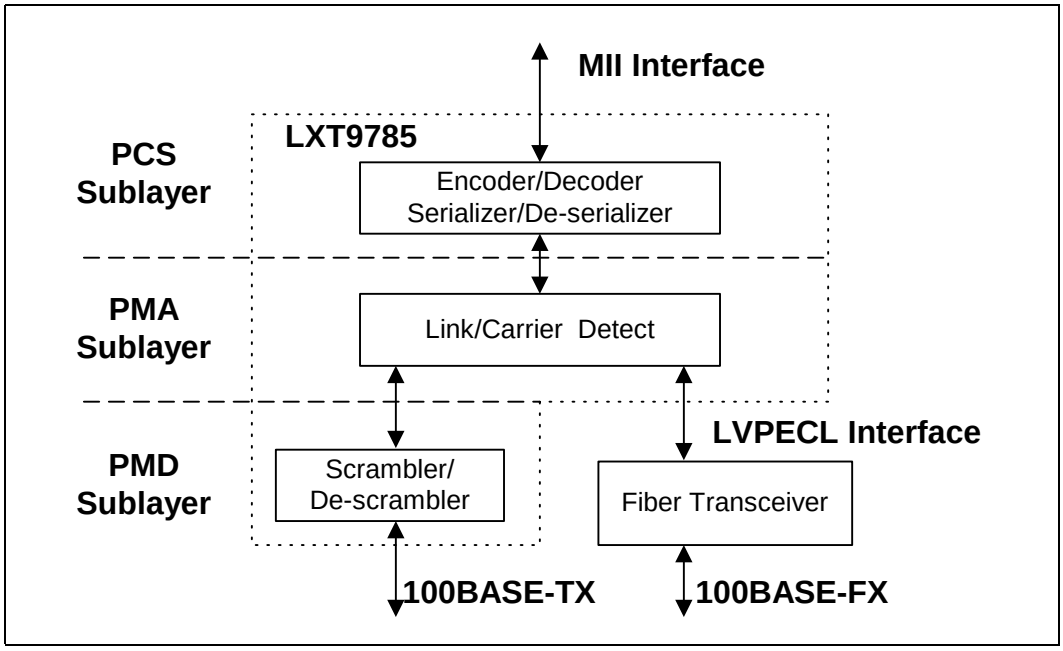
The Physical Coding Sublayer (PCS) provides the RMII interface, as well as the 4B/5B encoding/decoding function. For 100BASE-TX and 100BASE-FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TxEN is de-asserted. For 10T operation, the PCS layer merely provides a bus interface and serialization/de-serialization function. 10T operation does not use the 4B/5B encoder.

4.9.2.1.1 Preamble Handling

When the MAC asserts TxEN, the PCS substitutes a /J/K/ symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the RMII. The PCS layer continues to encode the remaining RMII data until TxEN is de-asserted (see Table 46 on page 142). It then returns to supplying IDLE symbols to the line driver.

The PCS layer performs the opposite function in the receive direction by substituting two preamble nibbles for the SSD.

Figure 28 Protocol Sublayers



4.9.3 PMA Sublayer

The 100BASE-X PMA protocol uses the 4B/5B data encoding scheme to encode/decode the data streams. The coding scheme is shown in Table 46.

Table 46 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

Table 46 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	0 1 1 0	6	0 1 1 1 0	Data 6
DATA	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Idle. Used as inter stream fill code.
	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2.
CONTROL	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2.
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2.
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2.
	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors.
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
INVALID	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

4.9.3.1 Link

In 100 Mbps mode, the LXT9785/LXT9785E establishes a link whenever the descrambler becomes locked and remains locked for approximately 50 ms. Whenever the descrambler loses lock (<16 consecutive idle symbols during a 2 ms window), the link is taken down. This provides a robust link, filtering out any small noise hits that may otherwise disrupt the link. Furthermore, 100 Mbps idle patterns will not bring up a 10 Mbps link.

The LXT9785/LXT9785E reports link failure via the Register status bits (1.2, 17.10, and 19.4) and interrupt functions. If auto-negotiate is enabled, link failure causes the device to re-negotiate.

4.9.3.2 Link Failure Override

The LXT9785/LXT9785E normally transmits 100 Mbps data packets or Idle symbols only if it detects the link is up, and transmits only FLP bursts if the link is not up. Setting bit 16.14 = 1 overrides this function, allowing the LXT9785/LXT9785E to transmit data packets even when the link is down. This feature is provided as a diagnostic tool.

Note: Auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT9785/LXT9785E automatically begins transmitting FLP bursts if the link goes down.

4.9.3.3 Carrier Sense/Data Valid (RMII)

The LXT9785/LXT9785E asserts CRS_DV whenever the respective port receiver is in a non-idle state (as defined by the RMII Specification Revision 1.2), including false carrier events. Assertion of CRS_DV is asynchronous with respect to REFCLK. In the event that signal decoding is not complete when CRS_DV is asserted, the LXT9785/LXT9785E outputs 00 on the RxData1:0 lines until the decoded data are available.

When the line returns to an idle state, CRS_DV is de-asserted synchronously with respect to REFCLK. If the FIFO still contains data to be passed to the MAC via the RMII when CRS is de-asserted, CRS_DV toggles on nibble boundaries until the FIFO is empty. For 100BASE-X signals, CRS_DV toggles at 25 MHz. For 10BASE-T signals, CRS_DV toggles at 2.5 MHz.

4.9.3.4 Carrier Sense (SMII)

For 100BASE-TX and 100BASE-FX links, a Start-of-Stream Delimiter (SSD) or /J/K/ symbol pair causes assertion of carrier sense (CRS). An End-of-Stream Delimiter (ESD), or /T/R/ symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R/. In this event, receive error is indicated during the IPG until the next packet is received.

For 10T links, CRS assertion is based on receipt of valid preamble, and de-assertion on receipt of an End-of-Frame (EOF) marker.

4.9.3.5 Receive Data Valid (SMII)

The LXT9785/LXT9785E asserts the RX_DV bit when it receives a valid packet. However, RxData outputs zeros until the received data are decoded and available for transfer to the controller.

4.9.3.6 Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides the signal scrambling and descrambling, line coding and decoding (MLT-3 for 100BASE-TX, Manchester for 10T), as well as receiving, polarity correction, and baseline wander correction functions.

4.9.3.6.1 Scrambler/Descrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, non-data-dependent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

The scrambler/descrambler can be bypassed by setting Register bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scrambler bypass is provided for diagnostic and test support.

4.9.3.6.2 Baseline Wander Correction

The LXT9785/LXT9785E provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is, by definition, “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander may cause receiver errors, particularly in less robust designs, at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent.

The LXT9785/LXT9785E baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

4.9.3.6.3 Polarity Correction

The LXT9785/LXT9785E automatically detects and corrects for the condition where the receive signal (TPFIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses or four inverted End-of-Frame (EOF) markers are received consecutively. If link pulses or data are not received by the maximum receive time-out period, the polarity state is reset to a non-inverted state. Before the polarity switch occurs, every frame is inverted and causes RxER to assert. The specific number of RxER events observed depends on how many link pulses occur between packets.

4.9.3.7 Fiber PMD Sublayer

The LXT9785/LXT9785E provides an LVPECL interface for connection to an external 3.3 V or 5 V fiber transceiver. (The external transceiver provides the PMD function for the optical medium.) The LXT9785/LXT9785E uses a 125 Mbaud NRZI format for the fiber interface, and does not support 10BASE-FL applications.

Note: The BGA15 package does not support fiber interface.

4.9.3.7.1 Far End Fault Indications

The LXT9785/LXT9785E Signal Detect pins independently detect signal faults from the local fiber transceivers via the SD pins. The device also uses Register bit 1.4 to report Remote Fault indications received from its link partner. The device “ORs” both fault conditions to set bit 1.4. Register bit 1.4 is set once and clears when read.

The far-end fault detection process in fiber operation requires idles to establish link. Link will not establish if a far-end fault pattern is the initial signal detected.

Either fault condition causes the LXT9785/LXT9785E to drop the link unless Forced Link Pass is selected (16.14 = 1). Link down condition is then reported via interrupts and status bits.

In response to locally detected signal faults (SD activated by the local fiber transceiver), the affected port can transmit the far end fault code if fault code transmission is enabled by Register bit 16.2.

- When Register bit 16.2 = 1, transmission of the far end fault code is enabled. The LXT9785/LXT9785E transmits far end fault code if fault conditions are detected by the Signal Detect pins.

- When Register bit 16.2 = 0, the LXT9785/LXT9785E does not transmit far end fault code. It continues to transmit idle code and may or may not drop link depending on the setting for Register bit 16.14.

The occurrence of a Far End Fault causes all transmission of data from the Reconciliation Sublayer to stop and the Far End fault code to begin. The Far End Fault code consists of 84 ones's followed by a single "0" and is repeated until the Far End Fault condition is removed.

4.10 10 Mbps Operation

The LXT9785/LXT9785E operates as a standard 10BASE-T transceiver and supports all the standard 10 Mbps functions. During 10BASE-T (10T) operation, the LXT9785/ LXT9785E transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the device sends out link pulses on the line.

In 10T mode, the polynomial scrambler/descrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT9785/LXT9785E and sent across the MII to the MAC.

Note: The LXT9785/LXT9785E does not support fiber connections at 10 Mbps.

4.10.1 Preamble Handling

The LXT9785/LXT9785E offers two options for preamble handling, which are selected by Register bit 16.5. In 10BASE-T mode, when Register bit 16.5 = 0, the device strips the preamble off the received packets. In RMII and the SMII modes, the CRS signal is asserted based upon receive activity. In the SMII modes, Out-of-Band (OOB) signaling is present until the SFD is output. The DV signal is initially asserted in the frame that the SFD is output. In RMII mode, zeros are output after receive activity is detected until the SFD is output. The packet is output following the SFD.

When Register bit 16.5 = 1 in 10BASE-T mode, the LXT9785/LXT9785E passes the preamble through the RMII and the SMII interfaces. In RMII and the SMII modes, the CRS signal is asserted based upon receive activity. In the SMII modes, OOB signaling is continued until preamble is available from the receive FIFO. After the preamble, the SFD is output with the initial assertion of the DV signal. The RMII interface outputs zeros after receive activity is detected until preamble is available from the FIFO. The number of zero nibbles output before preamble is based upon the FIFO initial fill settings (Register bits 18.15:14). The preamble is followed by the SFD and the packet body. Register bit 16.5 has no effect in 100 Mbps operation.

4.10.2 Dribble Bits

The LXT9785/LXT9785E device handles dribble bits in all modes. If one through four dribble bits are received, the nibble is passed across the RMII. If five through seven dribble bits are received, the second nibble is not sent onto the RMII bus.

4.10.3 Link Test

The LXT9785/LXT9785E always transmits link pulses in 10T mode. When enabled, the link test function monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continue. If link pulses stop, the data transmission is disabled.

If the link test function is disabled, the LXT9785/LXT9785E transmits to the connection regardless of detected link pulses. The link test function is disabled by setting Register bit 16.14 = 1.

4.10.3.1 Link Failure

Link failure occurs if Link Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT9785/LXT9785E returns to the auto-negotiation phase if auto-negotiation is enabled.

4.10.4 Jabber

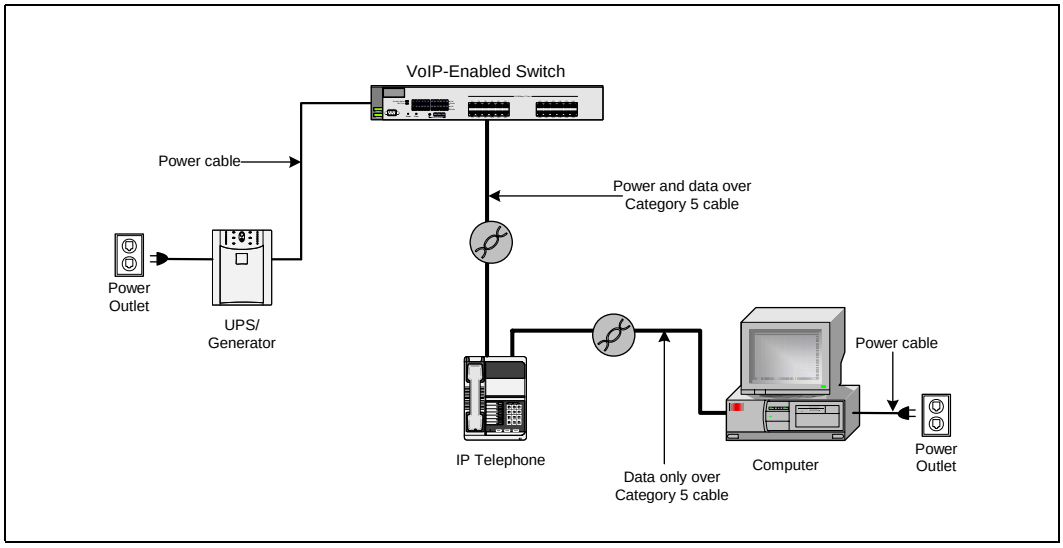
If a transmission exceeds the jabber timer, the LXT9785/LXT9785E disables the transmit and loopback functions and the Collision Status bit (Register bit 17.11) is set regardless of duplex. The jabber timer, according to the IEEE standard, must be between 20 ms to 150 ms. The RMII does not include a Jabber pin, but the MAC may read Register 1 to determine jabber status. The LXT9785/LXT9785E automatically exits jabber mode after the unjab time expires. This function is disabled by setting Register bit 16.10 = 1.

4.11 DTE Discovery Process

The DTE discovery process is port dependent and must be enabled through software. The process is implemented as a next page option to the auto-negotiation flow. When the process is enabled, manual control of auto-negotiation next pages is not allowed. This feature applies to the LXT9785E transceiver only.

The process depends upon an IP phone, or any other DTE capable of being powered remotely, having a specific filter that passes NLPs and FLPs. This filter should be non-polarized to insure that the latest status of Auto-MDIX operation does not effect operation. This filter attenuates 100 Mbps MLT3 signals and 10 Mbps Manchester-encoded signals, and must be bypassed when power is applied to the IP phone. Figure 29 shows a typical IP telephone system connection.

Figure 29 Typical IP Telephone System Connection



4.11.1 Definitions

The terms in Table 47 are used throughout the DTE discovery sections:

Table 47 DTE Terms

Term	Definition
Negotiation Process:	This includes auto-negotiation and parallel detection processes
System:	The switch system using the LXT9785E for DTE Discovery
Link Partner:	A device connected to the LXT9785E through twisted pair cables
DTE:	Data Terminal Equipment; any end-of-link partner
Standard Link Partner:	A link partner that is not requiring power over a Category 5 cable; typically a PC
Remote-Power DTE:	Data Terminal Equipment requiring power over a Category 5 cable; typically an IP telephone
Discovery:	The process of identifying the type of link partner present

4.11.2 Interaction between Processor, MAC, and PHY

The state machines that control the mechanics of the Discovery process reside within the LXT9785E device. However, control of the power supply and overall system control reside in the system processor. The processor communicates with the power supply unit (PSU) and switches it on and off dependant on the data that is supplied by the PHY. The PHY register data is read by the MAC using the MDIO interface. The required control bits are contained in the PHY device register map and are discussed in detail in the section labeled Section 4.11.3, *Management Interface and Control*, on page 149.

Note: The details of the processor/MAC interface and the processor/PSU interface are implementation specific and therefore are out of the scope of this specification.

The following is an overview of the system control for a successful Remote-Power DTE discovery:

1. The discovery process is enabled by the DTE Discovery Process Enable (Dis_EN) Register bit 27.6 and the Auto-Negotiation Enable Register bit 0.12. Writing Register bit 27.6 immediately affects the Auto-Negotiation Base Page. If already enabled, auto-negotiation should be restarted after this bit is written to ensure proper operation. Register bit 4.15 is used for manual control of auto-negotiation next pages and should be left in the default state (cleared).
2. The LXT9785E PHY then tests to see if a Remote-Power DTE is present as the link partner. If a Remote-Power DTE is found, the Power Enable (Power_EN) Register bit 27.4 is set. The processor polls this signal via the MAC.
3. Upon detecting a Remote-Power DTE, the processor instructs the power supply to switch on. Once power has been applied to the DTE, normal negotiation takes place. The processor must enable the required negotiation process by restarting auto-negotiation, or by setting forced speed mode after power has been applied. The processor must poll the link-up Register bit 1.2 for the corresponding LXT9785E port, or the link status change interrupt, to ensure that the link has been established.
4. A time-out must be connected with this feature so that if link is not established within a pre-determined time period (system dependant), the processor instructs the power supply to switch off. If link is not established prior to the expiration of the “link fail inhibit timer”, the LXT9785E restarts negotiation with DTE detection if auto-

negotiation mode was used to establish link with the phone, and the DTE process is still enabled. The LXT9785E restarts negotiation without DTE detection if either forced speed mode is used to establish link with the phone, or the DTE process is disabled.

5. If power is applied and link is established, the system must still poll the Link Status Register bit 1.2 for the corresponding LXT9785E port or the link status change interrupt. This is required since link status is the only way to know when the Remote-Power DTE is removed or unplugged. On seeing the Link_Down condition, the processor instructs the power supply to switch off, and the DTE Discovery begins again or is disabled.

4.11.3 Management Interface and Control

The management and control of the DTE discovery process is via the MDIO port. Each port on the LXT9785E is capable of running the discovery process, thus each port is independently controlled. This is achieved by each port having a dedicated set of control and status bits. These bits are found in Register 27 as follows:

DTE DISCOVERY PROCESS ENABLE - Register Bit 27.6 (Dis_EN)
R/W Default value = 0: Disabled.

Register bit 27.6 controls the operation of the process. The discovery process is disabled when Register bit 27.6 = 0, and enabled when Register bit 27.6 = 1. The MAC controller sets Register bit 27.6 to a 1 when a port search for a DTE requiring power is desired. Once set, Register bit 27.6 remains = 1 until the MAC clears it, either by directly clearing it or by resetting the PHY. This allows the discovery process to continue to function if unsuccessful in detecting a DTE, without being continually re-enabled by the MAC. If Register bit 27.6 is set after link is established, no action is taken until after the link goes down.

POWER ENABLE - Register Bit 27.4 (Power_EN)
R Default value = 0: No Remote-Power DTE found.

Register bit 27.4 contains the result of the discovery process. When Register bit 27.4 = 0, the discovery process has not found Remote-Power DTE, and when Register bit 27.4 = 1, the discovery process has potentially found a DTE requiring power. This indicates power should be applied to the Category 5 cable. Register bit 27.4 is polled by the MAC during the discovery process, and is cleared when the PHY is reset, when auto-negotiation is restarted, or when auto-negotiation is disabled. In the event of a discovery process being interrupted due to detection of an already powered link partner (auto-negotiation completion or Parallel Detection), Register bit 27.4 = 0.

STANDARD LINK PARTNER DETECTED - Register Bit 27.3 (SLP_Det)
R/W Clear on Read Default value = 0: No link partner found.

When Register bit 27.3 = 1, a standard link partner has been detected by the LXT9785E (NLPs, MLT3 data, FLPs without next page support, or FLPs with non-matching next pages). This indicates power should not be applied to the Category 5 cable. When Register bit 27.3 = 0, other bits are checked to determine overall status of the link partner. Register bit 27.3 is cleared on read, or DTE discovery is disabled, link is established, or auto-negotiation is either restarted or disabled.

LINK FAIL TIMEOUT - Register Bit 27.2 (LFIT Expired)
R/W Clear on Read Default value = 0 (Link Fail Inhibit timer has expired without establishment of link with a standard link partner). Valid only when Standard Link Partner Detected Register bit 27.3 = 1.

Register bit 27.2 is set if link is not established prior to the Link Fail Inhibit Timer expiring. This indicates that the Discovery process has restarted and the Standard Link Partner Detected Register bit may no longer be valid. Register bit 27.2 is cleared on read, or DTE discovery is disabled, link is established, or auto-negotiation is either restarted or disabled.

4.11.4 DTE Discovery Process Flow

The following section describes the DTE Discovery process.See Figure 30, *Cortina Systems® LXT9785E Negotiation Flow Chart*, on page 152 for a flow chart of the discovery process.When DTE Discovery (27.6) and auto-negotiation (0.12) are enabled (auto-negotiation mode is required), the LXT9785E transmits the auto-negotiation base page with the next page ability bit set (Section Table 88, *Auto-Negotiation Advertisement Register (Address 4)*, on page 195).

System software polls Register 27 to determine if or when a Remote-Power DTE is detected. The receiver monitors the line to determine if NLPs, MLT3 data, or FLP bursts are being received. If the receive activity is FLP bursts, the status of the next page ability bit is checked. If the detected “link partner” also supports next page, then the LXT9785E transmits out the next page sequence associated with message code #5 (Organizationally Unique Identifier (OUI) Tag Code). The definition for the next pages to be sent out for this message code include some user-defined code values. These values are loaded with randomly created data from an internal LSFR that is free running and seeded with the PHY address of the LXT9785E port. The Next Pages are hard coded in the logic (the LXT9785E ignores any data written into Register 7) and are outlined in Table 48. The receiver monitors the next pages to determine that the exact next page data (especially the random data) transmitted is received. As soon as the first non-matching next page is detected, the DTE Discovery process is stopped and the base page is used to determine the capability options. The Power-Enable Register bit 27.4 is set when a Remote-Power DTE is detected as the link partner, and the last next page is repeatedly transmitted until software restarts the required negotiation process (auto-negotiation or forced-speed mode).

The software should be written so that the negotiation is not restarted until the DTE has been powered up over the Category 5 cable. The Power-Enable Register bit 27.4 is cleared upon restarting or disabling auto-negotiation (selecting forced mode). The system must be able to detect over-current conditions and be capable of disabling power in case the link partner is not a Remote-Power DTE. Some examples of devices that would mistakenly set Power-Enable Register bit 27.4 are a token-ring balun and a loopback cable. Once link partner power has been stabilized and sufficient time has passed for the link partner to initialize, the auto-negotiation process may be restarted.

The negotiation process establishes link if a compatible mode exists between the LXT9785E and the link partner. If a compatible mode does not exist (not compatible or not established within the Link Fail Inhibit Timer period), the LXT9785E either restarts auto-negotiation/DTE discovery (discovery is enabled (27.6=1) and auto-negotiation is enabled (0.12 = 1)), or normal negotiation (discovery is disabled (27.6=0) and auto-negotiation is enabled (0.12 = 1)), or either 10 Mbps or 100 Mbps forced-mode operation (auto-negotiation is disabled (0.12 = 0)). The software must detect this non-link state and disable power.

Table 48 Next Page Message #5 Code Word Definitions

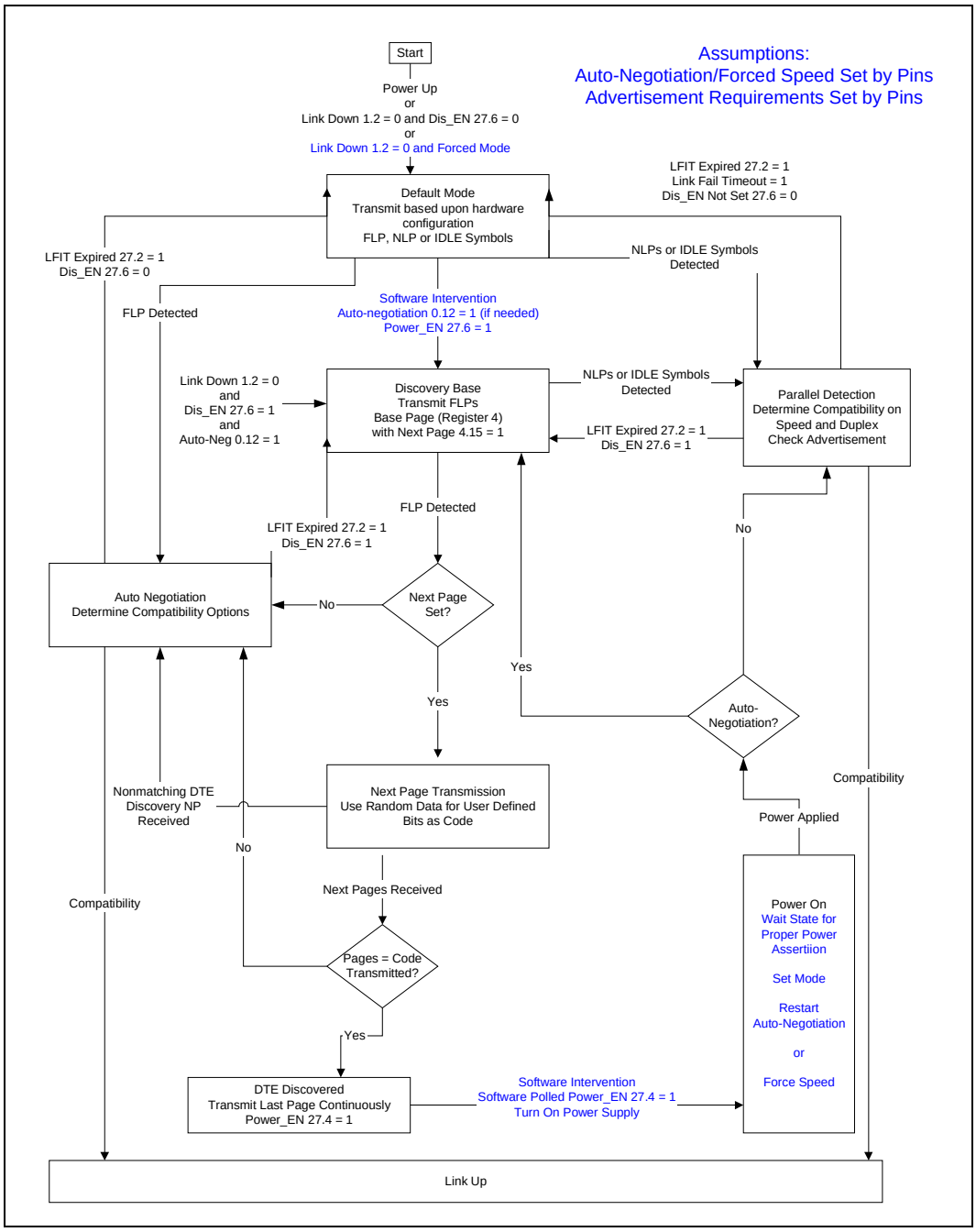
Next Page Encoding	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OUI Tagged Message	1	a	1	0	t	0	0	0	0	0	0	0	0	1	0	1
User Page 1	1	a	0	0	t	3.10	3.11	3.12	3.13	3.14	3.15	2.0	2.1	2.2	2.3	2.4
User Page 2	1	a	0	0	t	2.5	2.6	2.7	2.8	2.9	2.10	2.11	2.12	2.13	2.14	2.15
User Page 3	1	a	0	0	t	0	0	L.8	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0
User Page 4	1	a	0	0	t	L.10	L.9	L.8	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0

1. a is the acknowledge bit; t is the toggle bit; L is the LFSR

4.11.5 DTE Discovery Behavior

The device behavior checks the comparison bit after each next page is successfully auto-negotiated. If the first next page or any subsequent next page does not match, the DTE Discovery process transmits one last null page with the next page bit cleared to stop the DTE Discovery process. If each page is successfully auto-negotiated (it matches the transmitted page), DTE Discovery completes as previously described. The five Next Pages consist of a message page and four user pages.

Figure 30 Cortina Systems® LXT9785E Negotiation Flow Chart



4.12 Monitoring Operations

4.12.1 Monitoring Auto-Negotiation

Auto-negotiation may be monitored as follows:

- Bits 1.2 and 17.10 = 1 once the link is established.
- Additional bits in Register 1 (refer to Table 85, *Status Register (Address 1)*, on page 193) and Register 17 (refer to Table 94, *Quick Status Register (Address 17, Hex 11)*, on page 200) can be used to determine the link operating conditions and status.

4.12.2 Per-Port LED Driver Functions

The LXT9785/LXT9785E incorporates three direct drive LEDs per port (LED*n*_1_L, LED*n*_2_L, and LED*n*_3_L).

On power up, all the LEDs lights up for approximately one second after reset de-asserts. Each LED may be programmed to one of several different display modes using the LED Configuration Register. Each per-port LED may be programmed (refer to Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204) to indicate one of the following conditions:

- Operating Speed
- Transmit Activity
- Receive Activity
- Collision Condition
- Link Status
- Duplex Mode
- Isolate Condition

The LEDs can also be programmed to display various combined status conditions. For example, setting bits 20.15:12 = 1101 produces the following combination of Link and Activity indications:

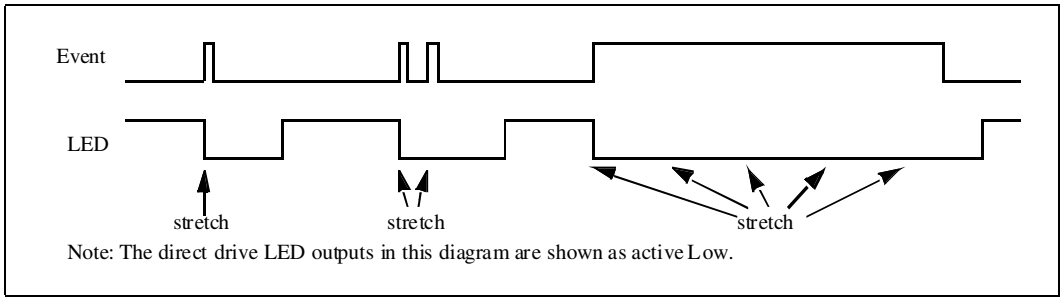
- If Link is down, LED is off.
- If Link is up, LED is on.
- If Link is up AND activity is detected, the LED blinks at the stretch interval selected by bits 20.3:2 and continues to blink as long as activity is present.

The LED driver pins are open drain circuits (10 mA max current rating). Refer to Section 5.2.6, *LED Circuit*, on page 164 under the Application Information Section for LED circuit design details. The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. If during this pulse stretch period, the event occurs again, the pulse stretch time is further extended (see Table 97, *LED Configuration Register (Address 20, Hex 14)*, on page 204).

When an event such as receiving a packet occurs, it is edge detected and starts the stretch timer. The LED driver remains asserted until the stretch timer expires. If another event occurs before the stretch timer expires, the stretch timer is reset and the stretch time extended.

When a long event (such as duplex status) occurs, it is edge detected and starts the stretch timer. When the stretch timer expires, the edge detector is reset so that a long event causes another pulse to be generated from the edge detector. The edge detector resets the stretch timer, causing the LED driver to remain asserted. Figure 31 on page 154 shows how the stretch operation functions.

Figure 31 LED Pulse Stretching



4.12.3 Out-of-Band Signaling

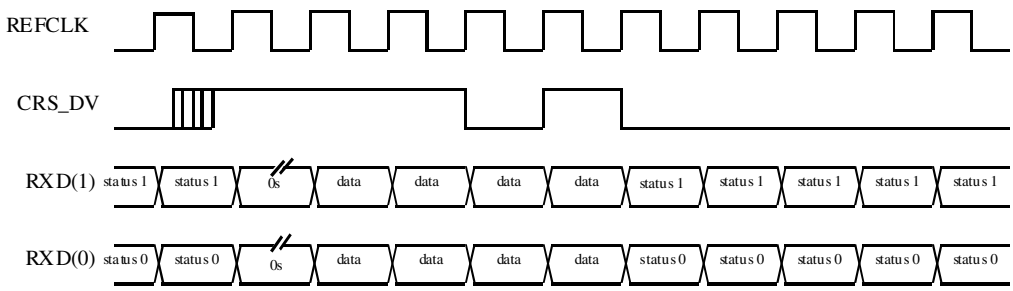
The LXT9785/LXT9785E provides an out-of-band signaling option to transfer status information across the RMII receive interface. This feature is enabled when Register bit 25.0 = 1 and uses the RxData(1:0) data bus during the Inter-Packet Gap (IPG) time as shown in Figure 32. Out-of-Band signaling is disabled when Isolate mode is enabled by setting Register 0.10.

Note: The BGA15 package does not support Out-of-Band Signaling nor the RMII interface.

The two status bits transferred across the RxData bus are software selectable via Register 25 (see Table 99, *RMII Out-of-Band Signaling Register (Address 25, Hex 19)*, on page 206).

In normal operation, the LXT9785/LXT9785E stuffs the RxData bus with zeros during the IPG. A software-selectable bit enables the RMII out-of-band signaling feature. Once this bit is set, the LXT9785/LXT9785E replaces the zeros with selected status bits during the IPG.

Figure 32 RMII Programmable Out-of-Band Signaling



1. When network activity is detected, the LXT9785/LXT9785E asserts CRS_DV asynchronously with respect to REFCLK.
2. After CRS_DV is asserted, the LXT9785/LXT9785E zero-stuffs the RxData bits until the received data has been processed through the FIFO.
3. When network activity ceases, the LXT9785/LXT9785E de-asserts CRS_DV synchronously with respect to REFCLK. CRS_DV toggles until all data in the FIFO has been processed through the RMII. Once the FIFO is empty, LXT9785/LXT9785E drives the status bits selected by the Out-of-Band Signaling Register (refer to Table 99, *RMII Out-of-Band Signaling Register (Address 25, Hex 19)*, on page 206) on the

The LXT9785/LXT9785E includes an IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible.

4.12.4 Boundary Scan Interface

This interface consists of five pins (TMS, TDI, TDO, TCK and TRST_L). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are internally pulled up and the TCK pin is internally pulled down. TDO does not have an internal pull-up or pull-down.

4.12.5 State Machine

The TAP controller is a 16-state machine driven by the TCK and TMS pins. Upon reset, the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS and TDI are High for five TCK periods.

4.12.6 Instruction Register

The IDCODE instruction is always invoked after the state machine resets. The decode logic ensures the correct data flow to the Data registers according to the current instruction. Valid instructions are listed in Table 50.

4.12.7 Boundary Scan Register

Each Boundary Scan Register (BSR) cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation as listed in Table 49. Refer to the Identification Information section in the Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers Specification Update (document number 249357) for the JTAG ID numbers.

Table 49 BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

Table 50 Supported JTAG Instructions

Name	Code	Description	Data Register
EXTEST	0000 Hex	External Test	BSR
IDCODE	FFFE Hex	ID Code Inspection	ID REG
SAMPLE	FFF8 Hex	Sample Boundary	BSR
High Z	FFCF Hex	Force Float	Bypass
Clamp	FFEF Hex	Clamp	BSR
BYPASS	FFFF Hex	Bypass Scan	Bypass

4.13 Cable Diagnostics Overview

Debugging cable problems increases the overall cost of owning and operating a local area network. Cable Diagnostic tools were incorporated into the LXT9785/LXT9785E device to help customers debug network cable problems. The Cable Diagnostic tools provide the ability to detect severe cable problems, such as open and short circuits, and determine the distance to the discontinuity.

4.13.1 Features

The following are three cases to consider for Cable Diagnostics:

- Distance to a short circuit between wires of a single twisted-pair
- An open circuit
- Detection of an improperly terminated cable by the link partner.

An improperly terminated cable will not meet IEEE 802.3 return loss requirements. Register 29 has been added to control cable testing and report cable testing results.

Cable Diagnostics provides a method to determine the distance to opens and shorts when the link partner is inactive on the twisted-pair under test. The cable tests produce undefined results if the link partner is transmitting signals. Implementation methods may vary depending upon the system use requirements of Cable Diagnostics.

4.13.2 Operation

Cable Diagnostics utilizes the PHY transmit drivers and receivers to test a single twisted-pair. A transmit pulse is driven down the twisted-pair under test and the reflected signal is analyzed. Link partners transmitting NLP, FLP, MLT3, or other TDR pulses may interfere with the ability of the LXT9785/LXT9785E to properly analyze the reflected Cable Diagnostic pulse. Implementation algorithms must take these potential situations into consideration.

4.13.2.1 Short and Long Cable Testing Requirements

Implementing Cable Diagnostic tests, by enabling short and long cable tests sequentially, allows more accurate measurements to a detected fault. Both tests are necessary to reach full precision. The short and long cable tests can be run by writing 0x7400h and 0x6C00h to Register 29, respectively. See Section 4.13.4, *Basic Implementation*, on page 158 for implementation details.

4.13.2.2 Precision

Cable Diagnostics estimates the distance to a fault up to 150 m. Category 5 or better cable produces the most accurate test results. Less than Category 5 cable may produce less accurate results on long cable lengths. Cable Diagnostics returns the distance to the closest fault, if a fault is present.

Cable Diagnostic tests report the distance to a cable fault based on the velocity of signal propagation, which is used to determine the electrical length to the fault. The electrical length may vary slightly from the physical cable length. The measurement accuracy may vary by +/- 2 m. The following basic equation is used to calculate the distance to a fault:

```
Distance_to_Fault = (Reg29[7:0] - 3.5) / 1.16
```

4.13.3 Implementation Considerations

Before performing Cable Diagnostics, the twisted-pair to be tested may be verified to be inactive. All applicable link configurations should be attempted. Cable Diagnostic tests may be started if the attempts indicate no link partners are active. If link partners are detected, additional tests and decisions as to next steps may need to be implemented in the cable testing algorithm to ensure the most accurate results.

Cortina recommends that a 100BASE-TX link be attempted with MDI and MDIX enabled sequentially, prior to performing Cable Diagnostic testing, to determine if a 100BASE-TX-only link partner is present. If a link partner is in forced 100BASE-TX operation, transmitting MLT3, the Cable Diagnostic test result will be undefined due to the interference MLT3 causes in attempting to process the reflected Cable Diagnostic pulse. Auto MDI/MDIX on the link partner should be accounted for in deriving the cable testing algorithm.

Cortina recommends auto MDI/MDIX be disabled when running the cable tests. The transmit and receive twisted-pairs must be tested one at a time with both short and long cable test suites. The MDI/MDIX control bits in Table 100, *Trim Enable Register (Address 27, Hex 1B)*, on page 207 can be used to select the twisted-pair to be tested. This requirement creates a minimum of four test permutations that must be completed to determine if the fault exists, the distance to the fault.

If Cable Diagnostics testing is completed using a powered down LXT9785/LXT9785E device as the link partner, specific results can be expected. The results will indicate an open connection when the PWRDWN hardware configuration pin is used. These power-down methods disable the internal termination resistors to create a high impedance connection equivalent to an open circuit.

If Transmit Disable (Register bit 16.13) or software controlled Power-Down (Register bit 0.11) is used, the powered down device transmit logic will look like an open circuit and the receive circuit will look like a 100 Ω terminated connection. The Transmit Disable bit and the software Power-Down bit disable the transmit circuit but do not affect the receive circuit.

The result of Cable Diagnostic tests using an IP Phone indicate an open or a short fault at a gross approximation of the distance to the IP Phone. The termination resistors are not powered and do not create a proper termination. The filter circuit used by some manufacturers adversely affects the test results.

Transmission and reception of packets is disabled when Cable Diagnostics is enabled. Internal loopback must be disabled for Cable Diagnostics to operate properly. Internal loopback disables the analog interface.

4.13.4 Basic Implementation

Register 29 is used to control and report the Cable Diagnostics test results. The function tests one pair of the twisted-pair cable at a time. The basic process flow is described as follows (see Table 101, *Cable Diagnostics Register (Address 29, Hex 1D)*, on page 209 for Register 29 bit definitions):

1. Disable auto-negotiation by clearing Register bit 0.12, set to MDI by clearing Register bits 27.9:8, and ensure internal loopback is disabled, Register bit 0.14 = 0.
2. Write 0x7400h to Register 29. Setting these bits places the device in short cable Cable Diagnostics mode and forces link to drop. The device waits a specific amount of time (1.2 s to 1.5 s) to ensure link drops on any connected link partner, and initiates the Cable Diagnostics test on the selected twisted-pair.
3. Poll Register bit 29.9. When this bit is set, the test is complete and Register bits 29.7:0 contain a value used to determine if a cable fault was found and the distance to that fault. A value of 0xFFh indicates no fault was found. Any other value indicates a fault was found, that value should be stored for later use.
4. Write 0x6C00h to Register 29. Setting these bits places the device in long cable Cable Diagnostics mode.
5. Poll Register bit 29.9. When set, record the value of Register bits 29.7:0 if a fault is found.
6. If a fault is present, a calculation is used to determine the distance to the fault. Insert the smallest value recorded from Register bits 29.7:0 in steps 3 and 5 above into the following formula:

   ```
   Distance_to_Fault = (Reg29[7:0] - 3.5) / 1.16
   ```

   Register bit 29.8 is set if the fault is detected as a short circuit and is cleared if the fault is detected as an open circuit. Register bits 29.12:11 are cleared when read and are cleared during the same read cycle when Register bit 29.9 is read, indicating a fault condition exists.
7. Normal PHY operation can be resumed by writing 0x4000h to Register 29 or by software or hardware reset. The test suite can be run again by resuming at step 2 above.

4.14 Link Hold-Off Overview

The PHY link is established as soon as the system platform powers-up. In many cases, the system platform is not capable of supporting network operation until configuration firmware is loaded. It is desirable in such cases to prevent the PHY from establishing a link until the system platform is fully configured and ready for network operation. Link Hold-Off was incorporated into the LXT9785/LXT9785E device to satisfy these requirements. Enabling Link Hold-Off disables the PHY Link capability until the system platform is fully capable of supporting network operation. The feature is enabled by hardware control at power-up or software control during normal operation.

4.14.1 Features

Link Hold-Off prevents the LXT9785/LXT9785E from establishing a link by disabling the analog transmit and receive capability. The digital capabilities of the PHY are unaffected including register access and LED operation. Link Hold-Off can be enabled by an external hardware pin for all ports or by software register access for individual ports. When Link Hold-Off is enabled, the transmitter and receiver on the selected ports are forced into software power-down mode (see Section 4.5.3, *Power-Down Mode*, on page 124) to block signal activity from establishing a link and passing packets through the PHY.

The hardware enabled Link Hold-Off is controlled by the LINKHOLD pin. Internal pull-down resistors hold the pin in the inactive state. Connecting a 5k pull-up resistor to the pin enables the feature at power-up reset or external hardware pin Reset. Once a PHY port is programmed as desired, clearing Register bit 0.11 will re-enable that port. Each port must be individually re-enabled.

When a port is software reset, by setting Register 0.15, the state of the hardware configuration pin captured by the last hardware or power-up reset determines the default register values for the specific function for that port. Link Hold-Off, once enabled by hardware configuration, is re-enabled on a port by issuing a software reset for that port. It is not necessary to reset the entire PHY or switch system to re-enable Link Hold-Off.

Link Hold-Off software control is enabled or disabled on individual ports by respectively setting or clearing Register bit 0.11, the power-down bit, during normal operation. It is not required to have previously enabled Link Hold-Off by hardware configuration.

Link Hold-Off is disabled if the external pin MDDIS is active. The MDDIS pin disables the MDIO interface required to re-enable normal transmit and receive link operation. MDDIS is intended to disable the MDIO management interface for unmanaged applications. Internal loopback circuitry is unaffected in Link Hold-Off mode.

4.14.2 Operation

Link Hold-Off is implemented in one of the following two ways:

- Using a hardware pin at power-up or hardware reset
- Using software control through the MII Management (MDC/MDIO) interface.

Link Hold-Off use by an external hardware pin is as follows:

1. Pull the LINKHOLD pin High with a pull-up resistor (approximately 5 k Ohms).
2. Power up the system or drive the reset pin active.
3. All ports are link disabled.
4. Program all ports to the desired configuration.

5. Clear Register Bit 0.11, power-down for each individual port.
6. Normal operation resumes on each port after Register bit 0.11 is cleared (see Table 83 for the recovery time).

Link Hold-Off is enabled on a per port basis by software control using the following two methods:

Method One:

This method requires that Link Hold-Off is enabled by the LINKHOLD pin during the last power-up or hardware reset.

1. Set Register bit 0.15 to reset and re-enable Link Hold-Off for the desired port.
2. Program the PHY to the desired configuration.
3. Clear Register bit 0.11 (power-down) to disable Link Hold-Off.
4. Normal operation resumes.

Method Two:

This method enables Link Hold-Off regardless of the LINKHOLD hardware configuration state.

1. Set Register bit 0.11(power-down) to enable Link Hold-Off for the desired port.
2. Program the PHY to the desired configuration.
3. Clear Register bit 0.11 (power-down) to disable Link Hold-Off.
4. Normal operation resumes.

Note: High is defined by the IO voltage supply level selected (2.5V or 3.3V).

5.0 Application Information

5.1 Design Recommendations

The LXT9785/LXT9785E is designed to comply with IEEE 802.3 requirements to provide outstanding receive Bit Error Rate (BER), and long-line-length performance. To achieve maximum performance from the LXT9785/LXT9785E, attention to detail and good design practices are required. Refer to the Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers Design and Layout Guide application note for detailed design and layout information.

5.2 General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV maximum of noise is considered acceptable. High-frequency switching noise can be reduced, and its effects eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of 0.01µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT9785/LXT9785E and the RJ-45 connectors at the edge of the board.
- Do not extend any circuit power and ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

5.2.1 Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane may cause EMI problems and degrade line performance. The best approach to this problem is to minimize ground noise as much as possible using good general techniques and by filtering the VCC plane. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (32-bits+) running at a high clock rate.
- DC-to-DC converters.

Cortina recommends filtering the power supply to the analog VCC pins of the LXT9785/LXT9785E. This has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT9785/LXT9785E, helping with line performance. Second, if the VCC planes are laid out correctly, digital switching noise is kept away from external connectors, reducing EMI problems.

The recommended implementation is to break the VCC plane into two sections. The digital section supplies power to the VCCD and VCCIO pins of the LXT9785/LXT9785E. The analog section supplies power to the VCCA pins. The break between the two planes should run underneath the device. In designs with more than one the LXT9785/ LXT9785E, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100 Ω impedance at 100 MHz. Beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. A bulk cap (2.2 -10µF) should be placed on each side of each bead.

In addition, a high-frequency bypass cap (0.01 µF) should be placed near each analog VCC pin.

5.2.2 Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes.

- Follow the guidelines in the Cortina Systems® LXT9785 and LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceivers Design and Layout Guide for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPFOP/N and TPFIP/N signals, the magnetics, and the RJ-45 connectors.
- Place the layers so the TPFOP/N and TFPIP/N signals can be routed close to the ground plane. For EMI reasons, it is more important to shield TPFOP/N than TPFIP/N.

5.2.2.1 Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ-45 connectors to the magnetics, and can be used to terminate unused signal pairs (Bob Smith termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2 kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2 kV isolation to the Bob Smith termination.

5.2.3 MII Terminations

Series termination resistors are required on all the SS-SMII output signals driven by the LXT9785/LXT9785E. Special trace layout consideration should be used when using the SMII interface. Keep all traces orthogonal and as short as possible. Whenever possible, route the clock and sync traces evenly between the longest and shortest data routes. This minimizes round-trip, clock-to-data delays and allows a larger margin to the setup and hold requirements.

5.2.4 Twisted-Pair Interface

Use the following standard guidelines for a twisted-pair interface:

- Place the magnetics as close as possible to the LXT9785/LXT9785E.
- Keep transmit pair traces as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.

- Keep the transmit and receive pairs apart to avoid cross-talk.
- Route the transmit pair adjacent to a ground plane. The optimum arrangement is to place the transmit traces two to three layers from the ground plane, with no intervening signals.
- Improve EMI performance by filtering the TPO center tap. A single ferrite bead rated at 400 mA may be used to supply center tap current to all ports.

5.2.4.1 Magnetic Requirements

The LXT9785/LXT9785E requires a 1:1 ratio for both the receive transformers and the transmit transformers. The transmit isolation voltage should be rated at 1.5 kV to protect the circuitry from static voltages across the connectors and cables. The LXT9785/LXT9785E is a current driven transceiver that requires an external voltage (center tap) to drive the transmit signal. In order to support the Auto-MDIX functionality of the LXT9785/LXT9785E, the magnetic must provide a center tap for both the transmit and receive magnetic winding, with both connected to VCCT. See the LXT9785/LXT9785E Design and Layout Guide (249509-001) for magnetic testing with the LXT9785/LXT9785E. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and validate the magnetics for the specific application. Table 51 provides the magnetics requirements.

Table 51 Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1:1	–	–	
Tx turns ratio	–	1:1	–	–	
Insertion loss	0.0	0.6	1.1	dB	
Primary inductance	350	–	–	µH	
Transformer isolation	–	2	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

5.2.5 The Fiber Interface

The fiber interface consists of an LVPECL transmit and receive pair to an external fiber transceiver. Both 3.3 V fiber transceivers and 5 V fiber transceivers can be used with the LXT9785/LXT9785E. See the 100BASE-FX Fiber Optic Transceivers-Connecting a PECL/LVPECL Interface Application Note (document number 250781) for detailed information on fiber interface designs and recommendations for Cortina PHYs.

The following should occur in 3.3 V fiber transceiver applications as shown in Figure 36:

- The transmit pair should be AC-coupled with 2.5 V supplies and re-biased to 3.3 V LVPECL levels
- The transmit pair should contain a balance offset in the pull-up resistors to prevent PHY-to-fiber transceiver crosstalk amplification in power-down, loopback, and reset states (see fiber interface application note)

- The receive pair should be DC-coupled with an emitter current path for the fiber transceiver
- The signal detect pin should be DC-coupled with an emitter current path for the fiber transceiver

Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 36 shows a typical example of an LXT9785/LXT9785E-to-3.3 V fiber transceiver interface.

The following occurs in 5 V fiber transceiver applications as shown in Figure 37:

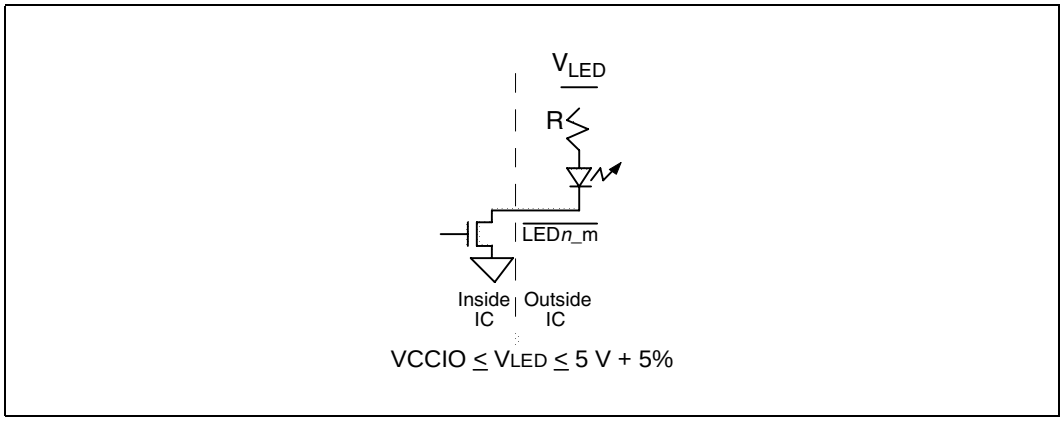
- The transmit pair should be AC-coupled and re-biased to 5 V PECL input levels
- The transmit pair should contain a balance offset in the pull-up resistors to prevent PHY-to-fiber transceiver crosstalk amplification in power-down, loopback, and reset states (see fiber interface application note)
- The receive pair should be AC-coupled with an emitter current path for the fiber transceiver and re-biased to 1.2 V
- The signal detect pin on a 5 V fiber transceiver interface should use the logic translator circuitry as shown in Figure 38.

Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 37 shows a typical example of an LXT9785/LXT9785E-to-5 V fiber transceiver interface, while Figure 38 shows the interface circuitry for the logic translator.

5.2.6 LED Circuit

Each Direct Drive LED has a corresponding open-drain pin. The LEDs are connected through a current-limiting resistor to a positive-voltage rail. The LEDs are turned on when the output pin drives Low. The open-drain LED pins are 5 V tolerant, allowing use of either a 3.3 V or 5 V rail (a 2.5 V rail is unlikely to work with standard forward voltage LEDs). A 5 V rail eases LED component selection by allowing more common, high-forward voltage LEDs to be used. Refer to Figure 33 for a circuit illustration.

Figure 33 LED Circuit



5.3 Typical Application Circuits

Figure 34 through Figure 37 on page 168 show typical application circuits for the LXT9785/LXT9785E. Figure 38 on page 169 shows the interface circuitry for the logic translator.

Figure 34 Power and Ground Supply Connections

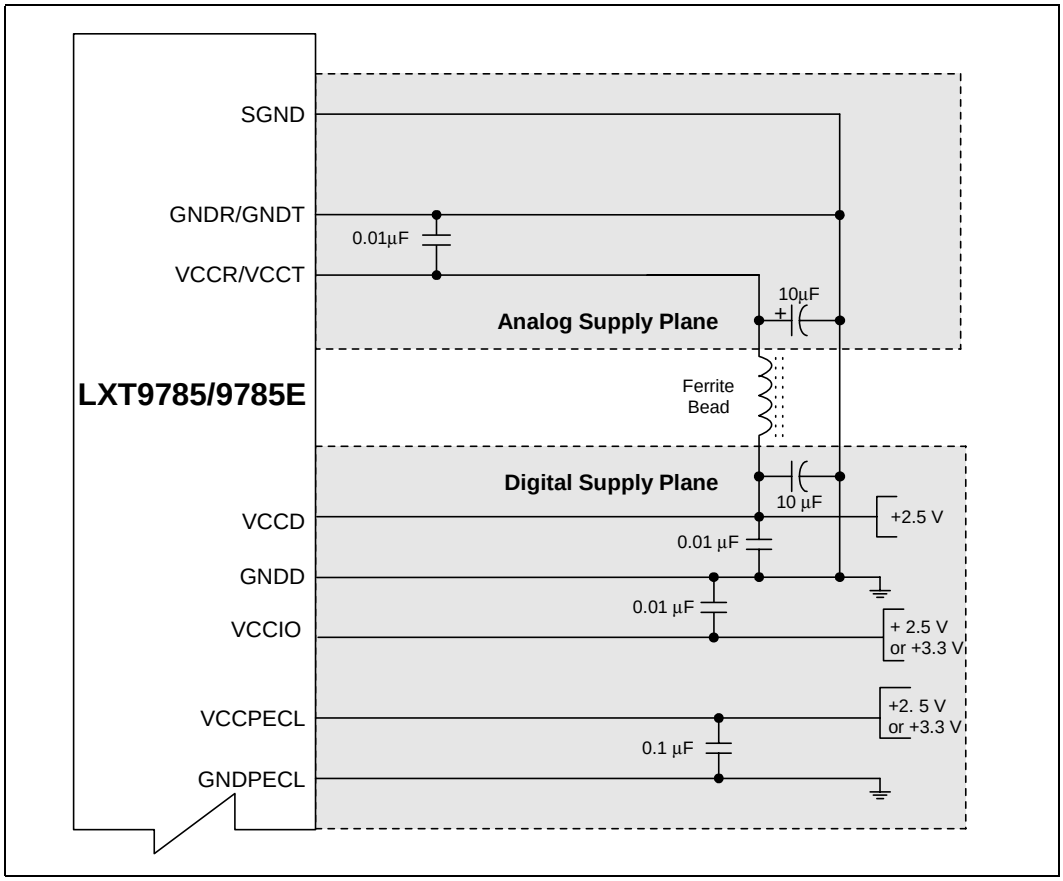
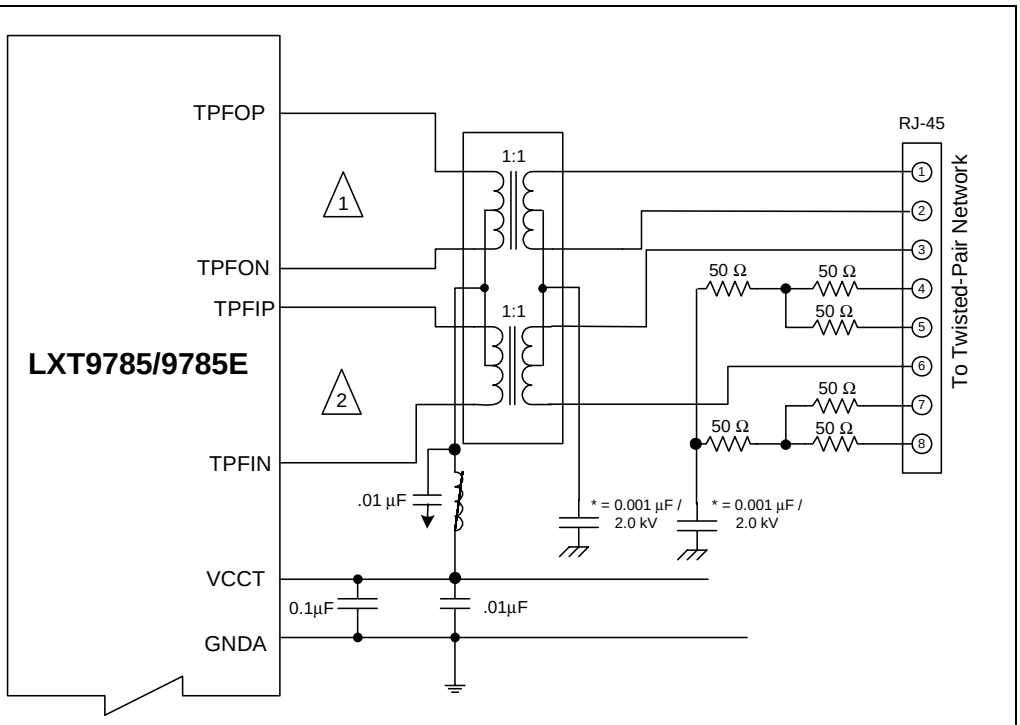
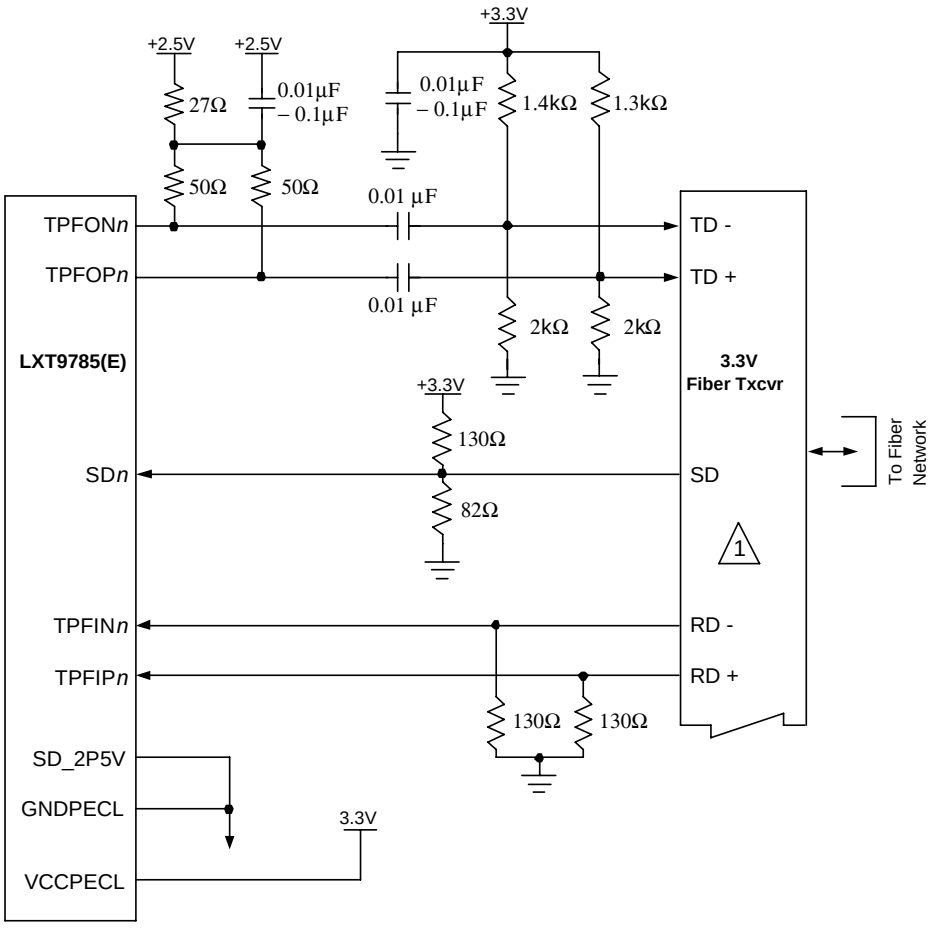


Figure 35 Typical Twisted-Pair Interface



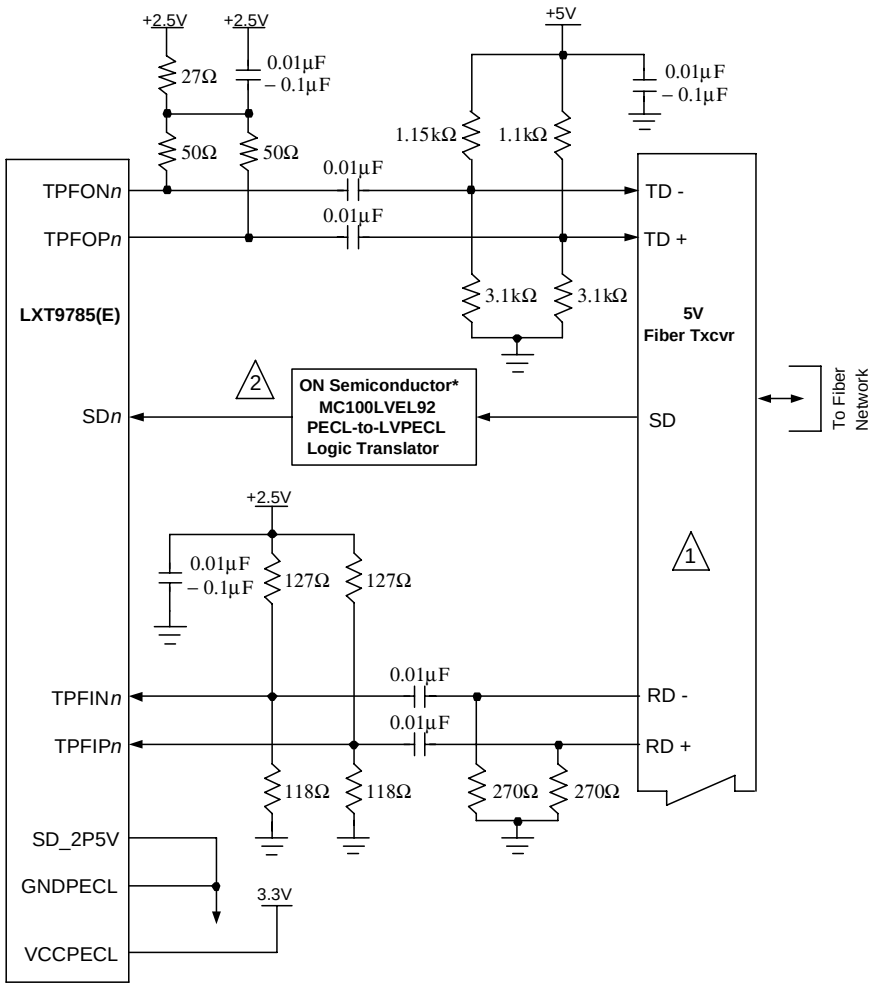
1. The 100 Ω transmit load termination resistor typically required is integrated in the LXT9785/ LXT9785E.
2. The 100 Ω receive load termination resistor typically required is integrated in the LXT9785/

Figure 36 Recommended LXT9785/LXT9785E-to-3.3 V Fiber Transceiver Interface Circuitry



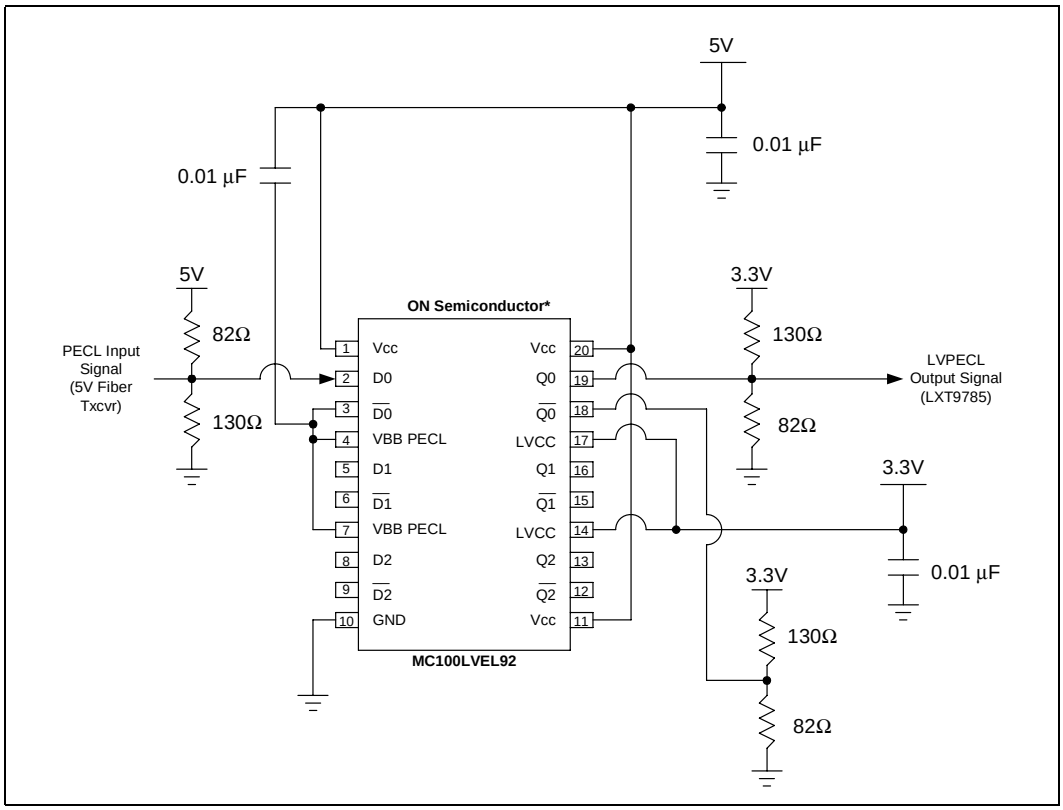
1. Refer to the transceiver manufacturers' recommendations for termination circuitry.

Figure 37 Recommended LXT9785/LXT9785E-to-5 V Fiber Transceiver Interface Circuitry



1. Refer to the transceiver manufacturers' recommendations for termination circuitry.
2. See Figure 38 on page 169 for recommended logic translator interface circuitry.

Figure 38 ON Semiconductor Triple PECL-to-LVPECL Translator



6.0 Test Specifications

Table 52 through Table 82 and Figure 39 through Figure 62 represent the target specifications of the LXT9785/LXT9785E. These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 54 through Table 82 apply over the recommended operating conditions specified in Table 53.

Table 52 Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply voltage	V_{CCIO}, V_{CC}PECL	-0.3	4.0	V
	V_{CCA}, VCCD	-0.3	3.0	V
Storage temperature	TST	-65	+150	ºC
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.				

Table 53 Operating Conditions (Sheet 1 of 2)

Parameter		Sym	Min	Typ1 (2.5 VCCIO)	Typ1 (3.3 VCCIO)	Max	Units
Commercial Operating Temperature	Ambient	Topa	0	–	–	70	ºC
	Case	Topc	0	–	–	108	ºC
Extended Operating Temperature	Ambient	TOPA	-40			85	ºC
	Case	TOPC	-40			123	ºC
Supply voltage[2]	Analog & Digital	Vcca, Vccd	2.38	2.5	2.5	2.63	V
	I/O	VCCIO	2.38	2.5	3.3	3.46	V
	I/O (SD_2P5V = 0)	VCCPECL	3.14	N/A	3.3	3.46	V
	I/O (SD_2P5V = 1)		2.38	2.5	N/A	2.63	V
Operating Current - RMII[3]	100BASE-TX	ICC	–	780		810	mA
		ICCIO	–	60	130	160	mA
	100BASE-FX	ICC	–	380		410	mA
		ICCIO	–	90	170	200	mA
	10BASE-T	ICC	–	710		765	mA
		ICCIO	–	30	70	90	mA
	Power-Down Mode Hardware	ICC	–	20		20	mA
		ICCIO	–	2	3	4	mA
	Auto-Negotiation	ICC	–	500		540	mA
		ICCIO	–	2	4	4	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.
3. Values are aggregated for all eight ports.

Table 53 Operating Conditions (Sheet 2 of 2)

Parameter		Sym	Min	Typ1 (2.5 V_{CCIO})	Typ1 (3.3 V_{CCIO})	Max	Units
Operating Current - SMII[3]	100BASE-TX	I_{CC}	–	800		830	mA
		I_{CCIO}	–	70	130	160	mA
	100BASE-FX	I_{CC}	–	380		410	mA
		I_{CCIO}	–	90	170	200	mA
	10BASE-T	I_{CC}	–	740		770	mA
		I_{CCIO}	–	60	110	130	mA
	Power-Down Mode Hardware	I_{CC}	–	50		50	mA
		I_{CCIO}	–	3	5	5	mA
	Auto-Negotiation	I_{CC}	–	520		570	mA
		I_{CCIO}	–	20	30	30	mA
Operating Current - SS-SMII[3]	100BASE-TX	I_{CC}	–	800		835	mA
		I_{CCIO}	–	90	170	200	mA
	100BASE-FX	I_{CC}	–	380		410	mA
		I_{CCIO}	–	90	170	200	mA
	10BASE-T	I_{CC}	–	740		780	mA
		I_{CCIO}	–	90	150	180	mA
	Power-Down Mode Hardware	I_{CC}	–	30		40	mA
		I_{CCIO}	–	3	5	5	mA
	Auto-Negotiation	I_{CC}	–	530		570	mA
		I_{CCIO}	–	50	70	80	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.
3. Values are aggregated for all eight ports.

Table 54 Digital I/O DC Electrical Characteristics (VCCIO = 2.5 V +/- 5%)

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.75	V	–
Input High voltage	V_{IH}	1.75	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.2	V	I_{OL} = 4 mA
Output Low voltage (LED*m*_*n*_L pins)	V_{OL}-LED	–	–	0.5	V	I_{OL} = 10 mA
Output High voltage	V_{OH}	2.07	–	–	V	I_{OH} = -4 mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 55 Digital I/O DC Electrical Characteristics (VCCIO = 3.3 V +/- 5%)

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.2	V	I_{OL} = 4 mA
Output Low voltage (LED*m*_*n*_L pins)	V_{OL}-LED	–	–	0.5	V	I_{OL} = 10 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 56 Digital I/O DC Electrical Characteristics – SD Pins

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
2.5 V Operation						
Input Low voltage	V_{IL}	0.69	0.8	1.03	V	VCCPECL = 2.5 V
Input High voltage	V_{IH}	1.34	1.6	1.62	V	VCCPECL = 2.5 V
3.3 V Operation						
Input Low voltage	V_{IL}	1.49	1.6	1.83	V	VCCPECL = 3.3 V
Input High voltage	V_{IH}	2.14	2.4	2.42	V	VCCPECL = 3.3 V

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. For 2.5 V operation, SD_2P5V = VCCPECL and VCCPECL=2.5 V.
3. For 3.3 V operation, SD_2P5V = GNDPECL or Floating and VCCPECL=3.3 V.

Table 57 Required Clock Characteristics

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
SMII Input frequency	f	–	125	–	MHz	–
RMII Input frequency	f	–	50	–	MHz	–
Input clock frequency tolerance[1]	Δf	–	–	± 50	ppm	–
Input clock duty cycle[1]	Tdc	35	50	65	%	RMII selection
Input clock duty cycle - REFCLK, TxCLK[1]	Tdc	40	50	60	%	SMII/SS-SMII selection
Output RxCLK duty cycle	Tdc	45	50	55	%	SS-SMII only

1. Parameter is guaranteed by design; not subject to production testing.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 58 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	V_P	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	t_{rf}	3	–	5	ns	Note 2
Rise/fall time symmetry	t_{rfs}	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 16 ns pulse width at 50% of pulse peak
Overshoot	V_O	–	–	5	%	–
Jitter magnitude (measured differentially)	$t_{tx\text{-}jit}$	–	–	1.4	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω (+/-1%) resistor.

Table 59 100BASE-FX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak-to-peak differential output voltage	$V_{DIFFP\text{-}P}$	0.6	1.44	–	V	–
Signal rise/fall time	t_{rf}	–	–	1.8	ns	Note 2
Jitter magnitude (measured differentially)	$t_{tx\text{-}jit}$	–	–	1.4	ns	–
Receiver						
Peak differential input voltage	V_{IP}	0.55	–	–	V	–
Common mode input range	V_{CMIR}	–	–	V_{CC} - 0.5	V	–
Input Low Voltage (SD pins)	V_{IL}	V_{CC} -1.84		V_{CC} -1.63	V	–
Input High Voltage (SD Pins)	V_{IH}	V_{CC} -1.04		V_{CC} -0.88	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 20 - 80 percent into 100 Ω equivalent load of a typical fiber transceiver.

Table 60 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VOP	2.2	2.5	2.8	V	Note 2
Link transmit period	–	8	–	24	ms	–
Jitter magnitude added by the MAU and PLS sections [3,4]	$t_{tx\text{-}jit}$	–	–	11	ns	–
Receiver						
Receive input impedance[3]	ZIN	–	100	–	W	Between TPFIP and TPFIN
Link min receive timer	TLRmin	2	–	7	ms	–
Link max receive timer	TLRmax	50	–	150	ms	–
Differential squelch threshold	VDS	–	475	–	mV Peak	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter addition at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.
4. After line model specified by IEEE 802.3 for 10BASE-T MAU.

Figure 39 SMII - 100BASE-TX Receive Timing

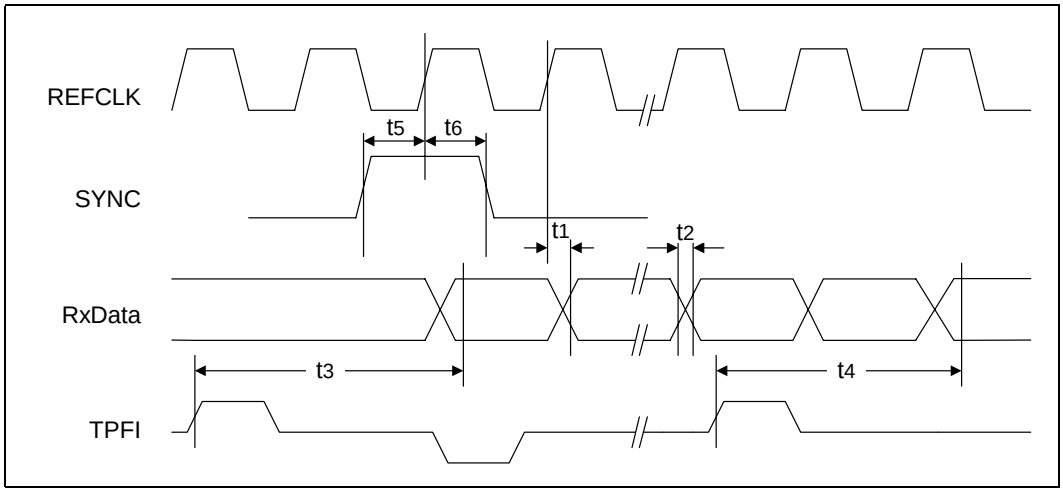


Table 61 SMII - 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
RxData output delay from REFCLK rising edge	t1	1.5	–	5	ns	Minimum C_L = 5 pF Maximum C_L = 20 pF
RxData Rise/Fall Time	t2	–	1.0	–	ns	–
Receive start of /J/ to CRS asserted	t3	–	21	29	BT^2	Synchronous sampling of SMII
Receive start of /T/ to CRS de-asserted	t4	–	25	30	BT^2	Synchronous sampling of SMII
SYNC setup to REFCLK rising edge	t5	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge	t6	1.0	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 40 SMII - 100BASE-TX Transmit Timing

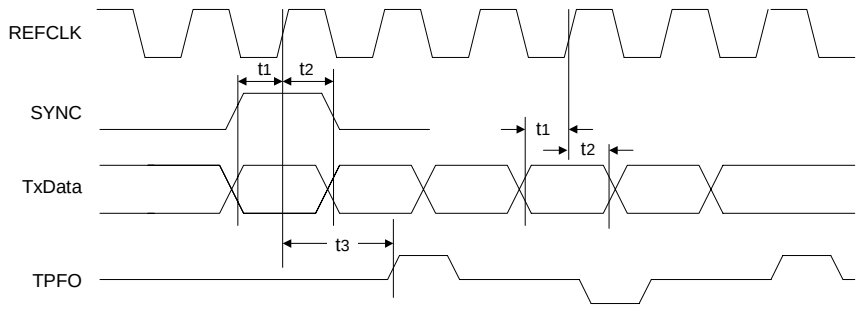


Table 62 SMII - 100BASE-TX Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge and TxData setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge and TxData hold from REFCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start of /J/	t3	–	11	18	BT^2	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 41 SMII - 100BASE-FX Receive Timing

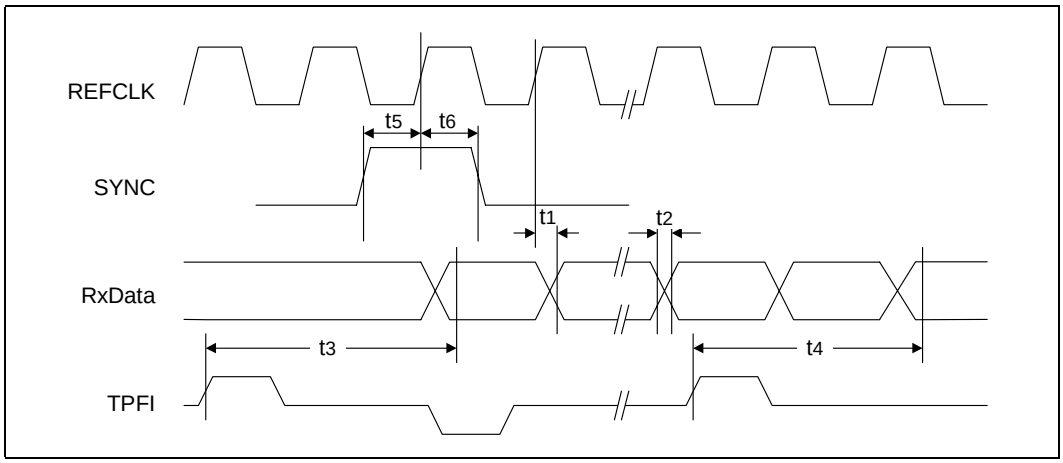


Table 63 SMII - 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
RxData output delay from REFCLK rising edge	t1	1.5	–	5	ns	Minimum C_L = 5 pF Maximum C_L = 20 pF
RxData Rise/Fall Time	t2	–	1	–	ns	–
Receive start of /J/ to CRS asserted	t3	–	18	26	BT[2]	Synchronous sampling of SMII
Receive start of /T/ to CRS de-asserted	t4	–	23	27	BT[2]	Synchronous sampling of SMII
SYNC setup to REFCLK rising edge	t5	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge	t6	1.0	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 42 SMII - 100BASE-FX Transmit Timing

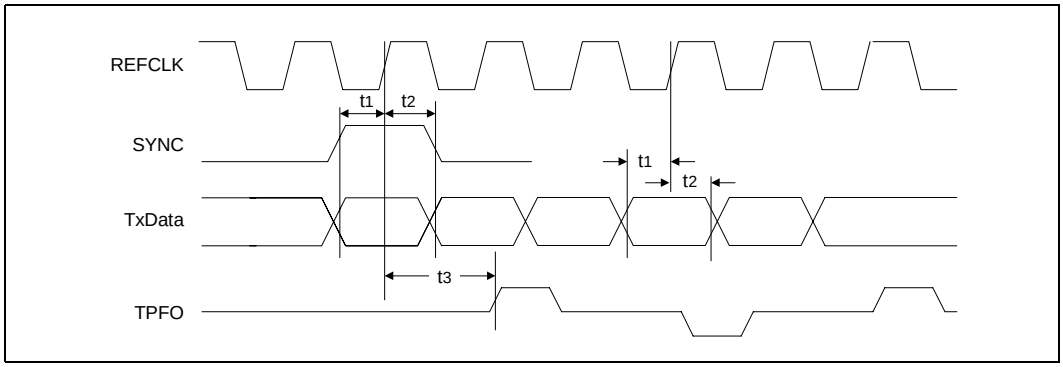


Table 64 SMII - 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge and TxData setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge and TxData hold from REFCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start of /J/	t3	–	10	17	BT[2]	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 43 SMII - 10BASE-T Receive Timing

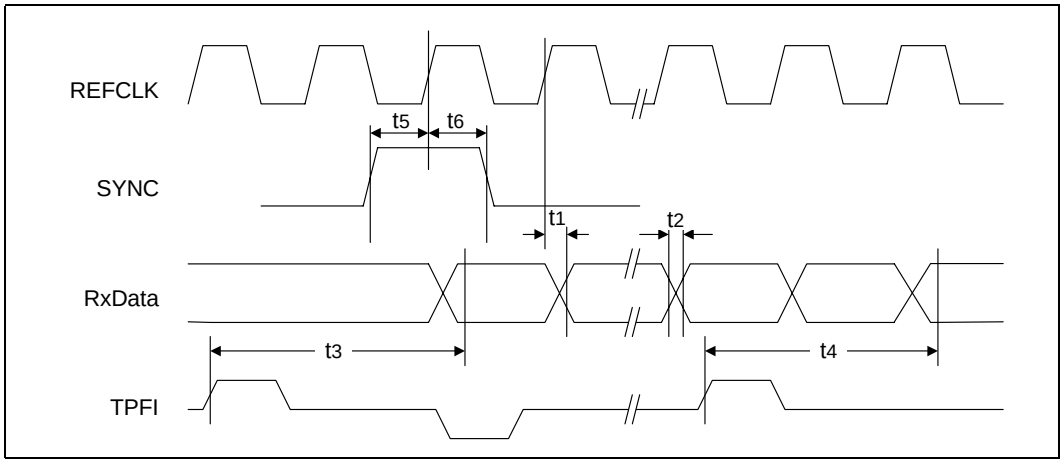


Table 65 SMII - 10BASE-T Receive Timing Parameters (Sheet 1 of 2)

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
RxData output delay from REFCLK rising edge	t1	1.5	–	5	ns	Minimum C_L = 5 pF Maximum C_L = 20 pF
RxData Rise/Fall Time	t2	–	1	–	ns	–
Receive Start-of-Frame to CRS asserted	t3	–	17	21	BT[3]	Synchronous sampling of SMII[2]

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Assumes each SMII segment is sampled for CRS.
3. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Table 65 SMII - 10BASE-T Receive Timing Parameters (Sheet 2 of 2)

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
Receive Start-of-Idle to CRS de-asserted	t4	–	17	18	BT[3]	Synchronous sampling of SMII[2]
SYNC setup to REFCLK rising edge	t5	1.5	–	–	ns	–
SYNC hold from REFCLK rising edge	t6	1.0	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Assumes each SMII segment is sampled for CRS.
3. "BT" signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 44 SMII - 10BASE-T Transmit Timing

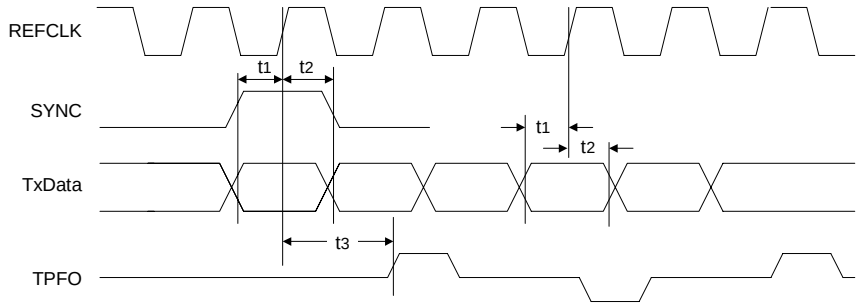


Table 66 SMII-10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
SYNC setup to REFCLK rising edge and TxData setup to REFCLK rising edge	t1	1.5	–	–	ns	–
SYNC hold to REFCLK rising edge and TxData hold from REFCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start-of-frame	t3	–	10	14	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. "BT" signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 45 SS-SMII - 100BASE-TX Receive Timing

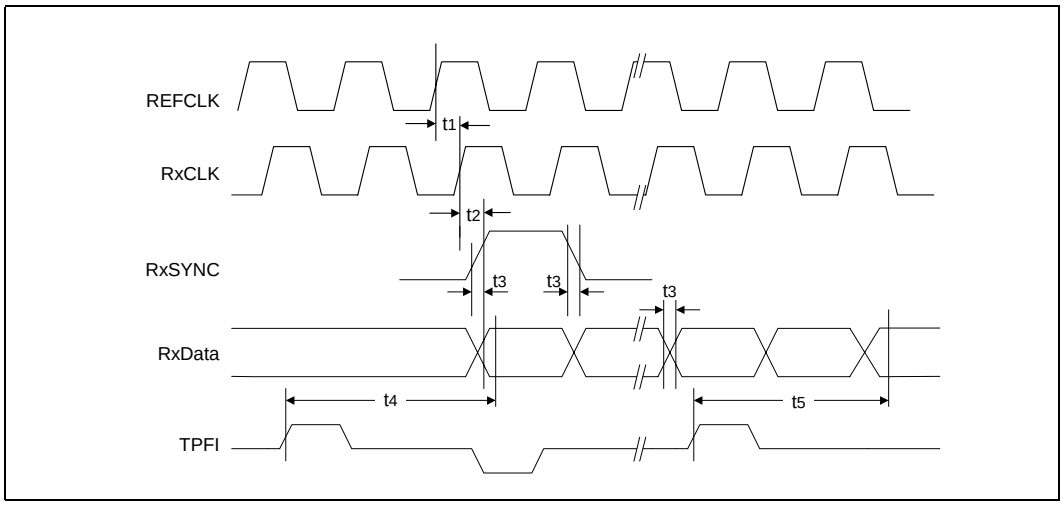


Table 67 SS-SMII - 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
REFCLK rising edge to RxCLK rising edge	t1	–	1.5	–	ns	–
RxData/RxSYNC output delay from RxCLK rising edge	t2	1.5	–	5	ns	Minimum C_L = 5pF Maximum C_L = 40pF
RxData/RxSYNC Rise/Fall time	t3	–	1.0	–	ns	–
Receive start of /J/ to CRS asserted	t4	–	21	27	BT[2]	–
Receive start of /T/ to CRS de-asserted	t5	–	25	30	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 46 SS-SMII - 100BASE-TX Transmit Timing

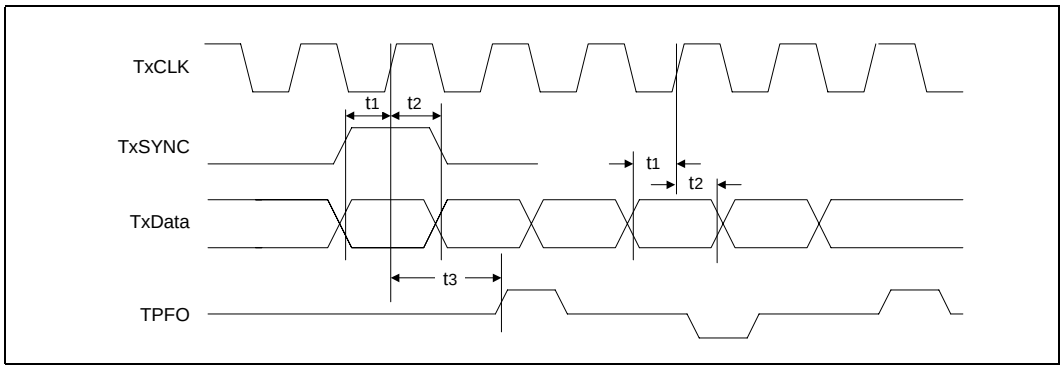


Table 68 SS-SMII - 100BASE-TX Transmit Timing

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
TxSYNC setup to TxCLK rising edge and TxData setup to TxCLK rising edge	t1	1.5	–	–	ns	–
TxSYNC hold from TxCLK rising edge and TxData hold to TxCLK rising edge	t2	1.0	–	–	ns	–
TxEN sampled to start of /J/	t3	–	11	18	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 47 SS-SMII - 100BASE-FX Receive Timing

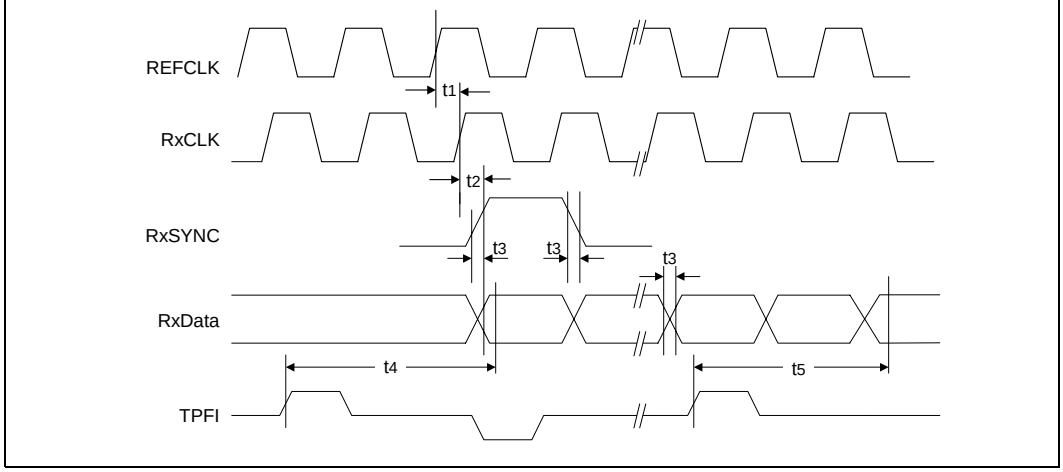


Table 69 SS-SMII - 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
REFCLK rising edge to RxCLK rising edge	t1	–	1.5		ns	–
RxData/RxSYNC output delay from RxCLK rising edge	t2	1.5	–	5	ns	Minimum C_L = 5pF Maximum C_L = 40pF
RxData/RxSYNC Rise/Fall time	t3	–	1	–	ns	–
Receive start of /J/ to CRS asserted	t4	–	18	23	BT[2]	–
Receive start of /T/ to CRS de-asserted	t5	–	21	26	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 48 SS-SMII - 100BASE-FX Transmit Timing

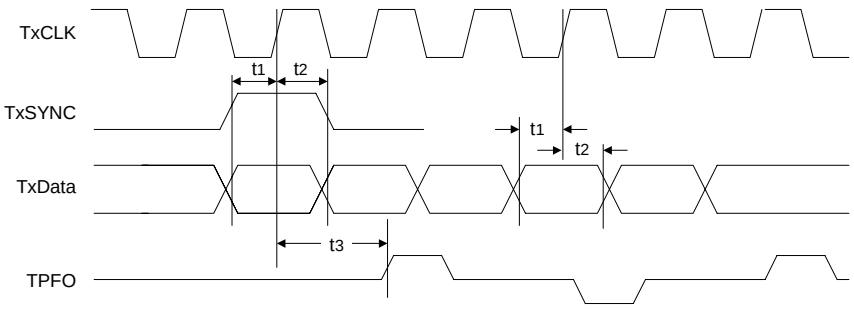


Table 70 SS-SMII - 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
TxSYNC setup to TxCLK rising edge and TxData setup to TxCLK rising edge	t1	1.5	–	–	ns	–
TxSYNC hold from TxCLK rising edge and TxData hold to TxCLK rising edge	t2	1.0	–	–	ns	–
TxData to TPFO Latency	t3	–	11	13	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 49 SS-SMII - 10BASE-T Receive Timing

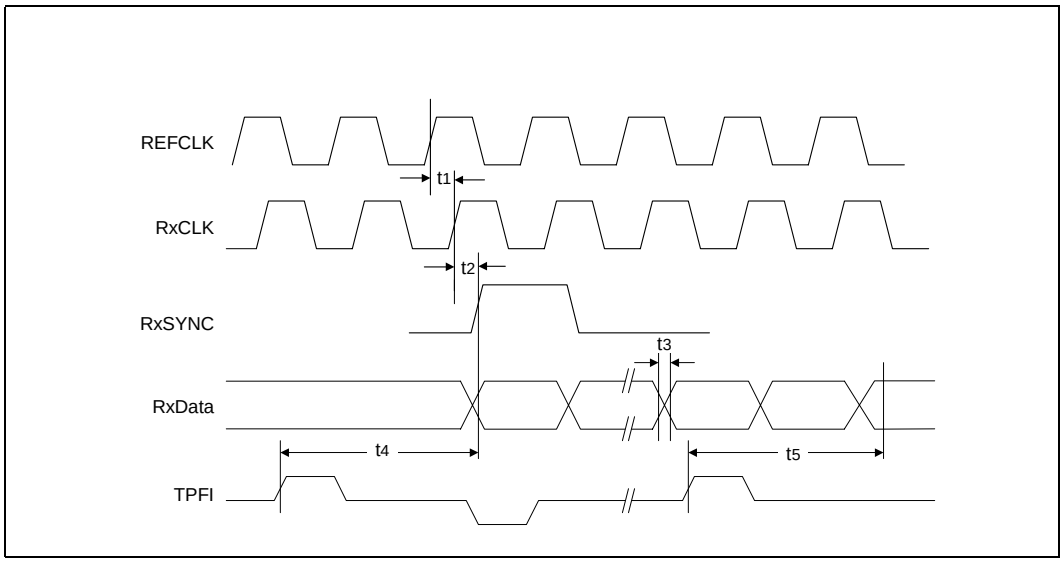


Table 71 SS-SMII - 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
REFCLK rising edge to RxCLK rising edge	t1	–	1.5	–	ns	–
RxData/RxSYNC output delay from RxCLK rising edge	t2	1.5	–	5	ns	Minimum C_L = 5pF Maximum C_L = 40pF
RxData/RxSYNC Rise/Fall time	t3	–	1	–	ns	–
Receive Start-of-Frame to CRS asserted	t4	–	10	11	BT[3]	Synchronous sampling of SMII[2]
Receive Start-of-Idle to CRS de-asserted	t5	–	18	21	BT[3]	Synchronous sampling of SMII[2]

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Assumes each SMII segment is sampled for CRS.
3. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 50 SS-SMII - 10BASE-T Transmit Timing

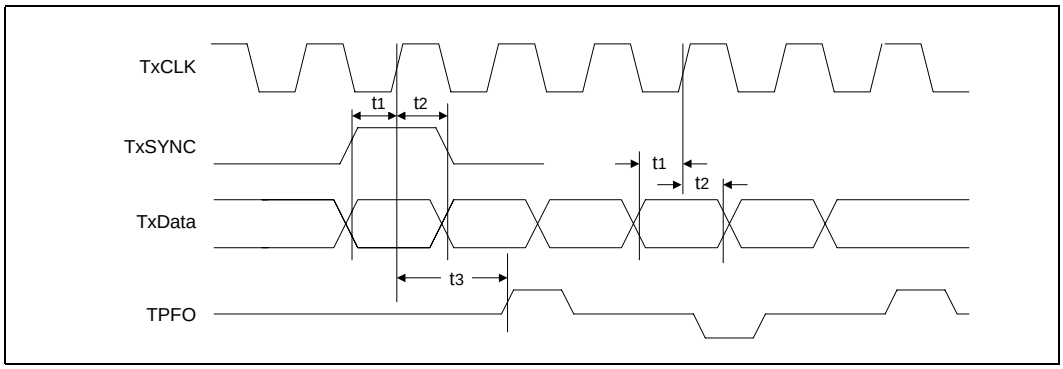


Table 72 SS-SMII - 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
TxSYNC setup to TxCLK rising edge and TxData setup to TxCLK rising edge	t1	1.5	–	–	ns	–
TxSYNC hold to TxCLK rising edge and TxData hold from TxCLK rising edge	t2	1.0	–	–	ns	–
TxData to TPFO Latency	t3	–	10	14	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 51 RMII - 100BASE-TX Receive Timing

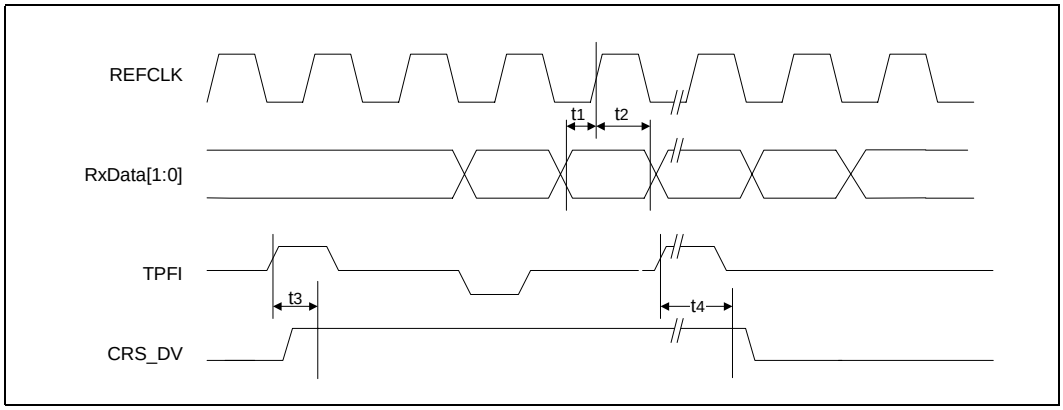


Table 73 RMII - 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
RxData<1:0>, CRS_DV, RXER setup to REFCLK rising edge[3]	t1	4	–	14	ns	–
RxData<1:0>, CRS_DV, RXER hold from REFCLK rising edge[3]	t2	2	–	14	ns	–
Receive start of /J/ to CRS_DV asserted	t3	–	16	21	BT[2]	–
Receive start of /T/ to CRS_DV de-asserted	t4	–	20	27	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. "BT" signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).
3. Values and conditions from RMII Specification, Rev. 1.2.

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 52 RMII - 100BASE-TX Transmit Timing

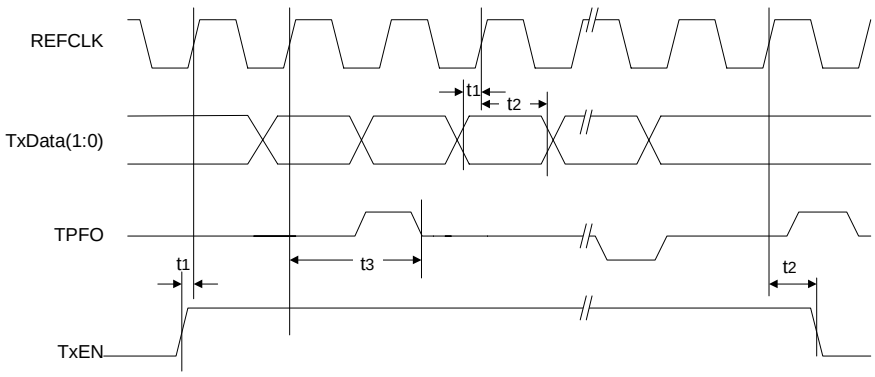


Table 74 RMII - 100BASE-TX Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
TxData<1:0>/TxEN setup to REFCLK rising edge	t1	4	–	–	ns	–
TxData<1:0>/TxEN hold from REFCLK rising edge	t2	2	–	–	ns	–
TxEN sampled to TPFO out (Tx latency)	t3	–	12	17	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. "BT" signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 53 RMII - 100BASE-FX Receive Timing

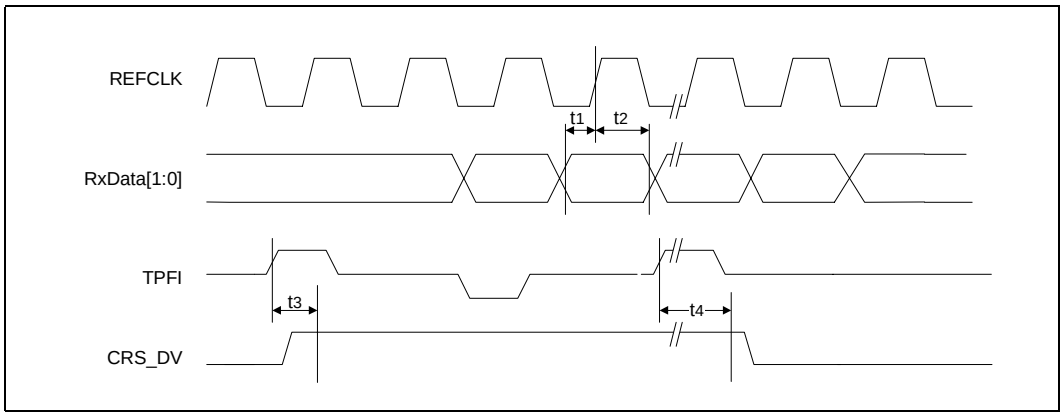


Table 75 RMII - 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
RxData<1:0>, CRS_DV, RXER setup to REFCLK rising edge[3]	t1	4	–	14	ns	–
RxData<1:0>, CRS_DV, RXER hold from REFCLK rising edge[3]	t2	2	–	14	ns	–
Receive start of /J/ to CRS_DV asserted	t3	–	14	18	BT[2]	–
Receive start of /T/ to CRS_DV de-asserted	t4	–	18	25	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).
3. Values and conditions from RMII Specification, Rev. 1.2.

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 54 RMII - 100BASE-FX Transmit Timing

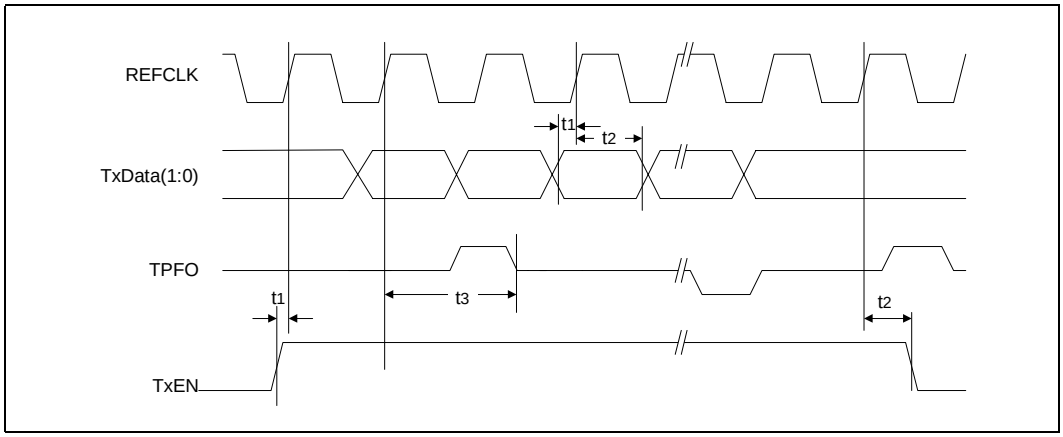


Table 76 RMII - 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
TxData<1:0>/TxEN setup to REFCLK rising edge	t1	4	–	–	ns	–
TxData<1:0>/TX-EN hold from REFCLK rising edge	t2	2	–	–	ns	–
TxEN sampled to TPFO out (Tx latency)	t3	–	10	12	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 55 RMII - 10BASE-T Receive Timing

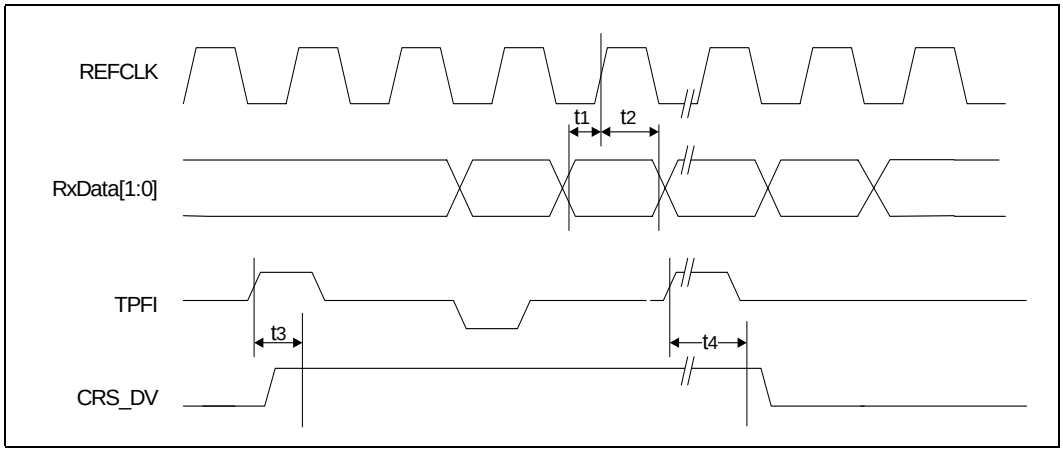


Table 77 RMII - 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
RxData<1:0>, CRS_DV setup to REFCLK rising edge[3]	t1	4	–	14	ns	–
RxData<1:0>, CRS_DV hold from REFCLK rising edge[3]	t2	2	–	14	ns	–
TPFI in to CRS_DV asserted	t3	1.5	3	4	BT[2]	–
TPFI quiet to CRS_DV de-asserted	t4	12	15	16	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).
3. Values and conditions from RMII Specification, Rev. 1.2.

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 56 RMII - 10BASE-T Transmit Timing

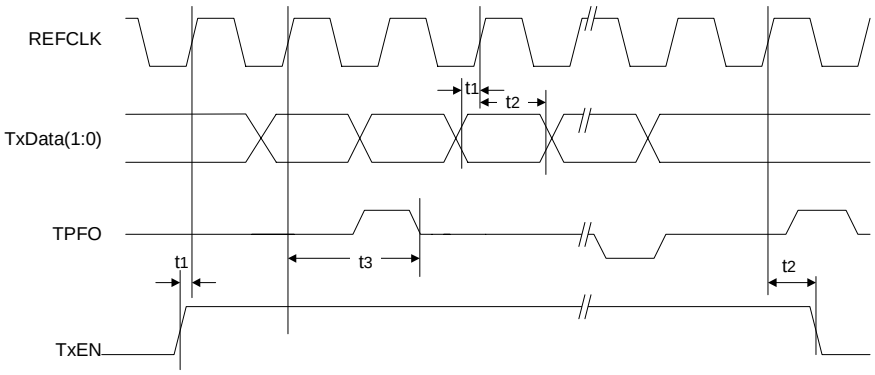


Table 78 RMII - 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
TxData<1:0>/TxEN setup to REFCLK rising edge	t1	4	–	–	ns	–
TxData<1:0>/TxEN hold from REFCLK rising edge	t2	2	–	–	ns	–
TxEN sampled to TPFO out (Tx latency)	t3	–	8.5	14	BT[2]	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. “BT” signifies bit times at the line rate (that is, BT = 100 ns if using 10BASE-T, BT = 10 ns if using 100BASE-TX or 100BASE-FX).

Note: The table latency values are derived with the hardware configuration pins FIFOSEL[1:0] set at a default configuration of 00 (32 bits of initial fill).

Figure 57 Auto-Negotiation and Fast Link Pulse Timing

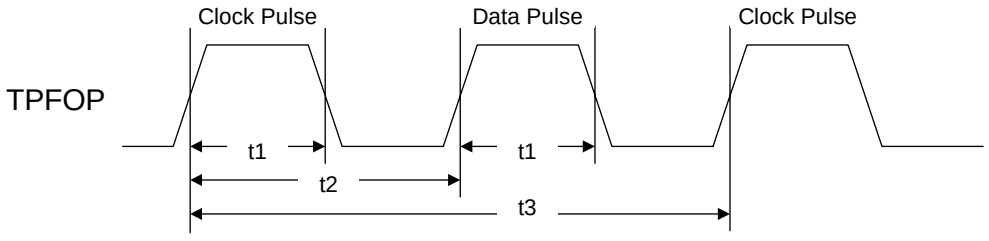


Figure 58 Fast Link Pulse Timing

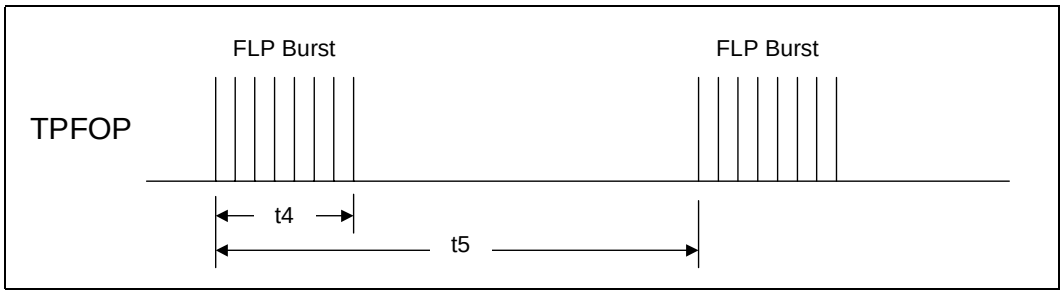


Table 79 Auto-Negotiation and Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	69.5	µs	–
Clock pulse to Clock pulse	t3	111	–	139	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	–	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 59 MDIO Write Timing (MDIO Sourced by MAC)

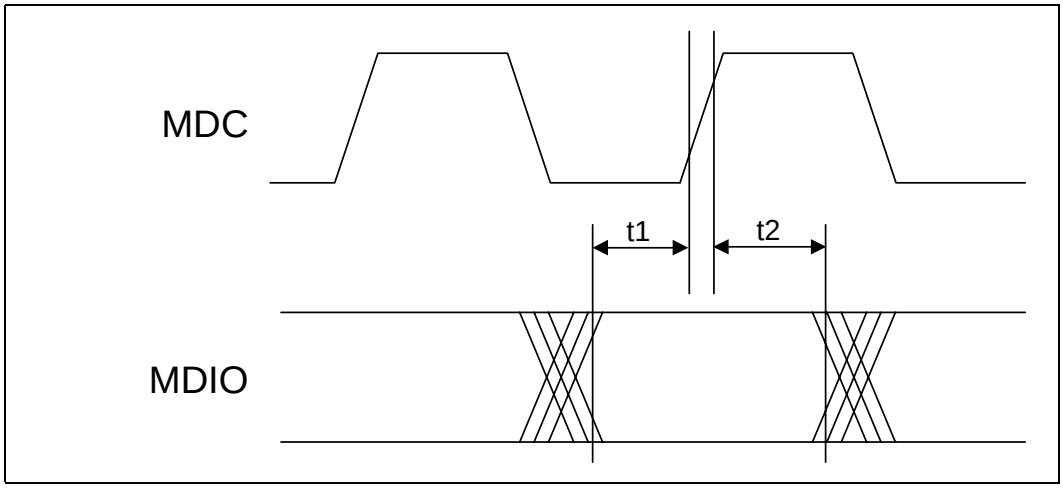


Figure 60 MDIO Read Timing (MDIO Sourced by PHY)

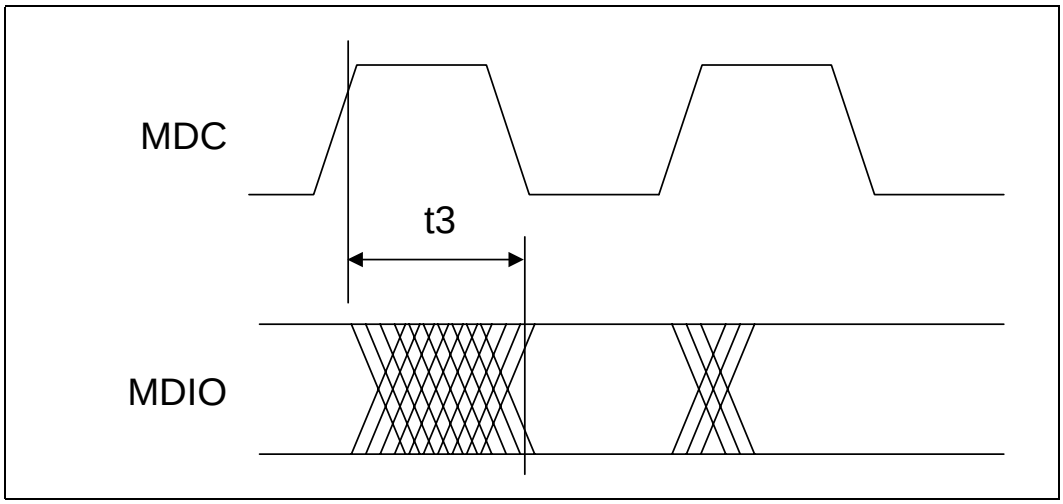


Table 80 MDIO Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	–
MDIO hold after MDC, sourced by STA	t2	10	–	–	ns	–
MDC to MDIO output delay, sourced by PHY	t3	0	–	40	ns	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 61 Power-Up Timing

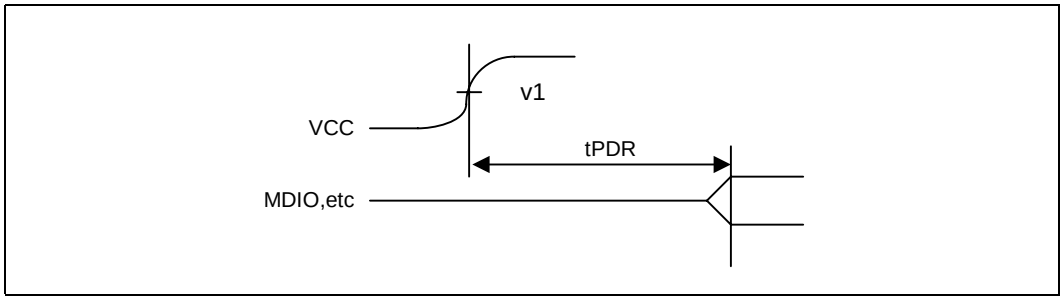


Table 81 Power-Up Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
Voltage Threshold	v1	2.1	–	–	V	–
Power-up recovery time	t_{PDR}	100	–	–	ms	–
Software power-down[2]	t_{SPDR}	20	–	–	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. The minimum time required between bringing up consecutive ports powered down by Register bit 0.11, or a software or hardware reset.

Figure 62 RESET_L Recovery Timing

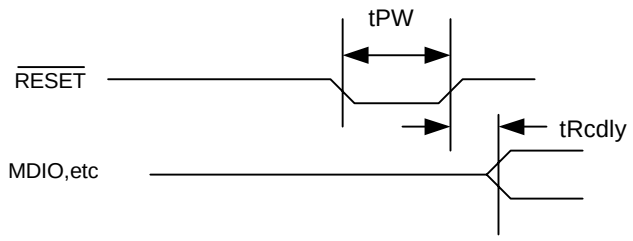


Table 82 RESET_L Recovery Timing Parameters

Parameter	Sym	Min	Typ1	Max	Units	Test Conditions
Reset pulse width	tPW	10	–	–	ns	–
Reset recovery delay	tRcdly	0.4	–	–	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

7.0 Register Definitions

The LXT9785/LXT9785E register set includes multiple 16-bit registers and 18 registers per port. Table 83 presents a complete register listing. Table 84, *Control Register (Address 0)*, on page 192 through Table 101, *Cable Diagnostics Register (Address 29, Hex 1D)*, on page 209 define individual registers and Table 102, *Register Bit Map, on page 210* provides a consolidated memory map of all registers.

Base registers (0 through 8) are defined in accordance with the “Reconciliation Sublayer and Media Independent Interface” and “Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation” sections of the IEEE 802.3 standard.

Additional registers (16 through 21, 25, 27, and 29) are defined in accordance with the IEEE 802.3 standard for adding unique device functions.

The BGA15 package on some registers has different default values. Some LXT9785/ LXT9785E features are not available on the BGA15 package. These differences are called out in the register description and in the table notes in individual register tables.

Table 83 Register Set

Address	Register Name	Bit Assignments
0	*Control Register (Address 0)*	Refer to Table 84 on page 192
1	*Status Register (Address 1)*	Refer to Table 85 on page 193
2	*PHY Identification Register 1 (Address 2)*	Refer to Table 86 on page 194
3	*PHY Identification Register 2 (Address 3)*	Refer to Table 87 on page 194
4	*Auto-Negotiation Advertisement Register (Address 4)*	Refer to Table 88 on page 195
5	*Auto-Negotiation Link Partner Base Page Ability Register (Address 5)*	Refer to Table 89 on page 196
6	*Auto-Negotiation Expansion Register (Address 6)*	Refer to Table 90 on page 197
7	*Auto-Negotiation Next Page Transmit Register (Address 7)*	Refer to Table 91 on page 198
8	*Auto-Negotiation Link Partner Next Page Receive Register (Address 8)*	Refer to Table 92 on page 198
9	1000BASE-T/100BASE-T2 Control	Not Implemented
10	1000BASE-T/100BASE-T2 Status	Not Implemented
15	Extended Status	Not Implemented
16	*Port Configuration Register (Address 16, Hex 10)*	Refer to Table 93 on page 199
17	*Quick Status Register (Address 17, Hex 11)*	Refer to Table 94 on page 200
18	*Interrupt Enable Register (Address 18, Hex 12)*	Refer to Table 95 on page 201
19	*Interrupt Status Register (Address 19, Hex 13)*	Refer to Table 96 on page 203
20	*LED Configuration Register (Address 20, Hex 14)*	Refer to Table 97 on page 204
21	*Receive Error Count Register (Address 21, Hex 15)*	Refer to Table 98 on page 205
22-24	Reserved	N/A
25	*RMII Out-of-Band Signaling Register (Address 25, Hex 19)*	Refer to Table 99 on page 206
26	Reserved	N/A
27	*Trim Enable Register (Address 27, Hex 1B)*	Refer to Table 100 on page 207

Table 83 Register Set

Address	Register Name	Bit Assignments
28	Reserved	N/A
29	*Cable Diagnostics Register (Address 29, Hex 1D)*	Refer to Table 101 on page 209
30 - 31	Reserved	N/A

Table 84 Control Register (Address 0)

Bit	Name	Description	Type[1]	Default
15	RESET_L	0 = Normal operation 1 = PHY reset	R/W SC	0[2]
14[6]	Loopback	0 = Disable loopback mode 1 = Enable loopback mode **Not recommended to enable auto-negotiation while in internal loopback operation.**	R/W	0
13	Speed Selection	0.6 / 0.13 1 / 1 = Reserved 1 / 0 = 1000 Mbps (not allowed) 0 / 1 = 100 Mbps 0 / 0 = 10 Mbps	R/W	LSHR[3,4]
12	Auto-Negotiation Enable	0 = Disable auto-negotiation process 1 = Enable auto-negotiation process	R/W	LSHR[3,4]
11	Power-Down	0 = Normal operation 1 = Power-down	R/W	LSHR[3,5]
10	Isolate	0 = Normal operation 1 = Electrically isolate PHY from RMII/SMII/SS-SMII interfaces	R/W	0
9	Restart Auto-Negotiation	0 = Normal operation 1 = Restart auto-negotiation process	R/W SC	0
8	Duplex Mode	0 = Half-duplex 1 = Full-duplex	R/W	LSHR[3,4]

1. R/W = Read/Write, SC = Self Clearing when operation complete.
2. During a hardware reset, all LHR information is latched in from the pins. During a software reset (0.15), the LSHR information is not re-read from the pins. This information reverts back to the information that was read in during the hardware reset. During a hardware rest, register information is unavailable from 1 ms after de-assertion of the reset. During a software reset (0.15) the registers are available for reading. The reset bit should be polled to see when the part has completed reset.
3. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
4. Default value of Register bits 0.12, 0.13, and 0.8 are determined by the CFG pins as described in Table 42, *Global Hardware Configuration Settings*, on page 126.
5. Default value of Register bit 0.11 is determined by the LINKHOLD configuration pin.
6. Link Status is reported in 10 Mbps mode as down and in 100 Mbps mode as up in loopback mode. Register bits 17.12 (Receive Status) and 17.13 (Transmit Status) are not updated in 10 Mbps loopback mode.

Table 84 Control Register (Address 0)

Bit	Name	Description	Type[1]	Default
7	Collision Test	This bit is ignored by the LXT9785/LXT9785E 0 = Disable COL signal test 1 = Enable COL signal test	R/W	0
6	Speed Selection 1000 Mbps	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	0
5:0	Reserved	Write as 0, ignore on Read	R/W	000000

1. R/W = Read/Write, SC = Self Clearing when operation complete.
2. During a hardware reset, all LHR information is latched in from the pins. During a software reset (0.15), the LSHR information is not re-read from the pins. This information reverts back to the information that was read in during the hardware reset. During a hardware rest, register information is unavailable from 1 ms after de-assertion of the reset. During a software reset (0.15) the registers are available for reading. The reset bit should be polled to see when the part has completed reset.
3. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
4. Default value of Register bits 0.12, 0.13, and 0.8 are determined by the CFG pins as described in Table 42, *Global Hardware Configuration Settings*, on page 126.
5. Default value of Register bit 0.11 is determined by the LINKHOLD configuration pin.
6. Link Status is reported in 10 Mbps mode as down and in 100 Mbps mode as up in loopback mode. Register bits 17.12 (Receive Status) and 17.13 (Transmit Status) are not updated in 10 Mbps loopback mode.

Table 85 Status Register (Address 1)

Bit	Name	Description	Type[1, 2]	Default
15	100BASE-T4	0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	R	0
14	100BASE-X Full-Duplex	0 = PHY not able to perform full-duplex 100BASE-X 1 = PHY able to perform full-duplex 100BASE-X	R	1
13	100BASE-X Half-Duplex	0 = PHY not able to perform half-duplex 100BASE-X 1 = PHY able to perform half-duplex 100BASE-X	R	1
12	10 Mbps Full-Duplex	0 = PHY not able to operate at 10 Mbps in full-duplex mode 1 = PHY able to operate at 10 Mbps in full-duplex mode	R	1
11	10 Mbps Half-Duplex	0 = PHY not able to operate at 10 Mbps in half-duplex 1 = PHY able to operate at 10 Mbps in half-duplex mode	R	1
10	100BASE-T2 Full-Duplex	0 = PHY not able to perform full-duplex 100BASE-T2 1 = PHY able to perform full-duplex 100BASE-T2	R	0
9	100BASE-T2 Half-Duplex	0 = PHY not able to perform half-duplex 100BASE-T2 1 = PHY able to perform half-duplex 100BASE-T2	R	0
8	Extended Status	0 = No extended status information in Register 15 1 = Extended status information in Register 15	R	0
7	Reserved	Write as 0, ignore on Read	R	0

1. R = Read Only
2. Bits that Latch High (LH) or Latch Low (LL) automatically clear when read.

Table 85 Status Register (Address 1)

Bit	Name	Description	Type[1, 2]	Default
6	MF Preamble Suppression	0 = PHY will not accept management frames with preamble suppressed 1 = PHY accepts management frames with preamble suppressed	R	0
5	Auto-Negotiation complete	0 = Auto-negotiation not complete 1 = Auto-negotiation complete	R	0
4	Remote Fault	0 = No remote fault condition detected 1 = Remote fault condition detected	R/LL	0
3	Auto-Negotiation Ability	0 = PHY is not able to perform auto-negotiation 1 = PHY is able to perform auto-negotiation	R	1
2	Link Status	0 = Link is down 1 = Link is up	R/LL	0
1	Jabber Detect	0 = Jabber condition not detected 1 = Jabber condition detected	R/LH	0
0	Extended Capability	0 = Basic register capabilities 1 = Extended register capabilities	R	1

1. R = Read Only
2. Bits that Latch High (LH) or Latch Low (LL) automatically clear when read.

Table 86 PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type[1]	Default
15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI	R	0013 hex

1. R = Read Only

Table 87 PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type[1]	Default
15:10	PHY ID Number	The PHY identifier composed of bits 19 through 24 of the OUI	R	011110
9:4	Manufacturer's Model Number	6 bits containing manufacturer's part number	R	001111
3:1	Manufacturer's Revision Number	3 bits containing manufacturer's revision number	R	XXX[2]
0	Model Variant	0 = LXT9785 1 = LXT9785/LXT9785E	R	X[2]

1. R = Read Only
2. Refer to the Identification Information section in the Cortina Systems® LXT9785/LXT9785E Specification Update.

Figure 63 PHY Identifier Bit Mapping

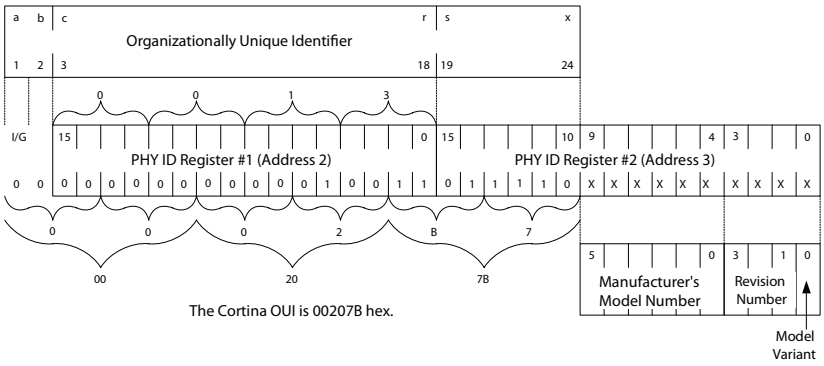


Table 88 Auto-Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type[1]	Default
15	Next Page	0 = Port has no ability to send manual next pages 1 = Port has ability to send manual next pages **Note:** This bit should only be set to manually control the auto-negotiation process. It is not needed and should be cleared for DTE Discovery.	R/W	0
14	Reserved	Write as 0, ignore on Read	R	0
13[6]	Remote Fault	0 = No remote fault 1 = Remote fault	R/W	0
12	Reserved	Write as 0, ignore on Read	R/W	0
11	Asymmetric Pause	Pause operation defined in Clause 40 and 27 0 = Port is not Pause capable 1 = Port can only send Pause	R/W	0
10	Pause[5]	0 = Pause operation disabled 1 = Port can send and receive Pause ***Note:*** Default for the BGA15 package is 0.	R/W	LSHR[2,3]

1. R/W = Read/Write, R = Read Only
2. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
3. The default setting of Register bit 4.10 is determined by the PAUSE pin. The BGA15 package does not have a Pause hardware configuration pin and has a default of 0.
4. Default settings for bits 4.5:8 are determined by CFG pins as described in Table 42, *Global Hardware Configuration Settings*, on page 126.
5. Pause operation is only valid for full-duplex modes.
6. If Register bit 4.13 is set to advertise a fault, Register bit 1.4 will be set. Register bit 4.13 is set or cleared only through the MDC/MDIO interface and is not cleared upon completion of auto-negotiation.

Note: Restart the auto-negotiation process whenever Register 4 is written/modified.

Table 88 Auto-Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type[1]	Default
9	100BASE-T4	0 = 100BASE-T4 capability is not available 1 = 100BASE-T4 capability is available (The LXT9785/LXT9785E does not support 100BASE-T4 but allows this bit to be set to advertise in the auto-negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
8	100BASE-TX Full-Duplex	0 = Port is not 100BASE-TX full-duplex capable. 1 = Port is 100BASE-TX full-duplex capable	R/W	LSHR[2,4]
7	100BASE-TX Half-Duplex	0 = Port is not 100BASE-TX half-duplex capable 1 = Port is 100BASE-TX half-duplex capable	R/W	LSHR[2,4]
6	10BASE-T Full-Duplex	0 = Port is not 10BASE-T full-duplex capable 1 = Port is 10BASE-T full-duplex capable	R/W	LSHR[2,4]
5	10BASE-T Half-Duplex	0 = Port is not 10BASE-T half-duplex capable 1 = Port is 10BASE-T half-duplex capable	R/W	LSHR[2,4]
4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future auto-negotiation development <11111> = Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted	R/W	00001

1. R/W = Read/Write, R = Read Only
2. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
3. The default setting of Register bit 4.10 is determined by the PAUSE pin. The BGA15 package does not have a Pause hardware configuration pin and has a default of 0.
4. Default settings for bits 4.5:8 are determined by CFG pins as described in Table 42, *Global Hardware Configuration Settings*, on page 126.
5. Pause operation is only valid for full-duplex modes.
6. If Register bit 4.13 is set to advertise a fault, Register bit 1.4 will be set. Register bit 4.13 is set or cleared only through the MDC/MDIO interface and is not cleared upon completion of auto-negotiation.

Note: Restart the auto-negotiation process whenever Register 4 is written/modified.

Table 89 Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type[1]	Default[2]
15	Next Page	0 = Link partner has no ability to send multiple pages 1 = Link partner has ability to send multiple pages	R	0
14	Acknowledge	0 = Link partner has not received Link Code Word from the the LXT9785/LXT9785E 1 = Link partner has received Link Code Word from the LXT9785/LXT9785E.	R	0
13	Remote Fault	0 = No remote fault 1 = Remote fault	R	0
12	Reserved	Write as 0, ignore on Read	R	0
11	Asymmetric Pause	Pause operation defined in Clause 40 and 27 0 = Link partner is not Pause capable 1 = Link partner can only send Pause	R	0

1. R = Read Only
2. Default value at the start of auto-negotiation code word transmission.

Table 89 Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type[1]	Default[2]
10	Pause	0 = Link partner is not Pause capable 1 = Link partner can send and receive Pause	R	0
9	100BASE-T4	0 = Link partner is not 100BASE-T4 capable 1 = Link partner is 100BASE-T4 capable	R	0
8	100BASE-TX Full-Duplex	0 = Link partner is not 100BASE-TX full-duplex capable 1 = Link partner is 100BASE-TX full-duplex capable	R	0
7	100BASE-TX	0 = Link partner is not 100BASE-TX capable 1 = Link partner is 100BASE-TX capable	R	0
6	10BASE-T Full-Duplex	0 = Link partner is not 10BASE-T full-duplex capable 1 = Link partner is 10BASE-T full-duplex capable	R	0
5	10BASE-T	0 = Link partner is not 10BASE-T capable 1 = Link partner is 10BASE-T capable	R	0
4:0	Selector Field S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future auto-negotiation development <11111> = Reserved for future auto-negotiation development Unspecified or reserved combinations shall not be transmitted	R	00000

1. R = Read Only
2. Default value at the start of auto-negotiation code word transmission.

Table 90 Auto-Negotiation Expansion Register (Address 6)

Bit	Name	Description	Type[1]	Default
15:5	Reserved	Write as 0, ignore on Read	R	0x000
4	Parallel Detection Fault	0 = Parallel detection fault has not occurred 1 = Parallel detection fault has occurred	R/ LH	0
3	Link Partner Next Page Able	0 = Link partner is not next page able 1 = Link partner is next page able	R	0
2	Next Page Able	0 = Local device is not next page able 1 = Local device is next page able	R	1
1	Page Received	Indicates that a new page has been received and the received code word has been loaded into Register 5 or Register 8 as specified in clause 28 of 802.3. 0 = Three identical and consecutive link code words have not been received from link partner 1 = Three identical and consecutive link code words have been received from link partner	R/ LH	0
0	Link Partner A/N Able	0 = Link partner is not auto-negotiation able 1 = Link partner is auto-negotiation able	R	0

1. R = Read Only, LH = Latching High – cleared when read

Table 91 Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type[1]	Default
15	Next Page (NP)	0 = Last page 1 = Additional next pages follow	R/W	0
14	Reserved	Write as 0, ignore on Read.	R	0
13	Message Page (MP)	0 = Unformatted page 1 = Message page	R/W	1
12	Acknowledge 2 (ACK2)	0 = Cannot comply with message 1 = Complies with message	R/W	0
11	Toggle (T)	0 = Previous value of the transmitted link code word equalled logic one 1 = Previous value of the transmitted link code word equalled logic zero	R	0
10:0	Message/ Unformatted Code Field	MP = 0: Code interpreted as “unformatted page” MP = 1: Code interpreted as “message page”	R/W	00000000001

1. R/W = Read Write, R = Read Only

Table 92 Auto-Negotiation Link Partner Next Page Receive Register (Address 8)

Bit	Name	Description	Type[1]	Default[2]
15	Next Page (NP)	0 = Link partner has no additional next pages to send 1 = Link partner has additional next pages to send	R	0
14	Acknowledge (ACK)	0 = Link partner has not received Link Code Word from the LXT9785/LXT9785E 1 = Link partner has received Link Code Word from the LXT9785/LXT9785E	R	0
13	Message Page (MP)	0 = Page sent by the link partner is an unformatted page 1 = Page sent by the link partner is a message page	R	0
12	Acknowledge 2 (ACK2)	0 = Link partner cannot comply with the message 1 = Link partner complies with the message	R	0
11	Toggle (T)	0 = Previous value of the transmitted Link Code Word equalled logic one 1 = Previous value of the transmitted Link Code Word equalled logic zero	R	0
10:0	Message/ Unformatted Code Field	MP = 1: Code interpreted as message page MP = 0: Code interpreted as unformatted page	R	0x000

1. R = Read Only
2. Default value at the start of auto-negotiation code word transmission.

Table 93 Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description		Type [1]	Default
15	Reserved	Write as 0, ignore on Read		R/W	0
14	Link Disable	0 = Normal operation 1 = Force link pass (sets appropriate registers and LEDs to pass) **Note:** Setting this bit in 100 Mbps mode by-passes the descrambler lock requirement to establish link and forces the link to the link-good state. Setting this bit produces unreliable results if the descrambler is not locked,		R/W	0
13	Transmit Disable	0 = Normal operation 1 = Disable twisted-pair transmitter		R/W	0
12	Bypass Scramble (100BASE-TX)	0 = Normal operation 1 = Bypass scrambler and descrambler		R/W	0
11	Reserved	Write as 0, ignore on Read		R/W	0
10	Jabber (10BASE-T)	0 = Normal operation 1 = Jabber function is enabled; however, jabber status reporting to Register bit 1.1 is disabled		R/W	0
9	Reserved	Write as 0, ignore on Read.		R/W	0
8	TP Loopback (10BASE-T)	0 = Normal operation 1 = Disable twisted-pair loopback during half-duplex operation **Note:** Valid function in SMII and S-SMII modes only.		R/W	1
7	Reserved	Write as 1, ignore on Read		R/W	1
6	Reserved	Write as 0, ignore on Read		R/W	0
5	Preamble Enable	10 Mbps	0 = No preamble (default) 1 = Preamble enabled ***Note:*** Default for BGA15 package is 0.	R/W	LSHR[2,4]
		100 Mbps	No effect		N/A
4	Reserved	Write as 0, ignore on Read		R/W	0
3	Reserved	Write as 0, ignore on Read		R/W	0
2	Far End Fault Transmission Enable	0 = Disable Far End Fault transmission 1 = Enable Far End Fault transmission		R/W	1
	Invalid for BGA15	Write as '0', ignore on Read (BGA15).			

1. R/W = Read/Write
2. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
3. The default value of Register bit 16.0 is determined by the G_FX/TP_L pin. If G_FX/TP_L is tied Low, the default value of Register bit 16.0 = 0. If G_FX/TP_L is not tied Low, the default value of Register bit 16.0 = 1. The BGA15 package does not have a G_FX/TP_L hardware configuration pin.
4. The default value of Register bit 16.5 is determined by the PREASEL pin. The BGA15 package does not have a PREASEL hardware configuration pin and has a default of 0.
5. The BGA15 package does not support fiber. Default for the BGA15 package is 0.
6. NA means the bits do not have a default value and may initially contain any value.

Table 93 Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
1	Reserved	Write as 0, ignore on Read.	R/W	0
0	Fiber Select[5]	0 = Select twisted-pair mode for this port 1 = Select fiber mode for this port	R/W	LSHR[2,3]
	Reserved for BGA15	Write as '0', ignore on Read (BGA15). ***Note:*** Default for BGA15 is 0.		

1. R/W = Read/Write
2. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
3. The default value of Register bit 16.0 is determined by the G_FX/TP_L pin. If G_FX/TP_L is tied Low, the default value of Register bit 16.0 = 0. If G_FX/TP_L is not tied Low, the default value of Register bit 16.0 = 1. The BGA15 package does not have a G_FX/TP_L hardware configuration pin.
4. The default value of Register bit 16.5 is determined by the PREASEL pin. The BGA15 package does not have a PREASEL hardware configuration pin and has a default of 0.
5. The BGA15 package does not support fiber. Default for the BGA15 package is 0.
6. NA means the bits do not have a default value and may initially contain any value.

Table 94 Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default [2]
15	Reserved	Write as 0, ignore on Read	R	0
14	10/100 Mode	0 = The LXT9785/LXT9785E is operating in 10 Mbps mode 1 = The LXT9785/LXT9785E is operating in 100 Mbps mode ***Note:*** The status is valid for TX and FX operation.	R	0
13	Transmit Status	0 = The LXT9785/LXT9785E is not transmitting a packet 1 = The LXT9785/LXT9785E is transmitting a packet	R LH	0
12	Receive Status	0 = Packet has not been received since last read 1 = Packet has been received since last read	R LH	0
11	Collision Status	0 = A collision is not occurring 1 = A collision is occurring ***Note:*** This bit is set when jabber is detected, regardless of duplex. Status is valid only when link is up.	R LH	0
10	Link	0 = Link is down 1 = Link is up	R	0
9	Duplex Mode	0 = Half-duplex 1 = Full-duplex	R	0
8	Auto-Negotiation	0 = The LXT9785/LXT9785E is in manual mode 1 = The LXT9785/LXT9785E is in auto-negotiation mode This signal is based upon Register bit 0.12.	R	Note 3

1. R = Read Only, LH = Latching High – cleared when read.
2. The default values are updated on completion of reset and reflect the status or change in status at that time. Cortina recommends that the register status be read on completion of reset.
3. The default value is determined by the default value of Register bit 0.12.
4. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
5. Default values are set by the hardware configuration PAUSE pin. The BGA15 package does not have a Pause hardware configuration pin. The default for the BGA15 package is 0.

Table 94 Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default [2]
7	Auto-Negotiation Complete	0 = Auto-negotiation process is not complete 1 = Auto-negotiation process is complete	R	0
6	FIFO Error	0 = No FIFO error occurred 1 = FIFO error occurred (overflow or underflow)	R LH	0
5	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed ***Note:*** During 100 Mbps operation, this bit is not valid and may vary. Auto MDIX activity may increase the variability.	R	0
4	Pause	0 = The LXT9785/LXT9785E is not Pause capable 1 = The LXT9785/LXT9785E is pause capable ***Note:*** This bit is not affected by Register bit 4.10. ***Note:*** The default for the BGA15 package is 0.	R	LSHR[4,5]
3	Error	0 = No error occurred 1 = Error Occurred (remote fault, RxERCntFUL, FIFO error, jabber, parallel detect fault) ***Note:*** The register is cleared when the registers that generated the error condition are read.	R	0
2:0	Reserved	Write as 0, ignore on Read.	R	0

1. R = Read Only, LH = Latching High – cleared when read.
2. The default values are updated on completion of reset and reflect the status or change in status at that time. Cortina recommends that the register status be read on completion of reset.
3. The default value is determined by the default value of Register bit 0.12.
4. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
5. Default values are set by the hardware configuration PAUSE pin. The BGA15 package does not have a Pause hardware configuration pin. The default for the BGA15 package is 0.

Table 95 Interrupt Enable Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
15:14[2]	RxFIFO Initial Fill	00 = Reserved 01 = Low, 16 bits 10 = Normal, 32 bits (default) 11 = Jumbo packets, 128 bits	R/W	LSHR[4,5]

1. R/W = Read/Write
2. In 10 Mbps operation, Register bit 18.13 = 1 cannot be used when Register bits 18.15:14 = “11” and in RMII mode, Registers bits 18.15:14 = “11” or “10” cannot be used because the minimum Inter Gap Packet becomes less than specified in the *IEEE 802.3 specification.
3. SFD Frame Alignment is applicable to SMII and SS-SMII only.
4. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset
5. Default values are set by hardware configuration pins FIFOSEL1 and FIFOSEL0 (see Table 17, *Receive FIFO Depth Considerations*, on page 50).

Table 95 Interrupt Enable Register (Address 18, Hex 12)

Bit	Name	Description		Type [1]	Default
13	SFD Frame Alignment[3] (RxDV asserts with CRS when enabled)	10 Mbps	When Register bit 16.5 = 1, preamble is not suppressed. 0 = Disabled 1 = Enabled When Register bit 16.5 = 0, SFD is always aligned, and preamble is suppressed.	R/W	0
		100 Mbps	0 = Disabled 1 = Enabled When enabled, all but one byte of preamble is suppressed.	R/W	0
12:9	Reserved	Write as 0, ignore on Read		R/W	0000
8	CNTRMSK	Mask for Counter Full 0 = Do not allow event to cause interrupt 1 = Enable event to cause interrupt		R/W	0
7	ANMSK	Mask for Auto-Negotiate Complete 0 = Do not allow event to cause interrupt 1 = Enable event to cause interrupt		R/W	0
6	SPEEDMSK	Mask for Speed Interrupt 0 = Do not allow event to cause interrupt 1 = Enable event to cause interrupt		R/W	0
5	DUPLEXMSK	Mask for Duplex Interrupt 0 = Do not allow event to cause interrupt 1 = Enable event to cause interrupt		R/W	0
4	LINKMSK	Mask for Link Status Interrupt 0 = Do not allow event to cause interrupt 1 = Enable event to cause interrupt		R/W	0
3	ISOLMSK	Mask for Isolate Interrupt 0 = Do not allow event to cause interrupt 1 = Enable event to cause interrupt		R/W	0
2	Reserved	Write as 0, ignore on Read		R/W	0
1	INTEN	0 = Disable interrupts on this port 1 = Enable interrupts on this port		R/W	0
0	TINT	0 = Normal operation 1 = Test force interrupt on MDINT_L		R/W	0

1. R/W = Read/Write
2. In 10 Mbps operation, Register bit 18.13 = 1 cannot be used when Register bits 18.15:14 = “11” and in RMII mode, Registers bits 18.15:14 = “11” or “10” cannot be used because the minimum Inter Gap Packet becomes less than specified in the *IEEE 802.3 specification.
3. SFD Frame Alignment is applicable to SMII and SS-SMII only.
4. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset
5. Default values are set by hardware configuration pins FIFOSEL1 and FIFOSEL0 (see Table 17, *Receive FIFO Depth Considerations*, on page 50).

Table 96 Interrupt Status Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default[2]
15:9	Reserved	Write as 0, ignore on Read	R	0
8	RxERCntFUL	**RxER Counter Full Status.** 0 = The internal counters have not reached maximum values 1 = One of the internal counters has reached its maximum value	R/LH	0
7	ANDONE	**Auto-Negotiation Status.** 0 = Auto-negotiation has not completed 1 = Auto-negotiation has completed	R/LH	N/A
6	SPEEDCHG	**Speed Change Status.** 0 = A speed change has not occurred since last reading this register 1 = A speed change has occurred since last reading this register	R/LH	0
5	DUPLEXCHG	**Duplex Change Status.** 0 = A duplex change has not occurred since last reading this register 1 = A duplex change has occurred since last reading this register	R/LH	0
4	LINKCHG	**Link Status Change Status.** 0 = A link change has not occurred since last reading this register 1 = A link change has occurred since last reading this register	R/LH	0
3	Isolate	**MII Isolate Change Status.** 0 = An Isolate change has not occurred since last reading this register 1 = An Isolate change has occurred since last reading this register	R/LH	0
2	MDINT	0 = Interrupt not pending 1 = Interrupt pending	R/LH	0
1:0	Reserved	Reserved	R	0

1. R = Read Only, LH = Latching High – cleared when read
2. The default values are updated on completion of reset and reflect the status or change in status at that time. Cortina recommends that the register status be read on completion of reset.

Table 97 LED Configuration Register (Address 20, Hex 14)

Bit	Name	Description	Type[1]	Default
15:12	LED1 Programming bits	0000 =Display Speed Status (Continuous, Default) 0001 =Display Transmit Status (Stretched) 0010 =Display Receive Status (Stretched) 0011 =Display Collision Status (Stretched) 0100 =Display Link Status (Continuous) 0101 =Display Duplex Status (Continuous) 0110 =Display Isolate Status (Continuous) 0111 = Display Receive or Transmit Activity (Stretched) 1000 =est mode- turn LED on (Continuous) 1001 =Test mode- turn LED off (Continuous) 1010 =Test mode- blink LED fast (Continuous) 1011 =Test mode- blink LED slow (Continuous) 1100 =Display Link and Receive Status combined[2] (Stretched)[3] 1101 =Display Link and Activity Status combined[2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined[4] (Stretched)[3] 1111 = Display Link and RxER Status combined[2] (Blink)	R/W	0000
11:8	LED2 Programming bits	0000 =Display Speed Status 0001 =Display Transmit Status 0010 =Display Receive Status 0011 =Display Collision Status 0100 =Display Link Status 0101 =Display Duplex Status 0110 =Display Isolate Status 0111 = Display Receive or Transmit Activity 1000 =Test mode- turn LED on 1001 =Test mode- turn LED off 1010 =Test mode- blink LED fast 1011 =Test mode- blink LED slow 1100 =Display Link and Receive Status combined[2] (Stretched)[3] 1101 =Display Link and Activity Status combined[2] (Default) (Stretched)[3] 1110 = Display Duplex and Collision Status combined[4] (Stretched)[3] 1111 = Display Link and RxER Status combined [2] (Blink)	R/W	1101

1. R/W = Read/Write
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive, Activity, or Error) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.

Table 97 LED Configuration Register (Address 20, Hex 14)

Bit	Name	Description	Type[1]	Default
7:4	LED3 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status 0011 = Display Collision Status 0100 = Display Link Status 0101 = Display Duplex Status 0110 = Display Isolate Status 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined[2] (Stretched)[3] 1101 = Display Link and Activity Status combined[2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined[4] (Default) (Blink)[3] 1111 = Display Link and RxER Status combined [2] (Blink)	R/W	1110
3:2	LEDFREQ	00 = Stretch LED events to 30 ms 01 = Stretch LED events to 60 ms 10 = Stretch LED events to 100 ms 11 = Reserved	R/W	00
1	PULSE-STRETCH	0 = Disable pulse stretching of all LEDs[3] 1 = Enable pulse stretching of all LEDs ***Note:*** Receive activity LEDs are initially active based upon carrier sense.	R/W	1
0	Reserved	Write as 0, ignore on Read	R/W	0

1. R/W = Read/Write
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive, Activity, or Error) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.

Table 98 Receive Error Count Register (Address 21, Hex 15)

Bit	Name	Description	Type[1]	Default
15:0	Receive Error Count	A 16-bit counter value indicating the number of times a receive packet with errors occurred. Only one event gets counted per packet. When maximum count is reached, the 16-bit counter remains full until cleared.	R/ LH	0x0000

1. R = Read Only, LH = Latching High – cleared when read

Note: Cortina recommends reading this register once every time link is established to clear the register.

Table 99 RMII Out-of-Band Signaling Register (Address 25, Hex 19)

Bit	Name	Description	Type[1]	Default
BGA15				
15:0	Reserved for BGA15	Write as 0, ignore on Read.	R/W	0x0000
PQFP and BGA23				
15:7	Reserved	Write as 0, ignore on Read	R/W	0x000
6:4	BIT1	These three bits select which status information is available on the RxData(1) bit of the RMII bus. 000 =Link 001 =Speed 010 =Duplex 011 =Auto-negotiation complete 100 =Polarity reversed 101 =Jabber detected 110 =Interrupt pending 111 = Reserved	R/W	000
3:1	BIT0	These three bits select which status information is available on the RxData(0) bit of the RMII bus. 000 =Link 001 =Speed 010 =Duplex 011 =Auto-negotiation complete 100 =Polarity reversed 101 =Jabber detected 110 =Interrupt pending 111 = Reserved	R/W	000
0	PROGRMII	0 = Disable Out-of-Band signaling. 1 = Enable programmable RMII Out-of-Band signaling. When enabled, Register bits 6:1 specify which status bits are available on the RMII RxData data bus. **Note:** Out-of-Band signaling is disabled when the Isolate mode is enabled by setting Register bit 0.10.	R/W	0

1. R/W = Read/Write

Note: The BGA15 package does not support RMII operation.

Table 100 Trim Enable Register (Address 27, Hex 1B)

Bit	Name	Description	Type[5]	Default
15:13	Reserved	Write as 0, ignore on Read	R	N/A
12	Reserved	Write as 0, ignore on Read.	R/W	0
11:10	Per-Port Rise Time Control	00 = 3.3 ns 01 = 3.6 ns 10 = 3.9 ns 11 = 4.2 ns ***Note:*** Values represent nominal load conditions.	R/W	LSHR[1,2]
9	AMDIX_EN	0 = Disable auto MDI/MDIX 1 = Enable auto MDI/MDIX	R/W	LSHR[1,3]
8	MDIX	0 = MDI, transmit on pair A (TPFIN*n*/TPFIP*n*) and receive on pair B (TPFON*n*/TPFOP*n*) 1 = MDIX transmit on pair B (TPFON*n*/TPFOP*n*) and receive on pair A (TPFIN*n*/TPFIP*n*) ***Note:*** Manual MDI/MDIX selection (This bit is ignored when Register bit 27.9 = 1). ***Note:*** BGA15 does not support the MDIX hardware configuration.	R/W	LSHR[1,4]
7	Analog Loopback	0 = Disable analog loopback 1 = Enable analog loopback (twisted-pair transmit outputs are active) ***Note:*** In fiber mode, SD for the port must be asserted.	R/W	0
6	Dis_EN	**DTE Discovery Process Enable.** 0 = Disable DTE discovery process 1 = Enable DTE discovery process Restart auto-negotiation after writing to this bit to ensure proper operation.	R/W	0
5	Reserved	Write as 0, ignore on Read.	R/W	0
4	Power_EN	**Power Enable (Requires Auto-Negotiation Enable Register bit 0.12 = 1).** 0 = Remote-Power DTE not discovered; process may not be complete. 1 = Potential Remote-Power DTE discovered; indication to turn on power over the cable.	R	0

1. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
2. Default values for Register bits 27.11:10 are determined by the TxSLEW pins.
3. Default value for Register bit 27.9 is determined by the AMDIX_EN pin.
4. Default value for Register bit 27.8 is determined by the MDIX pin. BGA15 does not support the MDIX hardware configuration. The BGA15 default = 0.
5. R/W = Read/Write, R = Read Only, LH = Latching High – cleared when read.

Table 100 Trim Enable Register (Address 27, Hex 1B)

Bit	Name	Description	Type[5]	Default
3	SLP_Det	**Standard Link Partner Detected.** 0 = Standard link partner not discovered; process may not be complete. 1 = Standard link partner discovered; indication not to turn on power over the cable. **Note:** This bit is only valid while link is down.	R, LH	0
2	LFIT Expired	**Link Fail Inhibit Timer expiration indicator. Valid only when SLP_Det = 1.** 0 = Link Fail Inhibit Timer has not expired or standard link partner not discovered 1 = Link Fail Inhibit Timer expired with a standard link partner detected since last register read or link establishment	R, LH	0
1:0	Reserved	Write as 0, ignore on Read.	R	00

1. LSHR = Default value is derived from a single device input pin state or a group of device input pin states as the pin(s) are latched at startup or hardware reset.
2. Default values for Register bits 27.11:10 are determined by the TxSLEW pins.
3. Default value for Register bit 27.9 is determined by the AMDIX_EN pin.
4. Default value for Register bit 27.8 is determined by the MDIX pin. BGA15 does not support the MDIX hardware configuration. The BGA15 default = 0.
5. R/W = Read/Write, R = Read Only, LH = Latching High – cleared when read.

Table 101 Cable Diagnostics Register (Address 29, Hex 1D)

Bit	Name	Description	Type[1]	Default[2]
15:14	Reserved	Write as 01, ignore on read	R/W	01
13:11	Start-Test	000 =Do not perform cable fault test (Default) 101 = Perform long cable fault test only 110 = Perform short cable fault test only Once Register bit 29.9 is set, the Start-Test bits will clear when read. Any other combination of the Register bit settings are reserved and should not be used.	R/W LH	000
10	CD_EN	0 = Normal operation 1 = Enable cable diagnostic tests. Forces link to drop.	R/W	0
9	Test_Done	0 = Testing is still in progress 1 = Testing is complete The Line Fault Counter and Fault_Type bits are valid.	R LH	0
8	Fault_Type	0 = Open condition has been detected 1 = Short Condition has been detected	R LH	0
7:0	Line Fault Counter	"FF" if no line fault is found, or Distance to fault, approximately 1 m * counter value (refer to Section 4.13, *Cable Diagnostics Overview*, on page 156 for details). (Valid only when Test_Done bit is set.)	R LH	0x00

1. R/W = Read/Write, R = Read only, LH = Latching High, cleared when read
2. Recommended default value.

Table 102 Register Bit Map

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Control Register (Address 0)																	
Control	Reset	Loopback	Speed Select	A/N Enable	Power Down	Isolate	Re-start A/N	Duplex Mode	COL Test	Speed Select	Reserved						0
Status Register (Address 1)																	
Status	100Base-T4	100Base-X Full-Duplex	100Base-X Half-Duplex	10 Mbps Full-Duplex	10 Mbps Half-Duplex	100Base-T2 Full-Duplex	100Base-T2 Half-Duplex	Extended Status	Reserved	MF Preamble Suppress	A/N Complete	Remote Fault	A/N Ability	Link Status	Jabber Detect	Extended Capability	1
PHY ID Registers (Address 2 and 3)																	
PHY ID 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	2
PHY ID2	PHY ID No						MFR Model No						MFR Rev No			Model Variant	3
Auto-Negotiation Advertisement Register (Address 4)																	
A/N Advertise	Next Page	Reserved	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full-Duplex	100Base-TX	10Base-T Full-Duplex	10Base-T	IEEE Selector Field					4
Auto-Negotiation Link Partner Base Page Ability Register (Address 5)																	
A/N Link Ability	Next Page	Ack	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full-Duplex	100Base-TX	10Base-T Full-Duplex	10Base-T	IEEE Selector Field					5
Auto-Negotiation Expansion Register (Address 6)																	
A/N Expansion	Reserved										Base Page	Parallel Detect Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner A/N Able	6
Auto-Negotiation Next Page Transmit Register (Address 7)																	
A/N Next Page Txmit	Next Page	Reserved	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											7
Auto-Negotiation Link Partner Next Page Ability Register (Address 8)																	
A/N Link Next Page	Next Page	Ack	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											8
Port Configuration Register (Address 16)																	

Table 102 Register Bit Map

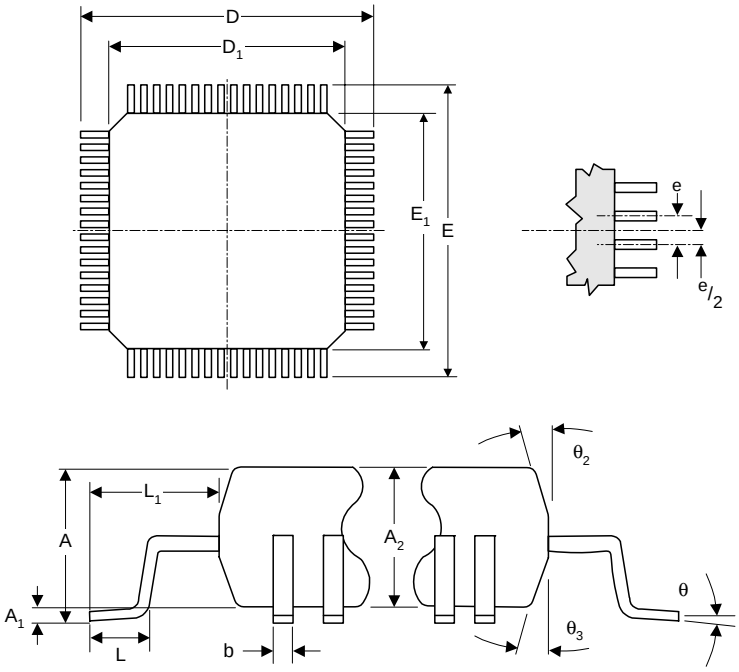
Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Port Config	Reserved	Link Disable	Txmit Disable	Bypass Scrambler (100BASE-TX)	Bypass 4B/5B (100BASE-TX)	Jabber (10T)	SQE (10T)	TP Loopback (10T)	Reserved	Reserved	PRE_EN	Reserved	Reserved	Far End Fault Enable	Reserved	Fiber Select	16
Quick Status Register (Address 17)																	
Quick Status	Reserved	10/100 Mode	Transmit Status	Receiver Status	Collision Status	Link	Duplex Mode	Auto-Neg	Auto-Neg Complete	FIFO Error	Polarity	Pause	Error	Reserved	Reserved	Reserved	17
Interrupt Enable Register (Address 18)																	
Interrupt Enable	Reserved							Counter Mask	Auto-Neg Mask	Speed Mask	Duplex Mask	Link Mask	Isolate Mask	Reserved	Interrupt Enable	Test Interrupt	18
Interrupt Status Register (Address 19)																	
Interrupt Status	Reserved							RxER Counter Full	Auto-Neg Done	Speed Change	Duplex Change	Link Change	Isolate Change	MD Interrupt	Reserved	Reserved	19
LED Configuration Register (Address 20)																	
LED Config	LED1				LED2				LED3				LED Freq		Pulse Stretch	Reserved	20
Receive Error Count Register (Address 21)																	
Rcv Error Count	Receive Error Count																21
Programmable RMII Out-of-Band Signaling Register (Register 25)																	
RMII OOB Signaling	Reserved									Bit 1			Bit 0			Program RMII	25
Trim Enable Register (Address 27)																	
Trim Enable	Reserved				Per Port Rise Time Control		AMDIX_EN	MDIX	Analog Loopback	Dis_EN	Loop Back Speed Up Enable	Power_EN	SLP_Det	LFIT Expired	Reserved		27
Cable Diagnostics Register (Address 29)																	
Cable Diagnostics	Reserved		Start-Test			CD_EN	Test-Done	Fault_ Type	Line Fault Counter								29

8.0 Package Specifications

Figure 64 208-Pin PQFP Plastic Package Specification

208-Pin Plastic Quad Flat Package

- Part Number LXT9785HC, LXT9785EHC, LXT9785HE
- Commercial Temperature Range (0 °C to 70 °C)
- Extended Temperature Range (-40 °C to +85 °C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

Figure 65 241-Ball BGA23 Package Specificationss - Top/Side Views (LXT9785BC)

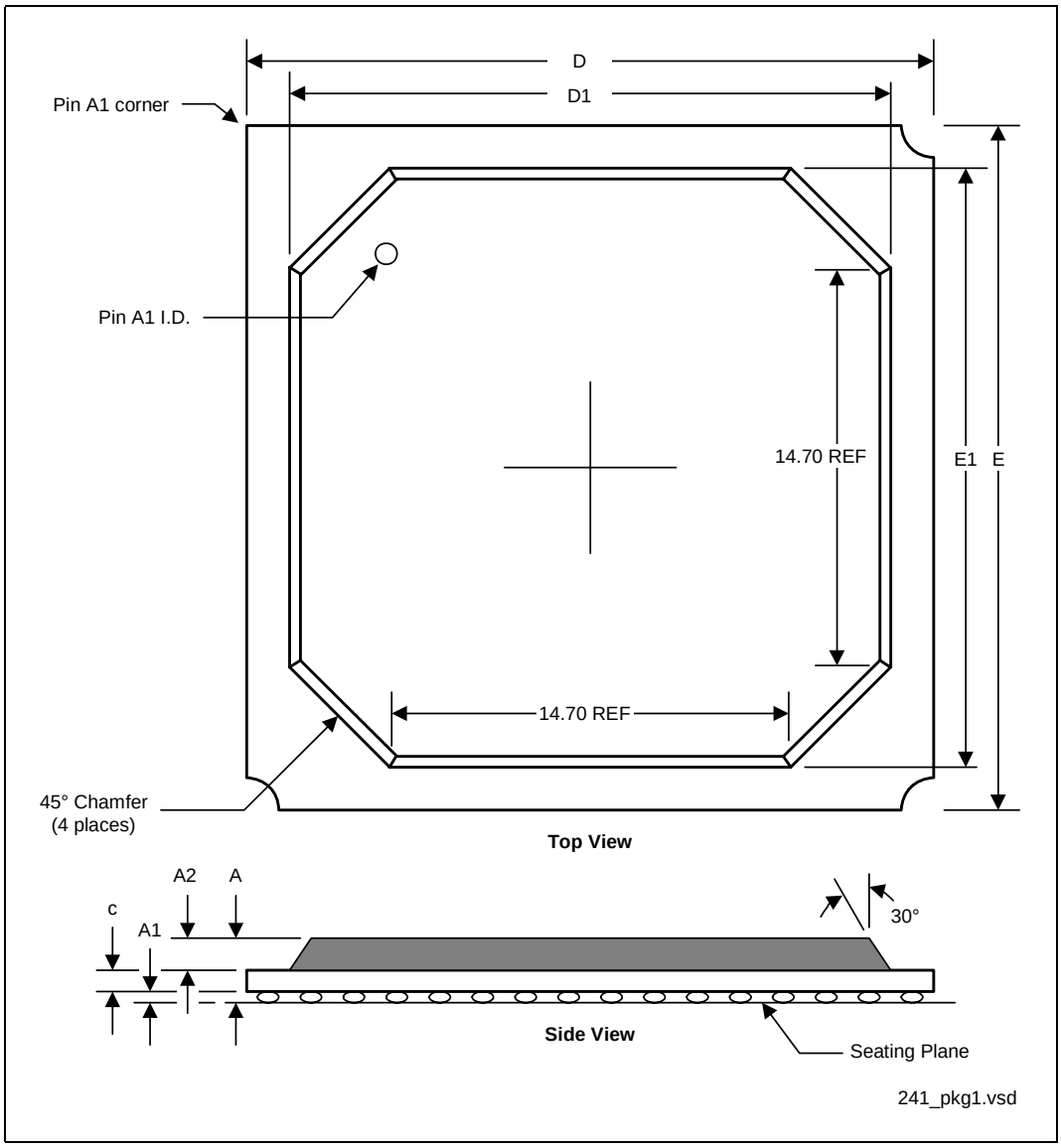


Figure 66 241-Ball BGA23 Package Specificationss - Bottom View (LXT9785BC)

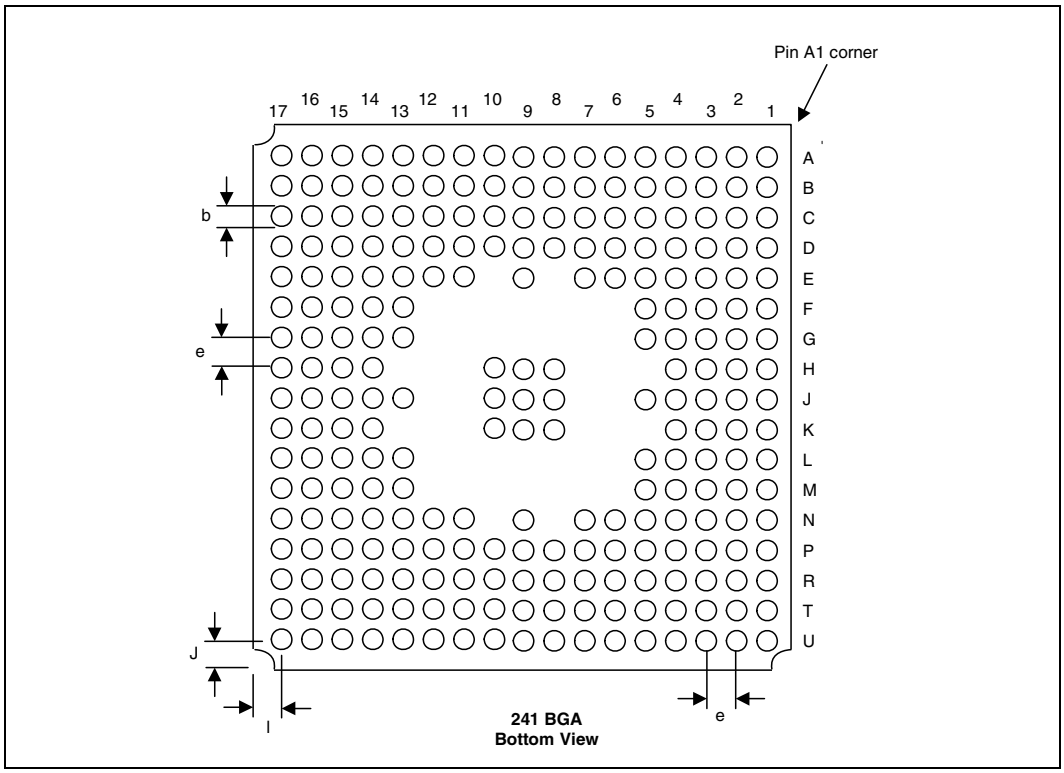


Table 103 241-Ball BGA23 Package Dimensions

Symbol	Min	Nominal	Max	Units
A	2.19	2.38	2.57	mm
A1	0.50	0.60	0.70	mm
A2	1.12	1.17	1.22	mm
D	22.90	23.00	23.10	mm
D1	19.30	19.50	19.70	mm
E	22.90	23.00	23.10	mm
E1	19.30	19.50	19.70	mm
e	1.27 (solder ball pitch)			mm
I	1.34 REF.			mm
J	1.34 REF.			mm
M	17 x 17 Matrix			mm
Note: All dimensions and tolerances conform to ANSI Y14.5-1982. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-). Primary datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.				

Table 103 241-Ball BGA23 Package Dimensions

Symbol	Min	Nominal	Max	Units
b	0.60	0.75	0.90	mm
c	0.52	0.56	0.60	mm
e		1.27		mm

Note: All dimensions and tolerances conform to ANSI Y14.5-1982. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-). Primary datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.

Figure 67 196-Ball BGA15 Package Specs - Top/Side Views (LXT9785MBC)

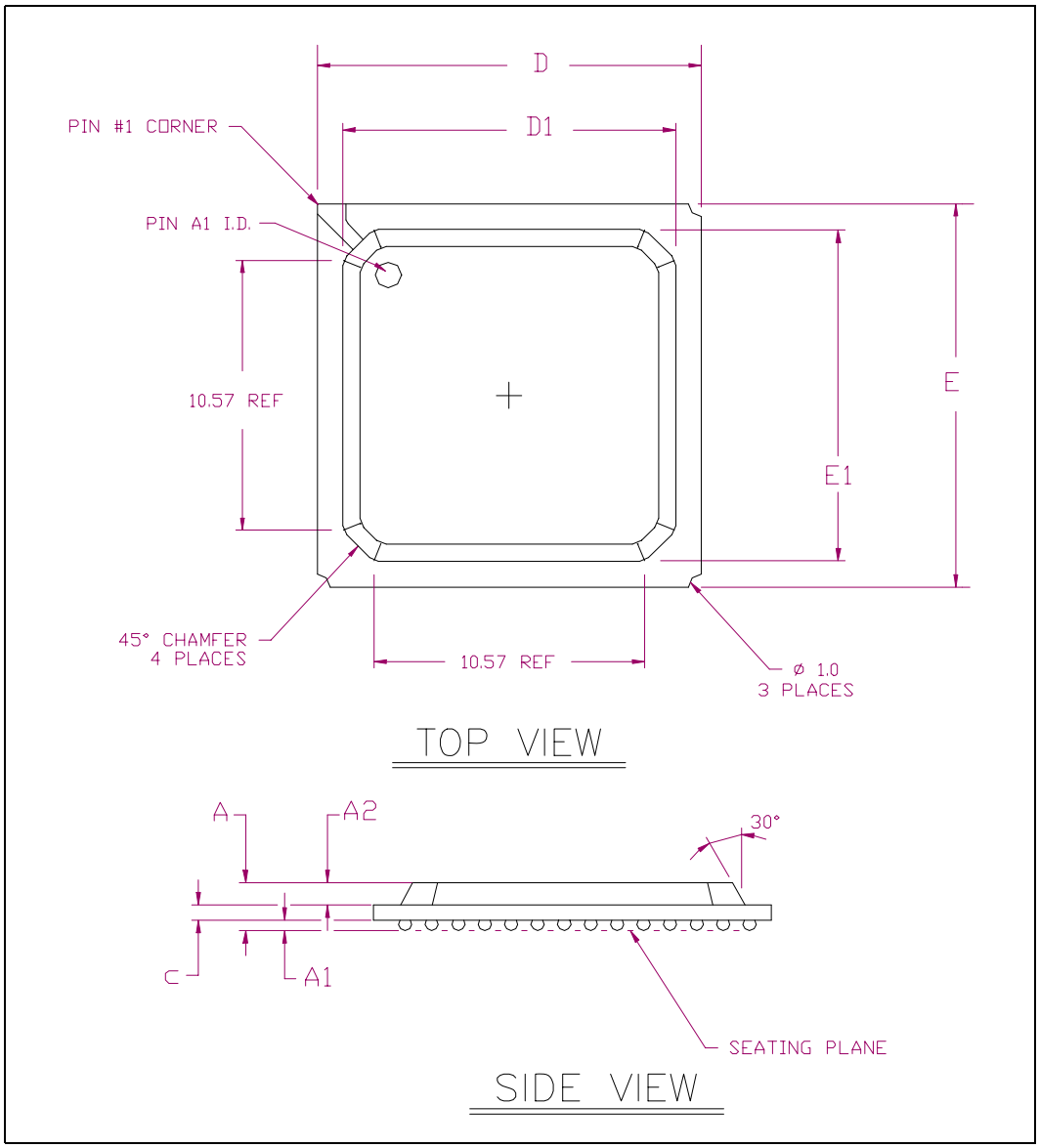


Figure 68 196-Ball BGA15 Package – Bottom View (LXT9785MBC)

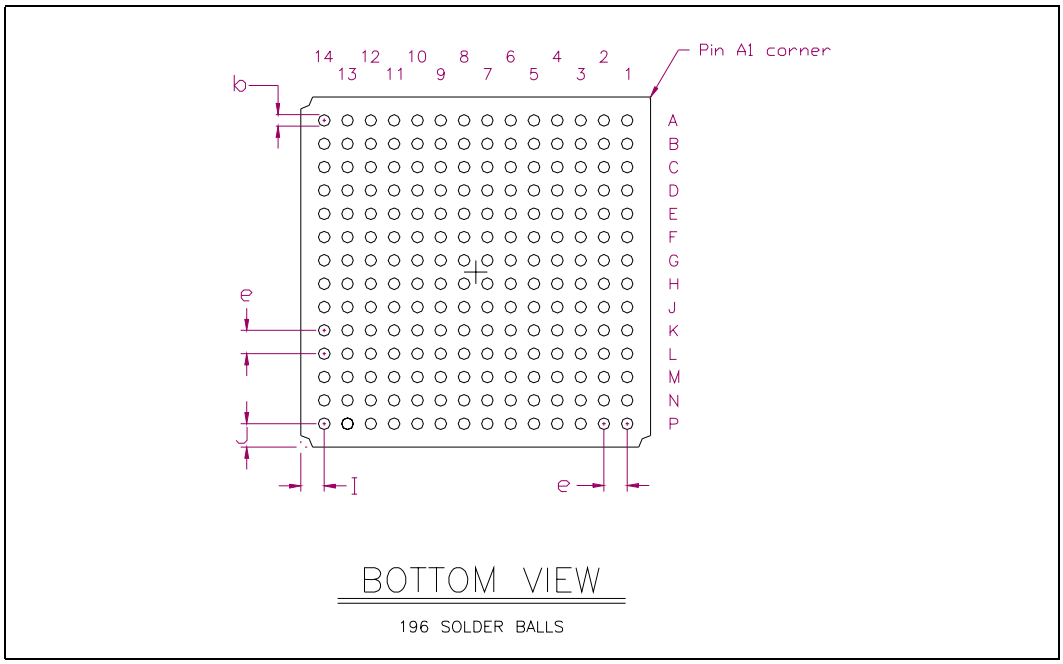


Table 104 196-Ball BGA15 Package Dimensions (LXT9785MBC)

Symbol	Min	Nominal	Max	Units
A	1.62	1.81	2.00	mm
A1	0.30	0.40	0.50	mm
A2	0.80	0.85	0.90	mm
D	14.90	15.00	15.10	mm
D1	12.80	13.00	13.20	mm
E	14.90	15.00	15.10	mm
E1	12.80	13.00	13.20	mm
e	1.00 (solder ball pitch)			mm
I	1.00 REF.			mm
J	1.00 REF.			mm
M	14 x 14 Matrix			mm
b	0.40	0.50	0.60	mm
c	0.52	0.56	0.60	mm
e		1.00		mm

Note: All dimensions and tolerances conform to ANSI Y14.5-1982.Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-). Primary datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.

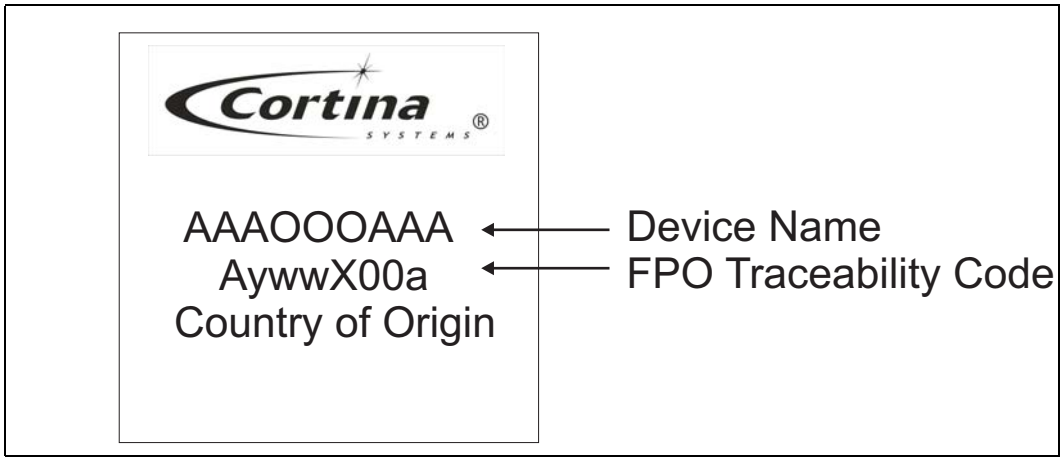
8.1 Top Label Markings

Figure 69 shows a sample PBGA package for the LXT9785/LXT9785E (Part numbers: FWLXT9785BC.C2V, FWLXT9785BC.D0 [241-Pin]).

Notes:

1. In contrast to the Pb-Free (RoHS-compliant) PBGA package, the non-RoHS-compliant package does not have the “e1” symbol in the last line of the package label.
2. Further information regarding RoHS and lead-free components can be obtained from your local Cortina representative.

Figure 69 Example of Top Marking Information Labeled as Cortina Systems, Inc.



Earlier versions of the silicon may be marked as either Intel* or Level One Communications* as shown in the examples in Figure 70 and Figure 71.

Figure 70 Example of Top Marking Information Labeled as Intel Corporation*

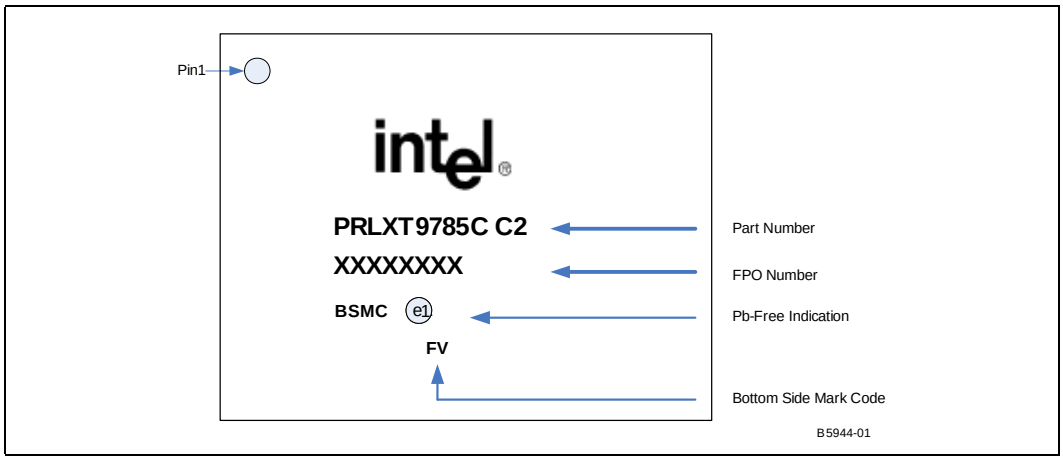
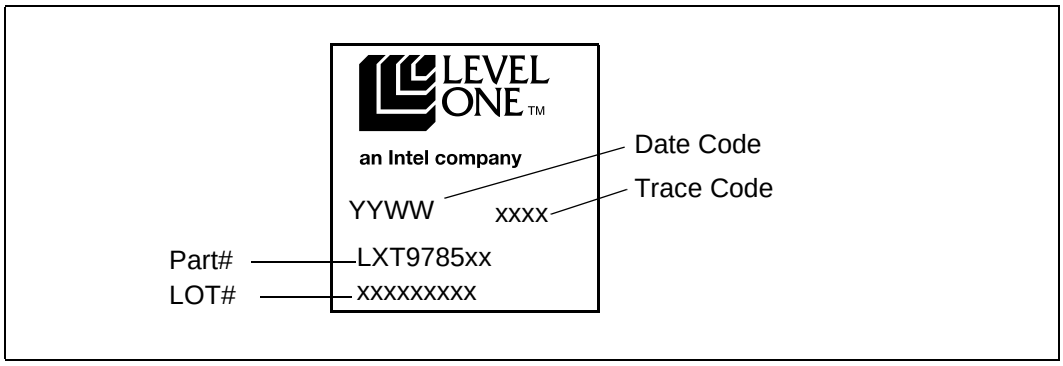


Figure 71 Example of Top Marking Information Labeled as Level One Communications*



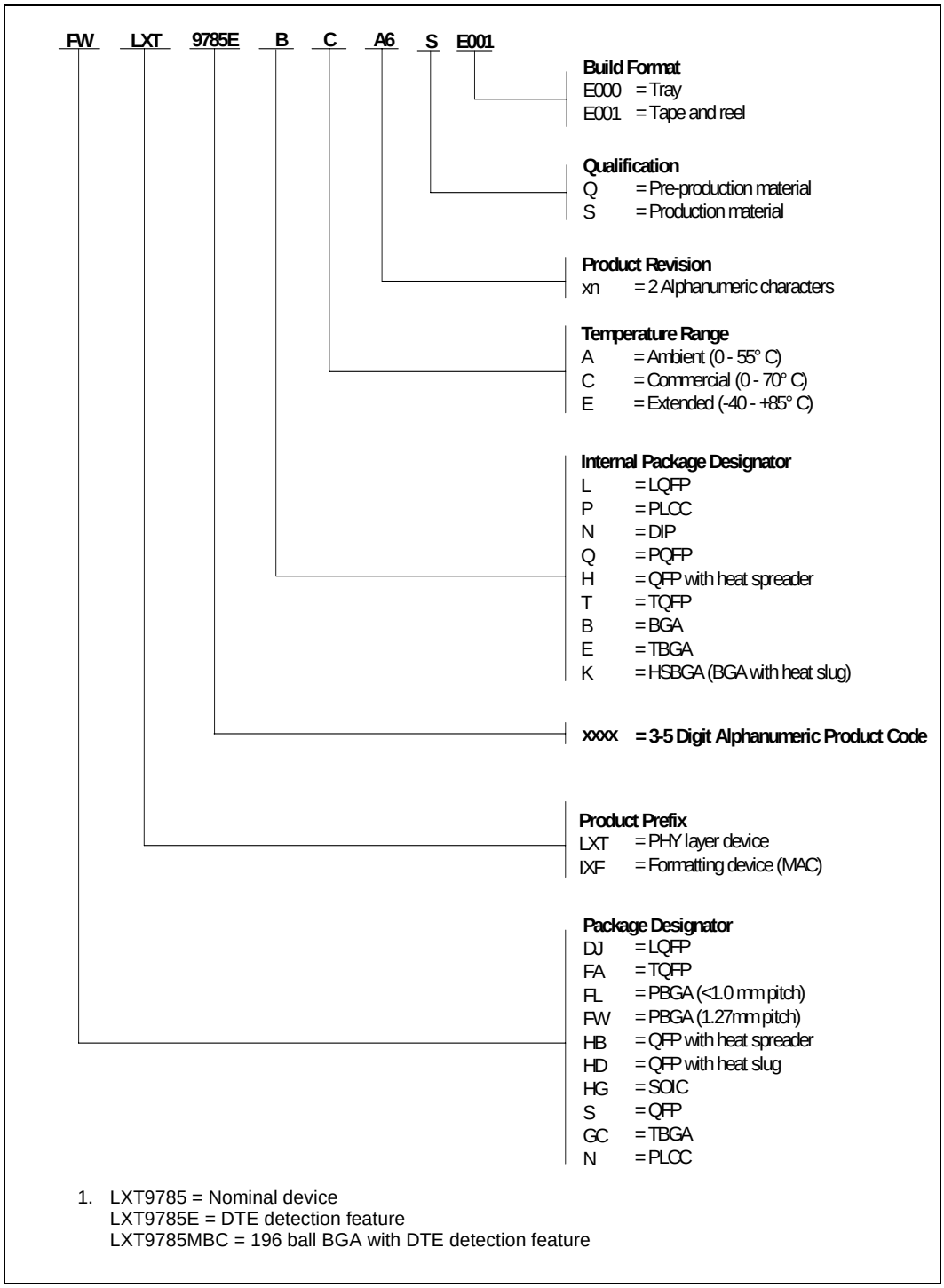
9.0 Ordering Information

Table 105 and Figure 72 provide product ordering information.

Table 105 Product Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
FWLXT9785BC.D0	D0	PBGA	241	No
PRLXT9785BC.D0	D0	PBGA	241	Yes
FWLXT9785EBC.D0	D0	PBGA	241	No
PRLXT9785EBC.D0	D0	PBGA	241	Yes
FWLXT9785BC.C2V	C2V	PBGA	241	No
PRLXT9785BC.C2V	C2V	PBGA	241	Yes
FWLXT9785EBC.C2V	C2V	PBGA	241	No
PRLXT9785EBC.C2V	C2V	PBGA	241	Yes
GDLXT9785MBC.D0	D0	PBGA	196	No
LULXT9785MBC.D0	D0	PBGA	196	Yes
HBLXT9785HC.D0	D0	HQFP	208	No
WBLXT9785HC.D0	D0	HQFP	208	Yes
HBLXT9785EHC.D0	D0	HQFP	208	No
WBLXT9785EHC.D0	D0	HQFP	208	Yes
HBLXT9785HE.D0	D0	HQFP	208	No
WBLXT9785HE.D0	D0	HQFP	208	Yes
HBLXT9785EHC.C2V	C2V	HQFP	208	No
WBLXT9785EHC.C2V	C2V	HQFP	208	Yes
HBLXT9785HC.C2V	C2V	HQFP	208	No
WBLXT9785HC.C2V	C2V	HQFP	208	Yes
HBLXT9785HE.C2V	C2V	HQFP	208	No
WBLXT9785HE.C2V	C2V	HQFP	208	Yes

Figure 72 Ordering Information - Sample



1. LXT9785 = Nominal device
   LXT9785E = DTE detection feature
   LXT9785MBC = 196 ball BGA with DTE detection feature

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