VRAM MODULE

256K x 32 DRAM WITH 512 x 32 SAM

NEW VRAM MODULE

FEATURES

- Proposed industry-standard pinout in a 104-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Low power, 40mW standby; 1,200mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Dual-port organization: 256K x 32 DRAM port
  512 x 32 SAM port
- 512-cycle refresh distributed across 16.7ms
- FAST-PAGE-MODE access cycle
- No refresh required for serial access memory

SPECIAL FUNCTIONS

- NONPERSISTENT MASKED WRITE
- BLOCK WRITE
- SPLIT READ TRANSFER

OPTIONS MARKING

- Timing (DRAM, SAM [cycle/access])
  70ns, 22/22ns -7
  80ns, 25/25ns -8

- Packages
  Leadless 104-pin SIMM M

- Part Number Example: MT4V25632M-7

PIN ASSIGNMENT (Top View)
104-Pin SIMM
(SDF-1)

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	27	SQ8	53	DQ18	79	A7
2	QSF0	28	Vss	54	DQ19	80	A8
3	RAS0	29	NC	55	DQ20	81	NC
4	PRD0	30	NC	56	DQ21	82	Vss
5	CAS1	31	CAS2	57	DQ22	83	DQ25
6	PRD1	32	DQ9	58	DQ23	84	DQ26
7	DSF	33	DQ10	59	DQ24	85	DQ27
8	DQ1	34	DQ11	60	Vcc	86	DQ28
9	DQ2	35	DQ12	61	SQ17	87	DQ29
10	DQ3	36	DQ13	62	SQ18	88	DQ30
11	DQ4	37	DQ14	63	SQ19	89	DQ31
12	DQ5	38	DQ15	64	SQ20	90	DQ32
13	DQ6	39	DQ16	65	SQ21	91	Vcc
14	DQ7	40	Vcc	66	SQ22	92	SQ25
15	DQ8	41	SQ9	67	SQ23	93	SQ26
16	TR/OE	42	SQ10	68	SQ24	94	SQ27
17	SE0	43	SQ11	69	NC	95	SQ28
18	SC	44	SQ12	70	CAS4	96	SQ29
19	Vcc	45	SQ13	71	Vss	97	SQ30
20	SQ1	46	SQ14	72	A0	98	SQ31
21	SQ2	47	SQ15	73	A1	99	SQ32
22	SQ3	48	SQ16	74	A2	100	Vss
23	SQ4	49	Vss	75	A3	101	PRD2
24	SQ5	50	ME/WE	76	A4	102	PRD3
25	SQ6	51	CAS3	77	A5	103	PRD4
26	SQ7	52	DQ17	78	A6	104	PRD5

GENERAL DESCRIPTION

The MT4V25632 is a high-speed, multiport CMOS dynamic random access memory module containing 262,144 words organized in a x32 configuration. The module may be accessed either by a 32-bit wide DRAM port or by a 512 x 32-bit serial access memory (SAM) port. Data may be transferred from the DRAM to the SAM. The module consists of four 256K x 8, dual-port dynamic RAMs mounted on a 104-pin SIMM, FR4 printed circuit board.

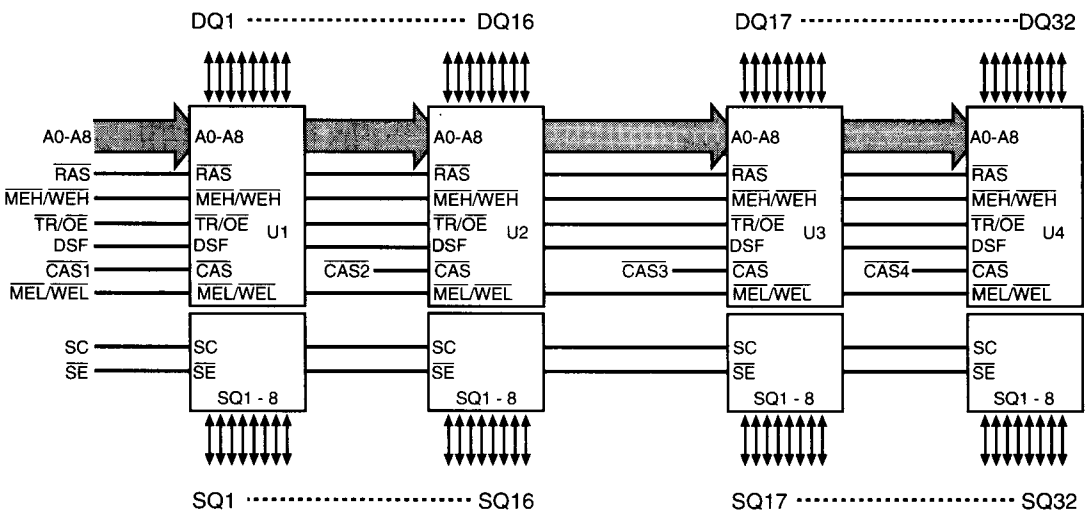
The DRAM portion of the VRAM components is functionally similar to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE and BLOCK WRITE. Thirty two 512-bit data registers make up the serial access memory portion on the VRAM module. Data I/O and internal data transfer are accomplished using three separate data paths for each component on the module: the 32-bit random access I/O port, the eight internal 512-bit-wide paths between the DRAM and the SAM, and the 32-bit serial output port for the SAM.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally to each component. As with all DRAM modules, the VRAM module must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh

cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT4V25632 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE allow further enchancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



U1 - U4 = MT42C8255DJ

PRESENCE DETECT

SYMBOL	-7	-8
PRD0	Vss	Vss
PRD1	Vss	Vss
PRD2	NC	NC
PRD3	Vss	NC
PRD4	NC	NC
PRD5	NC	NC

PIN DESCRIPTIONS

MODULE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
18	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
16	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z state.
50	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM and READ TRANSFER ($\overline{ME/WE}$ = H) to the SAM.
17	$\overline{SE0}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial output buffers and allows a serial READ operation to occur; otherwise, the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when $\overline{SE}$ is inactive (HIGH).
7	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
3	$\overline{RAS0}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 9 row-address bits and strobe the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycle.
5, 31, 51, 70	$\overline{CAS1-4}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits and strobe the DSF input (BLOCK WRITE only).
72-80	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 32-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A8 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address during SPLIT READ TRANSFER.
8-15, 32-39, 52-59,83-90	DQ1-DQ32	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
20-27, 41-48, 61-68, 92-99	SQ1-SQ32	Output	Serial Data Out: Output or High-Z.
2	QSF0	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
19, 40, 60, 91	V_{CC}	Supply	Power Supply: +5V ±10%
1, 28, 49, 71, 82, 100	V_{SS}	Supply	Ground

NEW VRAM MODULE

FUNCTIONAL DESCRIPTION

The MT4V25632 can be divided into three functional blocks (see Functional Block Diagram): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the TR/(OE) pin will be shown as TR/(OE) in references to transfer operations.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory module, the MT4V25632 VRAM module must be refreshed to retain data. All 512 row-address combinations must be accessed within 16.7ms. The MT4V25632 supports CBR, RAS-ONLY and HIDDEN types of refresh cycles.

For the CBR cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, but must simply perform 512 CBR cycles within the 16.7ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CBR cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CBR cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT4V25632 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES

The DRAM portion of the VRAM module is similar to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits used to select an 32-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when CAS goes from HIGH to LOW.

Note: *RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.*

For standard single-port DRAMs, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, TR/(OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CBR, where it is "don't care").

A DRAM READ operation is performed if (ME)/WE is HIGH when CAS goes LOW and remains HIGH until CAS goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ32 port. The (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For standard single-port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/WE performs two functions; write mask enable and data write enable. ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

MASKED WRITE

The MASKED WRITE (RWM) feature eliminates the need for a READ-MODIFY-WRITE cycle when changing individual bits within a 32-bit word. When $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT4V25632 supports the nonpersistent mode of MASKED WRITE. In this mode, mask data must be entered with every $\overline{RAS}$ falling edge. The data (mask data) present on the DQ1-DQ32 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ32 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ32 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle.

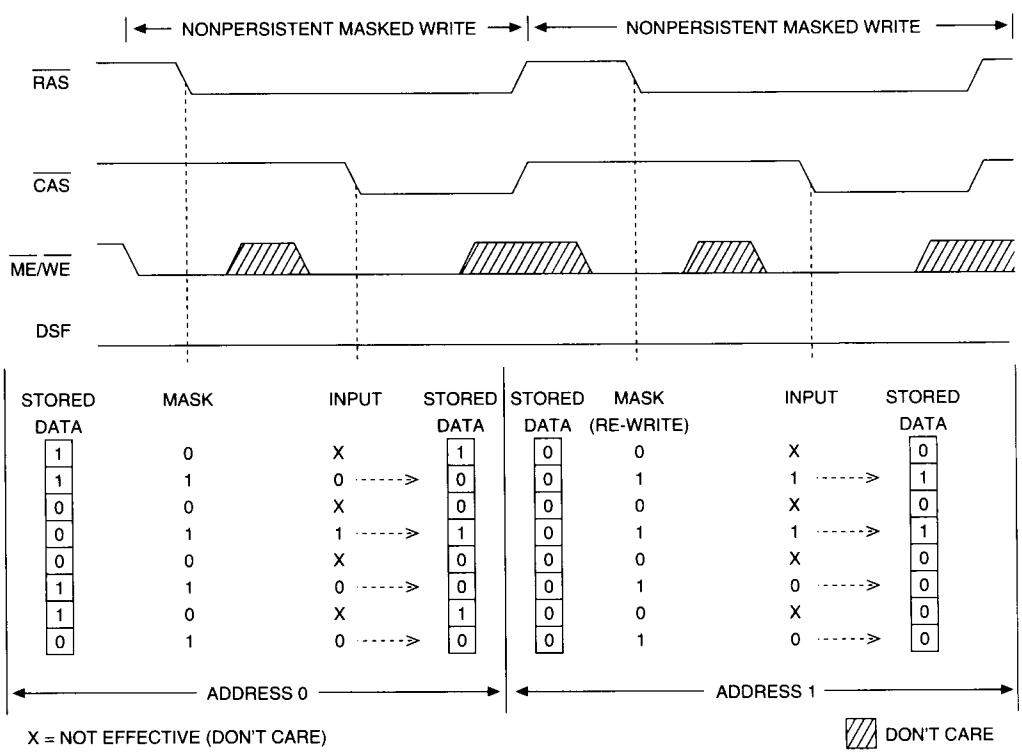


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE
(PER VRAM COMPONENT)

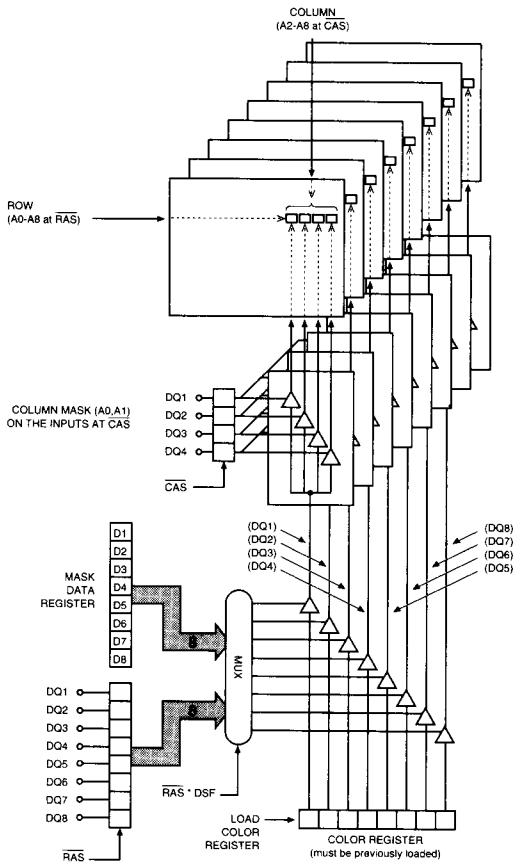


Figure 2
BLOCK WRITE EXAMPLE
(PER VRAM COMPONENT)

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT4V25632 will perform a BLOCK WRITE (BW) cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 2). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

MASKED BLOCK WRITE

The MASKED WRITE functions may be used during BLOCK WRITE cycles. MASKED BLOCK WRITE (BWM) operates exactly like the normal MASKED WRITE except the mask is now applied to the 32 bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a nonpersistent MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{CAS}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BLOCK WRITE, any combination of the 32 bit-planes may be masked, along with any combination of the four column locations.

	COLUMN ADDRESS CONTROLLED	
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

LOAD COLOR REGISTER

A LOAD COLOR REGISTER (LCR) cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the 32-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of theTRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER (RT) cycle is selected. The row-address bits indicate which 32 of the 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column-address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every RT in order to load a valid Tap address. An RT may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC, (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW and the actual data

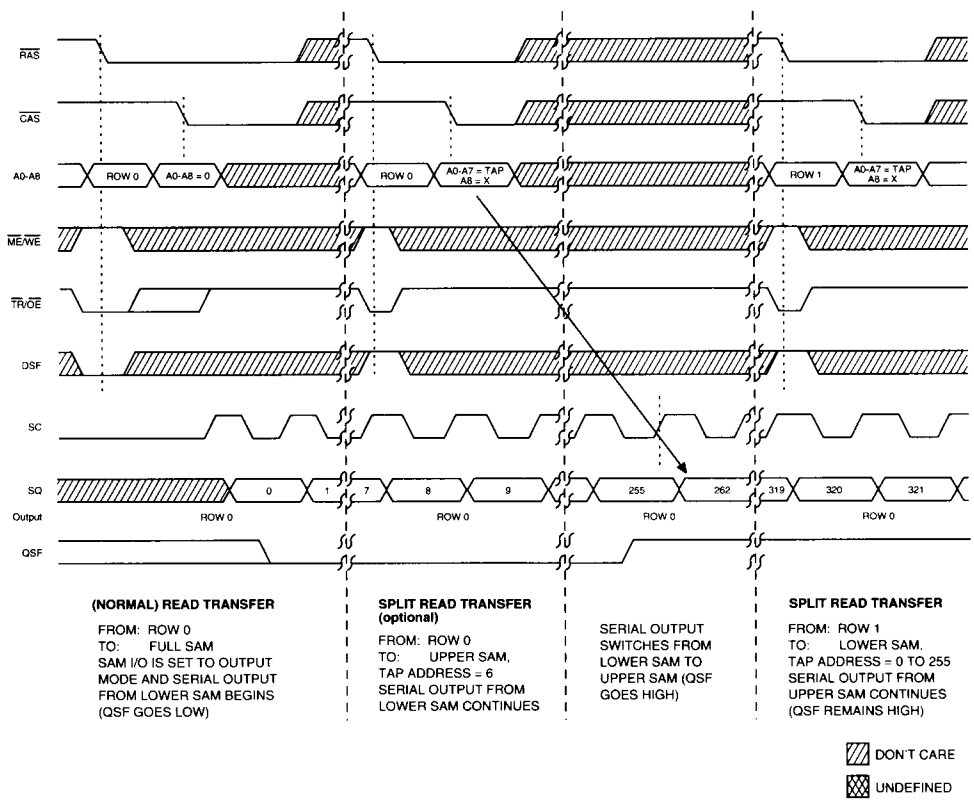


Figure 3
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers, and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER must occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer is not synchronized with the serial clock and may occur at any time while the other half is outputting data.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and, therefore, is independent of the falling edge of $\overline{CAS}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF). Then an SRT may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of $\overline{CAS}$. It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 3 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need be done only if the Tap for the upper half is ≠ 0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1) the QSF output goes HIGH. If an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 3 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode. The access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 4).

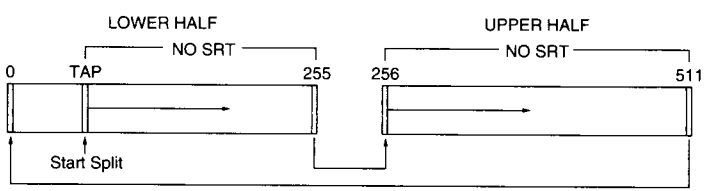


Figure 4
SPLIT SAM TRANSFER

SERIAL OUTPUT

The control inputs for serial output are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SRT cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 32-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 4. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

POWER-UP and INITIALIZATION

After V_{CC} is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS}$ = $\overline{TR}$/ $\overline{OE}$ ≥ V_{IH} during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT4V25632 module is completely static in operation and does not require refresh or initialization. The SAM port will power-up with the output pins (SQs) in High- Z, regardless of the state of $\overline{SE}$. QSF initializes in the LOW state. The color register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE				CAS FALL	A0-A8[1]		DQ1-DQ32[2]		REGISTER
		CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS,WE[3]	COLOR
	DRAM OPERATIONS										
CBR	CAS-BEFORE-RAS REFRESH	0	X	1[6]	1[6]	—	X	X	—	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	—	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	X	VALID DATA	X
RWM	MASKED WRITE TO DRAM (NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK	VALID DATA	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	X	COLUMN MASK	USE
BWM	MASKED BLOCK WRITE TO DRAM (NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	USE
	REGISTER OPERATIONS										
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW[4]	X	X	REG DATA	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ32 inputs when RAS falls and when CAS falls.
3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but a ROW address is not required.
5. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for the lower half, 511 for the upper half).
6. The MT4V25632 does not require a "1" on these pins, but to ensure compatibility with other 2 Meg VRAM function sets, it is recommended.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-40	40	µA	
OUTPUT LEAKAGE CURRENT (DQ, SQ disabled, 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	1
Output Low Voltage (IOUT = 2.5mA)	VOL		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		24	pF	2
Input Capacitance: $\overline{RAS}$, ME/$\overline{WE}$, TR/$\overline{OE}$, SC, $\overline{SE}$, DSF	CI2		32	pF	2
Input Capacitance: $\overline{CAS}$1-4	CI3		8	pF	2
Input/Output Capacitance: DQ1-32, SQ1-32	CI/O		10	pF	2
Output Capacitance: QSF	CO		10	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	Icc1	500	440	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN], other inputs ≥ VIH or ≤ VIL)	Icc2	460	400	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ VIH or ≤ VIL)	Icc3	40	40	mA	4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = VIH)	Icc4	500	440	mA	3, 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc5	500	440	mA	3, 5
SAM/DRAM DATA TRANSFER	Icc6	135	120	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC [MIN])	Icc7	700	640	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL; $\overline{CAS}$ = Cycling: ^tPC = ^tPC [MIN])	Icc8	660	600	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles [MIN]; other inputs ≥ VIH or ≤VIL)	Icc9	240	240	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = VIH)	Icc10	700	640	mA	3, 4 25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	Icc11	700	640	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	Icc12	185	170	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	tRWC	175		190		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		45		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	90		95		ns	
Access time from $\overline{RAS}$	tRAC		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		20		25	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	tOE		20		20	ns	
Access time from column-address	tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		ns	
$\overline{CAS}$ precharge time	tCP	10		10		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	55	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		ns	
Row-address setup time	tASR	0		0		ns	
Row-address hold time	tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		ns	
Column-address hold time	tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	35		40		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	
Output buffer turn-off delay from $\overline{CAS}$	tOFF	3	20	3	20	ns	20,23
Output disable delay from ($\overline{TR}$)/$\overline{OE}$	tOD	3	10	3	10	ns	20,23
Output disable hold time from start of WRITE	tOEH	10		10		ns	27
Output Enable to $\overline{RAS}$ delay	tROH	0		0		ns	

NEW VRAM MODULE

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Transition time (rise or fall)	^tT		35		35	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ setup time	tTLS	0		0		ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time	tTLH	15	10,000	15	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	tRTH	65	10,000	70	10,000	ns	
$\overline{TR}/(\overline{OE})$ LOW to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	tCTH	25		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ precharge time	tTRP	50		60		ns	
$\overline{TR}/(\overline{OE})$ precharge time	tTRW	20		25		ns	
$\overline{TR}/(\overline{OE})$ HIGH to SC lead time	tTSL	5		5		ns	
First SC edge to $\overline{TR}/(\overline{OE})$ HIGH delay time	tTSD	15		15		ns	
SC to $\overline{RAS}$ setup time	tSRS	25		30		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ setup time	tYS	0		0		ns	
$\overline{TR}/(\overline{OE})$ HIGH to $\overline{RAS}$ hold time	tYH	15		15		ns	
DSF to $\overline{RAS}$ setup time	tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	tRFH	15		15		ns	
SC to QSF delay time	tSQD		25		30	ns	
SPLIT TRANSFER setup time	tSTS	25		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		ns	
DSF (at $\overline{CAS}$ LOW) to $\overline{RAS}$ hold time	tFHR	45		55		ns	
DSF to $\overline{CAS}$ setup time	tFSC	0		0		ns	
DSF to $\overline{CAS}$ hold time	tCFH	15		15		ns	
$\overline{TR}/\overline{OE}$ to QSF delay time	tTQD		25		25	ns	
$\overline{RAS}$ to QSF delay time	tRQD		75		75	ns	
$\overline{CAS}$ to QSF delay time	tCQD		35		35	ns	
$\overline{RAS}$ to first SC delay	tRSD	80		80		ns	
$\overline{CAS}$ to first SC delay	tCSD	30		30		ns	

NEW VRAM MODULE

NEW VRAM MODULE

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5V ±10%)

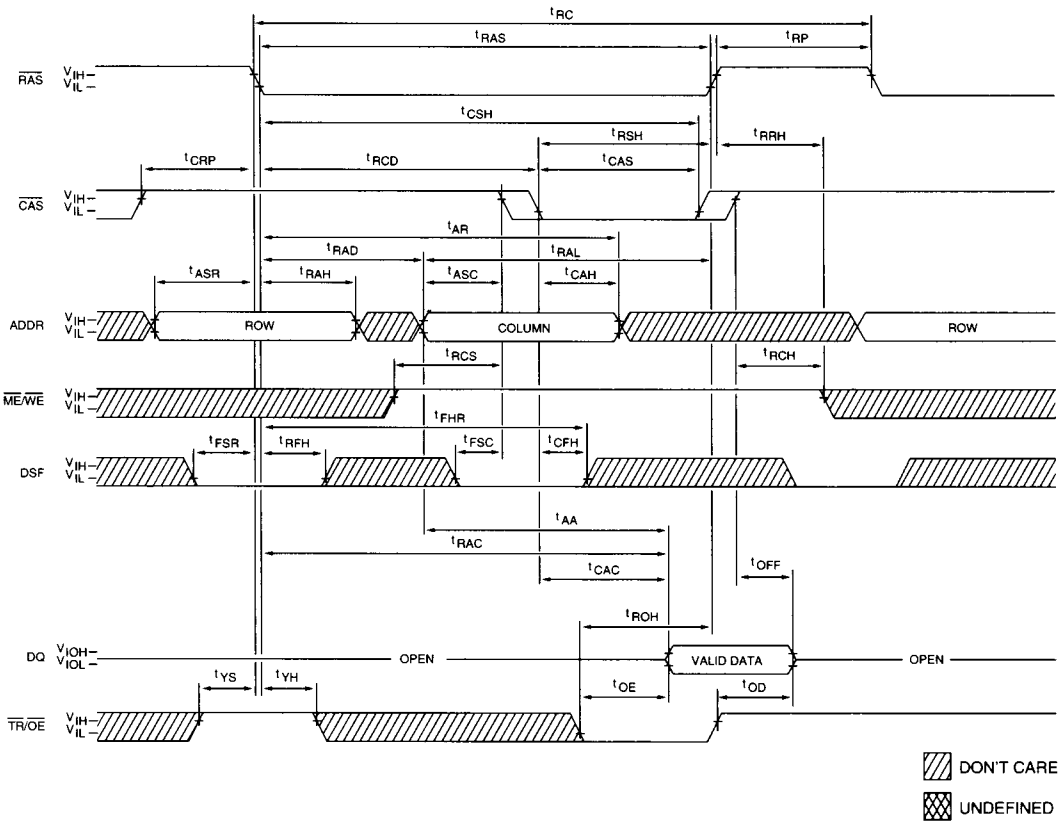
AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	22		25		ns	
Access time from SC	^tSAC		22		25	ns	24, 28
SC precharge time (SC LOW time)	^tSP	8		10		ns	
SC pulse width (SC HIGH time)	^tSAS	8		10		ns	
Access time from $\overline{SE}$	^tSEA		15		15	ns	24
$\overline{SE}$ precharge time	^tSEP	8		10		ns	
$\overline{SE}$ pulse width	^tSE	8		10		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	3	12	3	12	ns	20, 24

NOTES

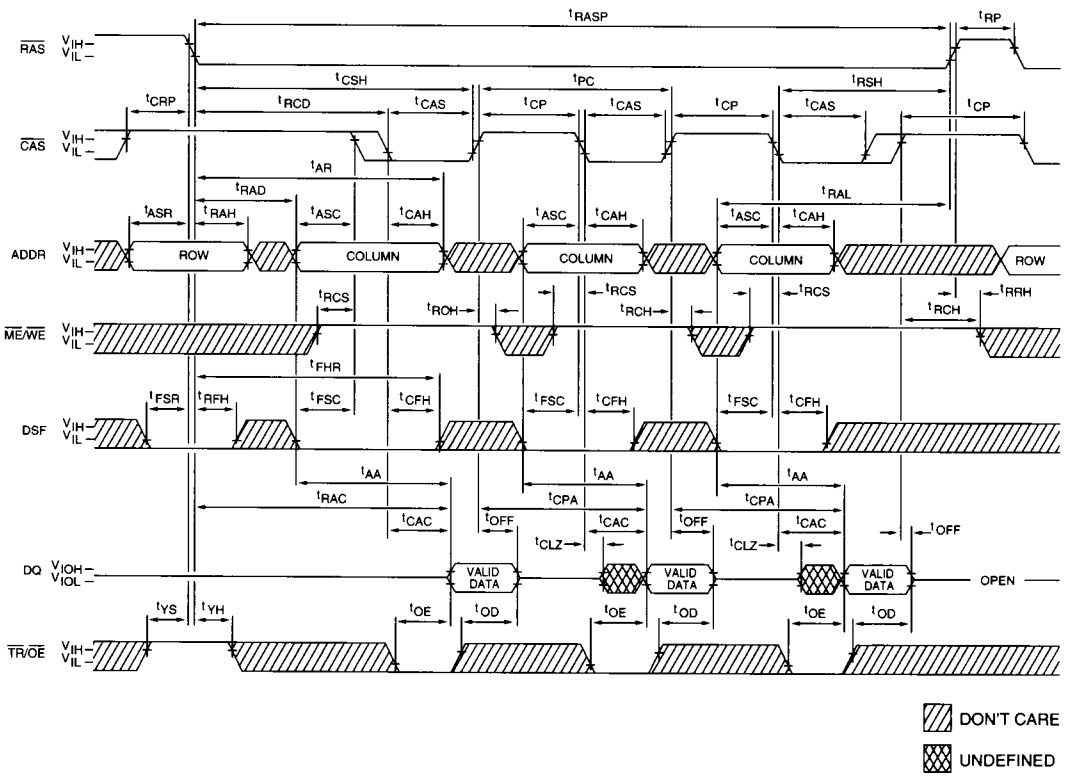
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16.7ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}). Input signals transition from 0 to 3V for AC testing.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ32) is High-Z.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ32) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (V_{OH} -200mV, V_{OL} +200mV). This parameter is sampled and not 100 percent tested.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the WRITE to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. Address (A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
26. Address (A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ($^tSOH = ^tSAC$ - output transition time); this is guaranteed by design.

NEW VRAM MODULE

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST-PAGE-MODE.

NEW VRAM MODULE

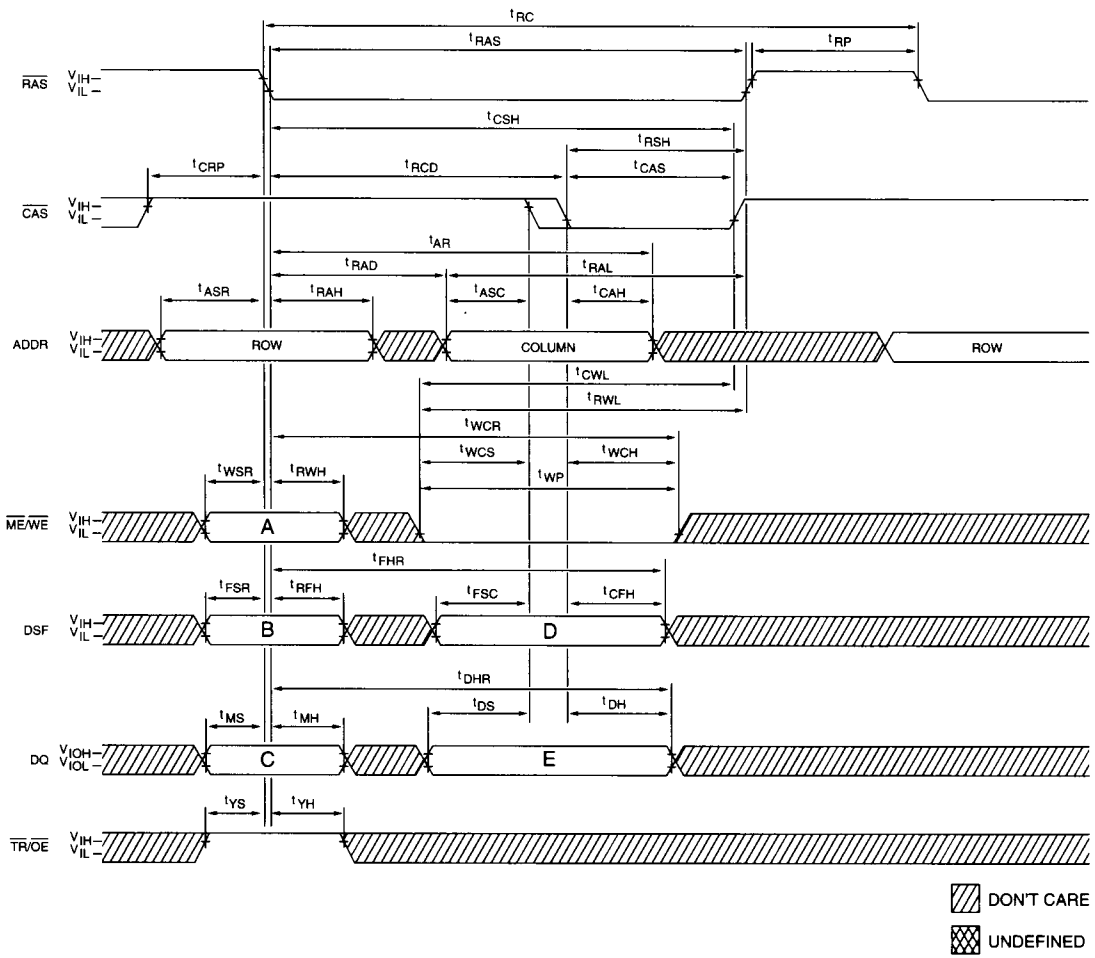
WRITE CYCLE FUNCTION TABLE [1]

FUNCTION	LOGIC STATES				
	RAS Falling Edge			CAS Falling Edge	
	A ME/WE	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)
Normal DRAM WRITE	1	0	X	0	DRAM Data
MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask
MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask
Load Color Register	1	1	X	1	Color Data

NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. CAS or ME/WE falling edge, whichever occurs later.

NEW VRAM MODULE

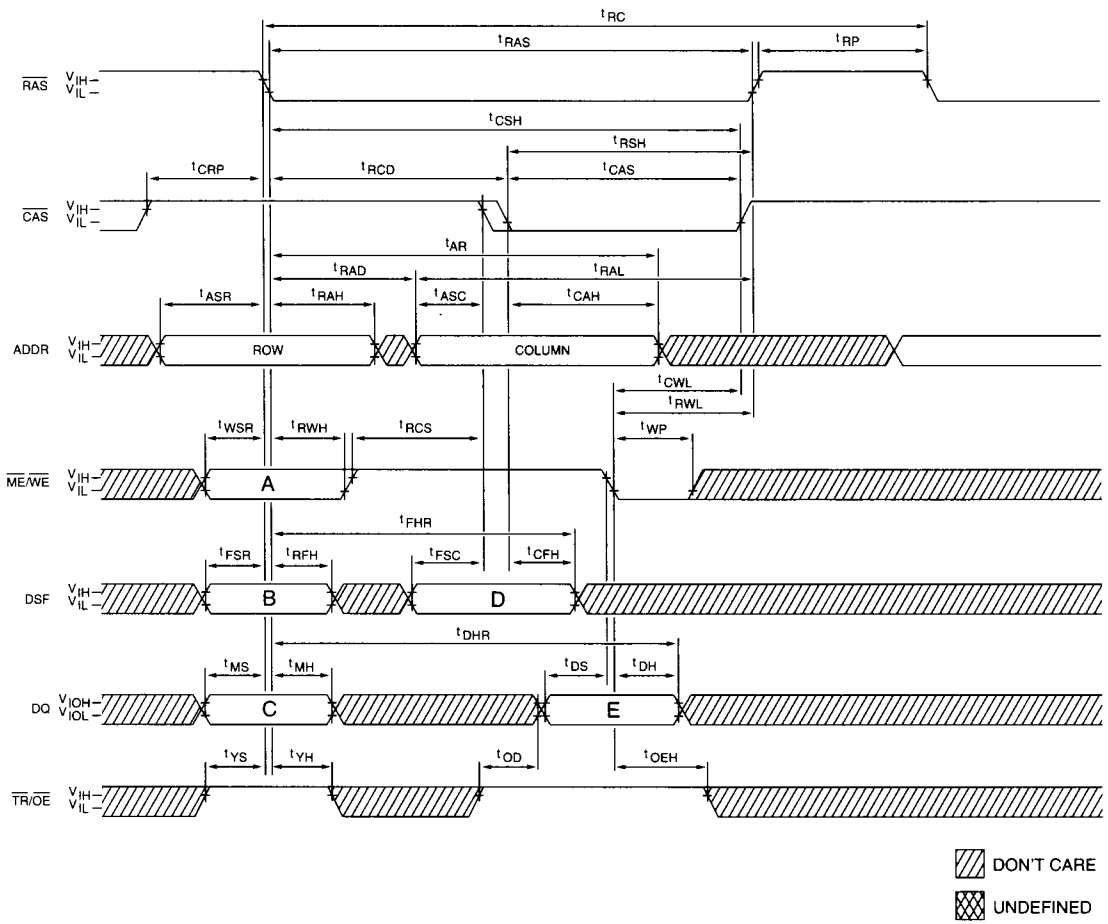
DRAM EARLY-WRITE CYCLE [1]



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

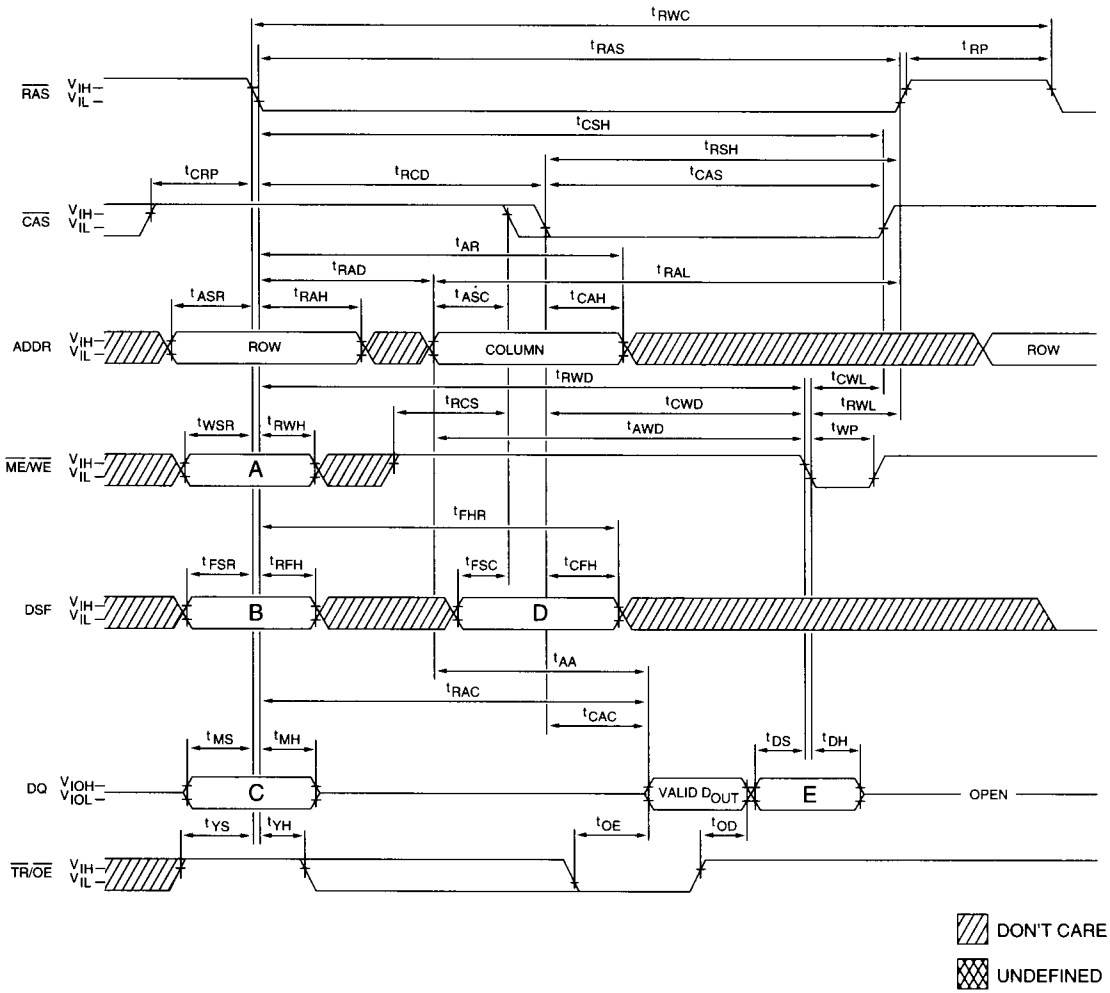
NEW VRAM MODULE

DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

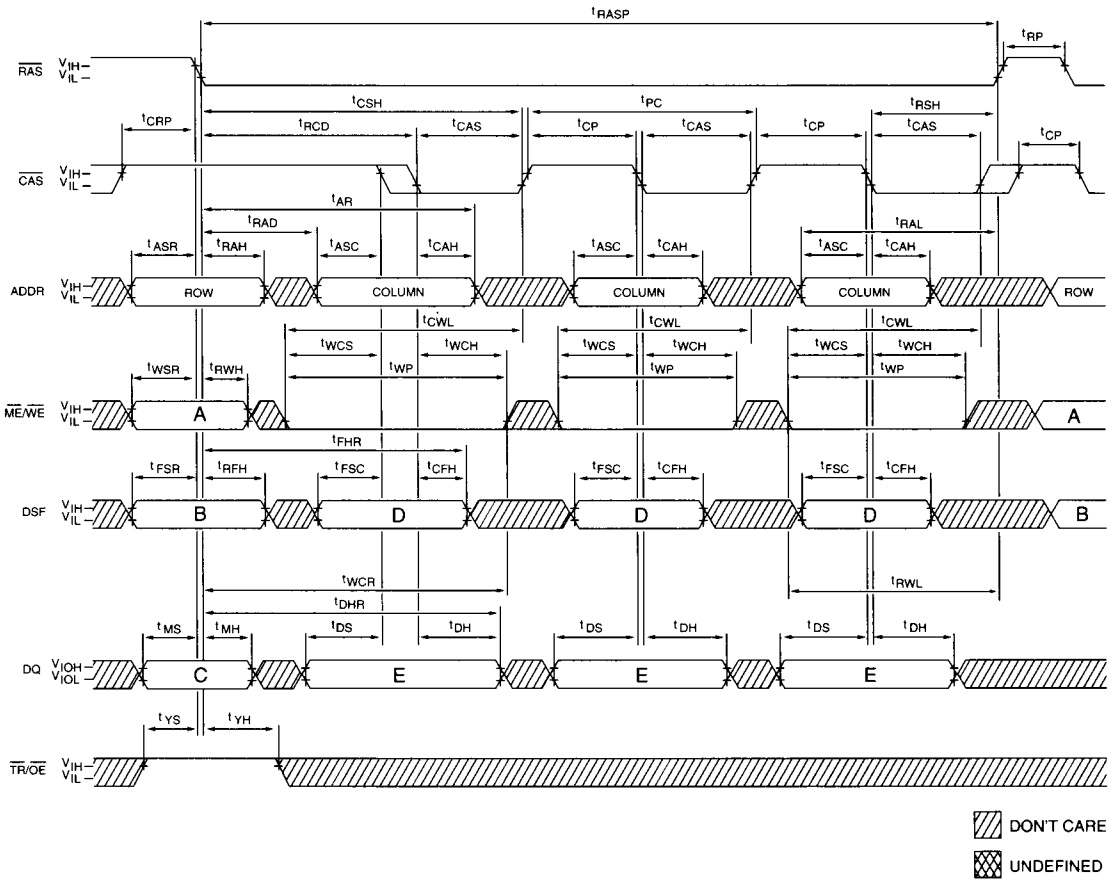
DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

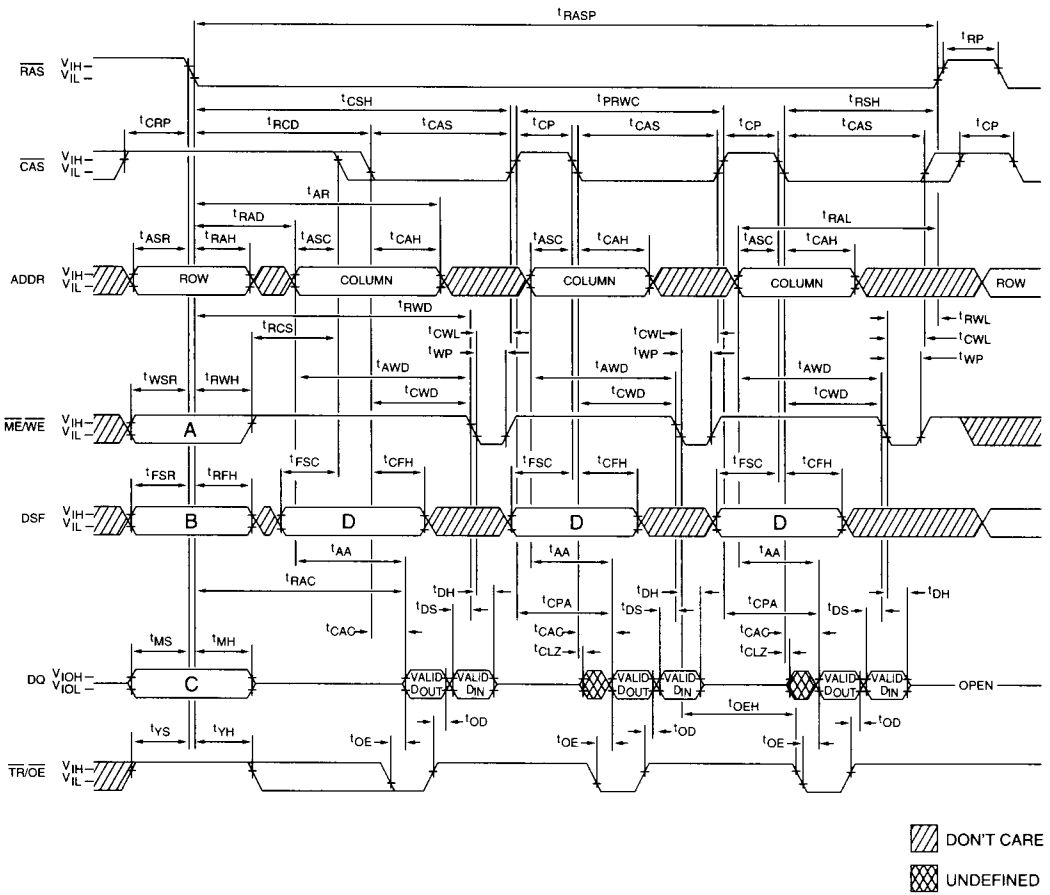
NEW VRAM MODULE

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST-PAGE-MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

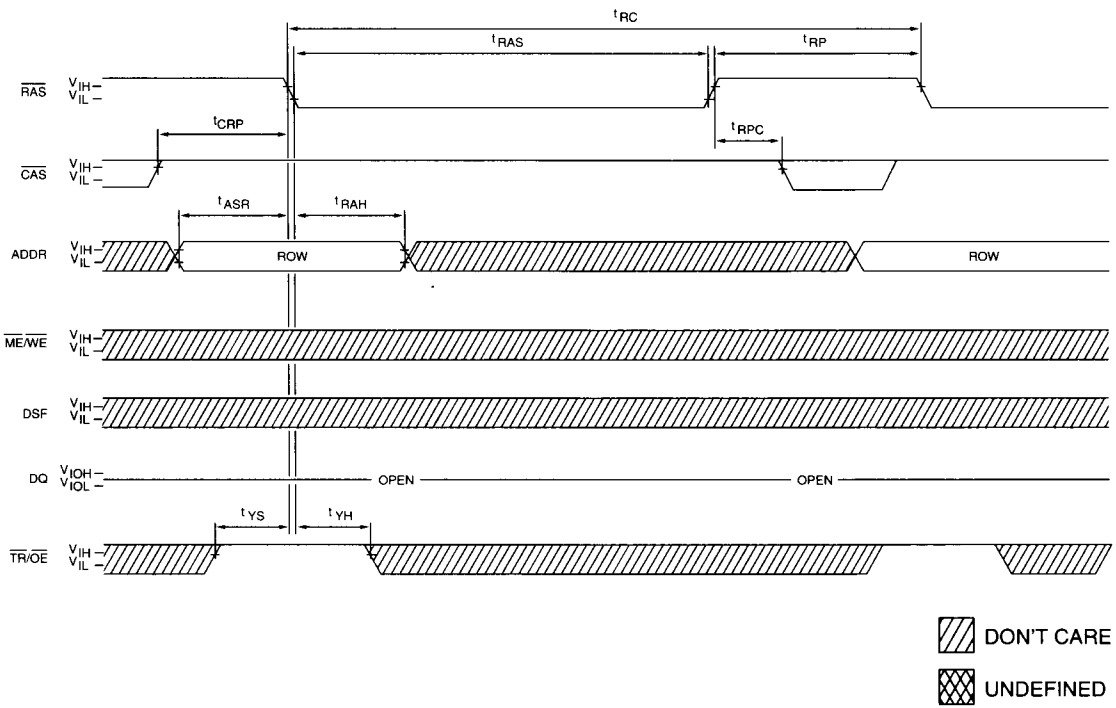
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



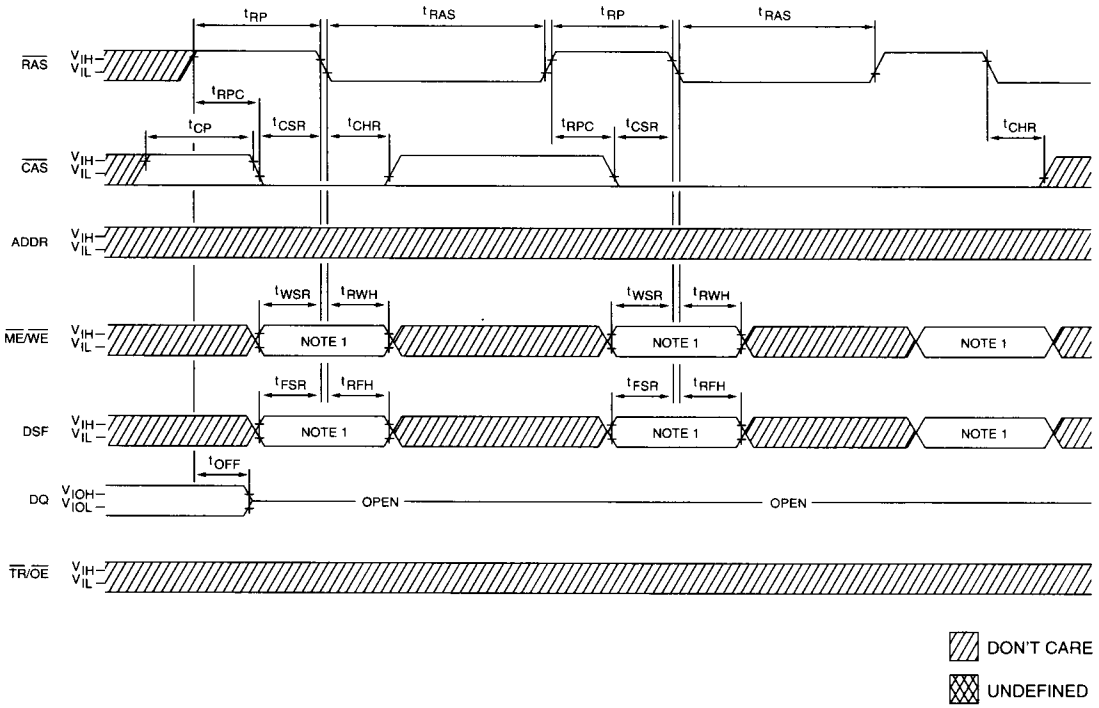
NOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST-PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" , "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

NEW VRAM MODULE

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

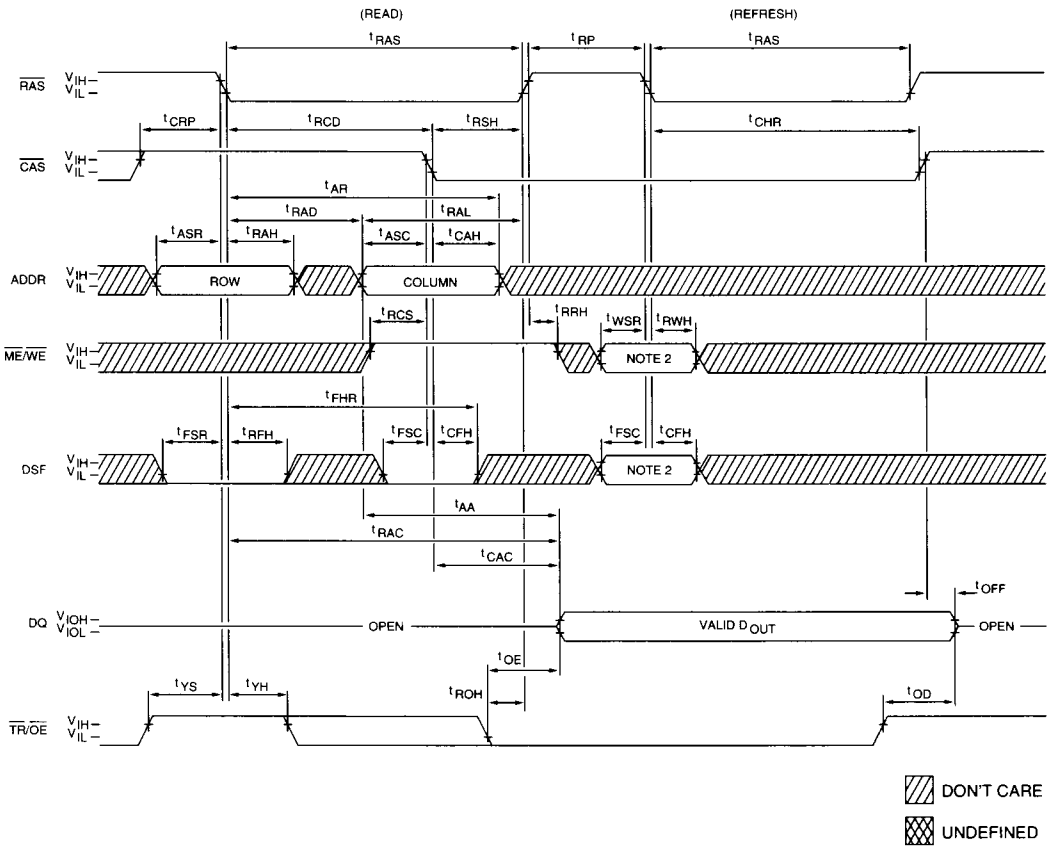


CBR REFRESH CYCLE



NOTE: 1. The MT4V25632 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

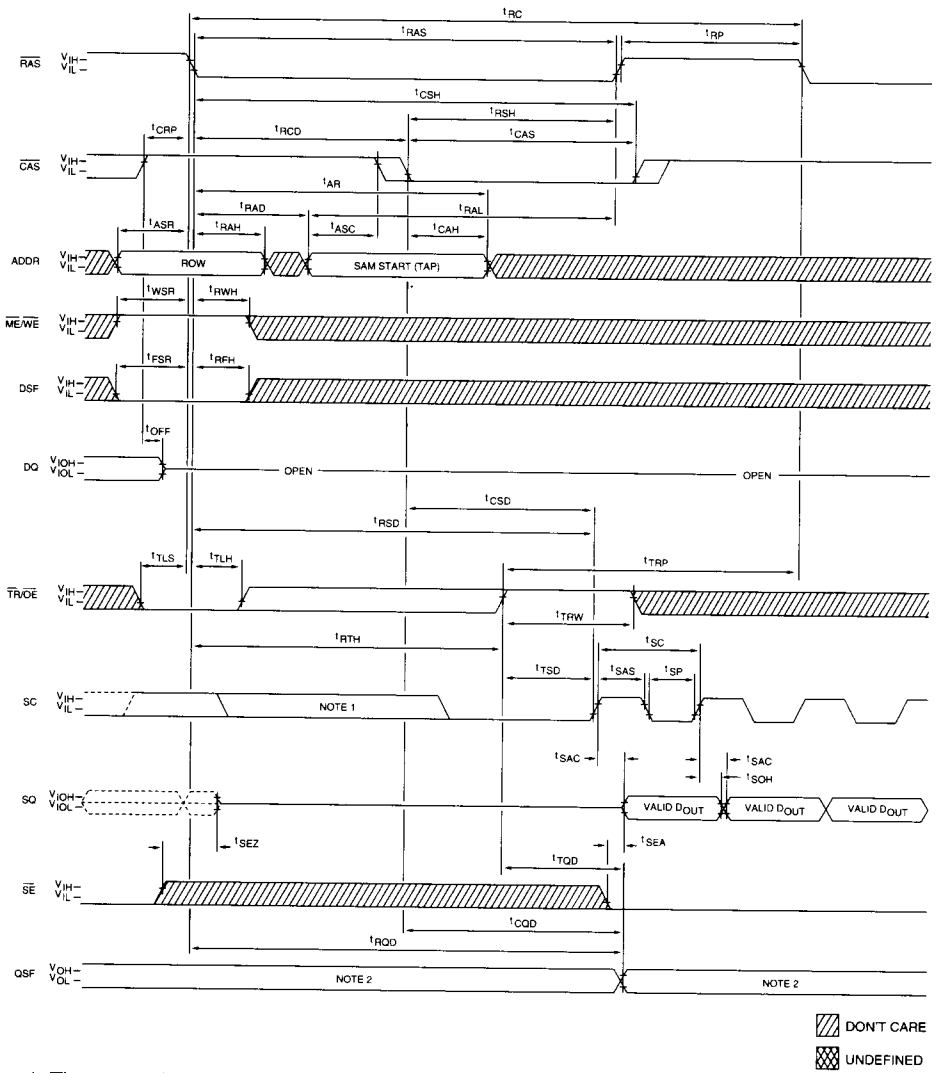
DRAM HIDDEN-REFRESH CYCLE



NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

2. The MT4V25632 operates with $\overline{ME}/\overline{WE}$ and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

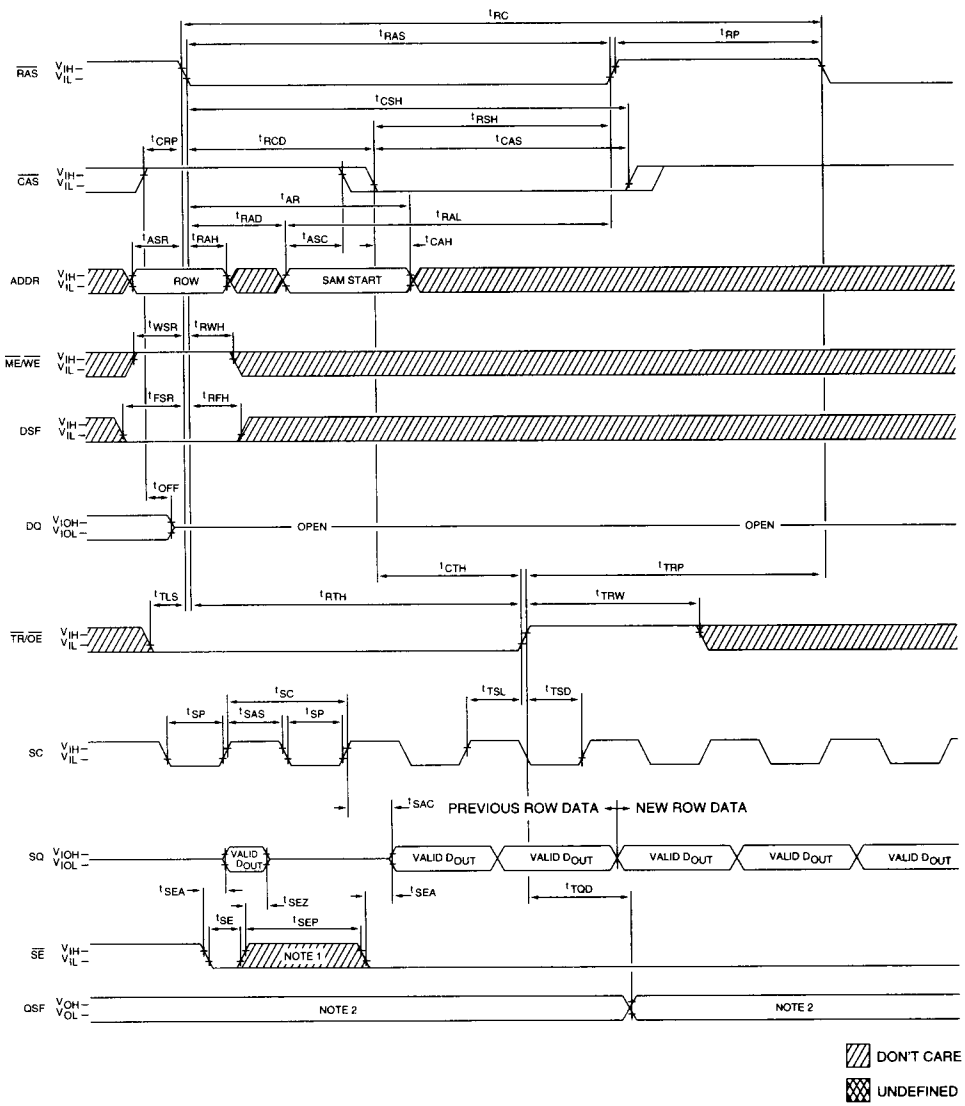
READ TRANSFER [3]
(DRAM-TO-SAM TRANSFER)
(When serial part was previously High-Z or SC idle)



NOTE:
1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. If tTLH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If tRTH is timing for the $\overline{TR}/(\overline{OE})$ rising edge, the transfer is done off of the $\overline{TR}/(\overline{OE})$ rising edge and tTSD must be met.

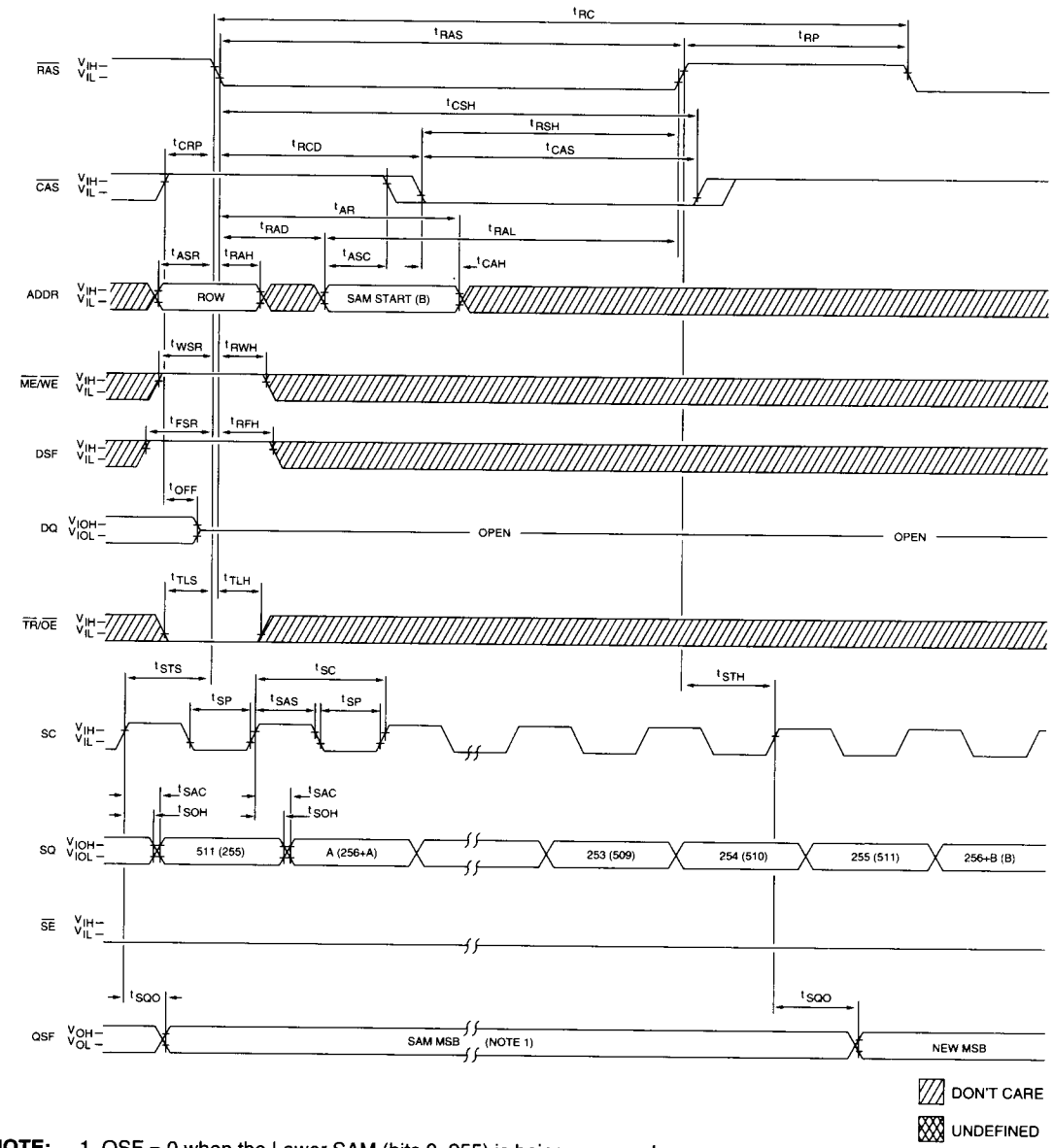
NEW VRAM MODULE

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL OUTPUT