Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9403

16-CHANNEL, 12-BIT DATA ACQUISITION SYSTEM

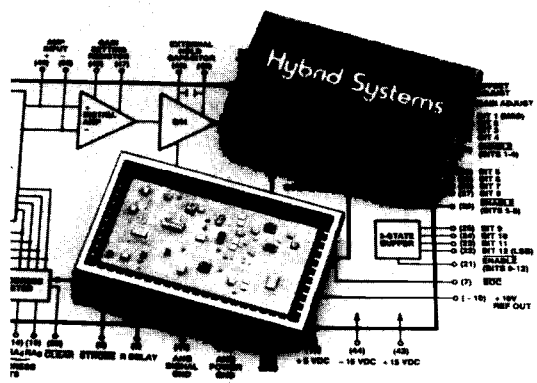
FEATURES

- Multiplexer, instrumentation amp, S/H, A/D and control logic in a 62-pin package
- Three state output buffer
- Instrumentation amp with selectable gain ranging 1 to 1000
- Single-ended (−16) and differential (−8) inputs
- 50 kHz minimum throughput

DESCRIPTION

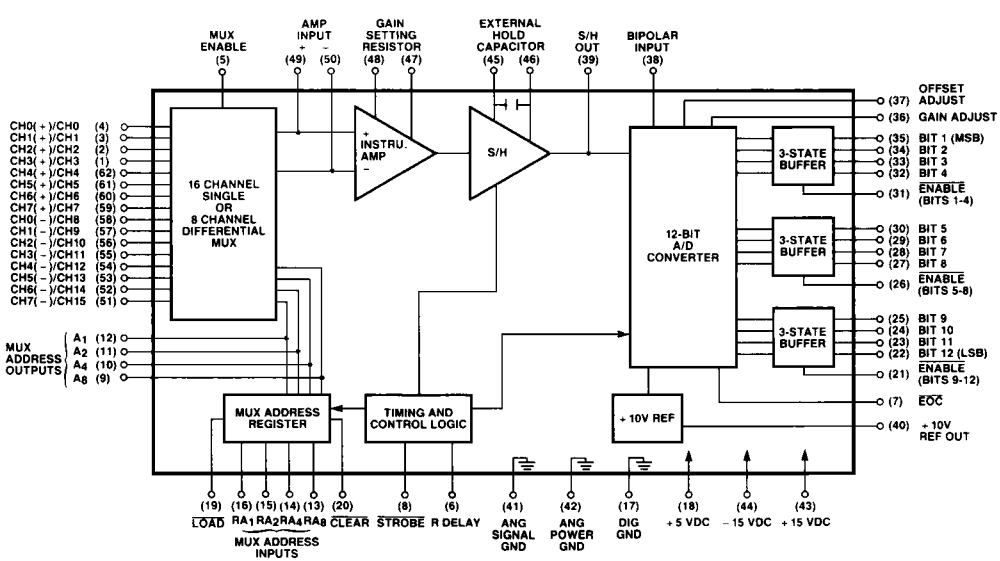
The HS9403-8 and 9403-16 provide complete 12-bit data acquisition functionality in a single, 62-pin package. The 9403 includes 8- or 16-channel multiplexing, a programmable gain instrumentation amplifier, sample-hold circuit, 10V buffered reference, 12-bit 10μsec A/D and three-state output buffers.

The 9403 is flexible enough to accept full scale input ranges from ± 10 mV to ± 10V. Three-state output buffers allow output data to be accessed in any combination of three 4-bit bytes. Expansion to 32 single-ended or 16 differential inputs can be achieved with the addition of only 2 ICs.



The 9403 is packaged in a 62-pin, hermetically-sealed, ceramic package. Temperature ranges available are 0°C to 70°C for commercial versions and −55°C to 125°C with MIL-STD-883C screening for military grades.

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

ANALOG INPUTS	HS 9403
Number of Input Channels	
HS 9403-8	8 Differential
HS 9403-16	16 Single-Ended
Input Voltage Range[1]	
Unipolar	0 to +10V
Bipolar	±10V
Common Mode Voltage Range	±11V min
CMRR	
G = 1 (1 kHz)	74 dB
G = 1000 (60 Hz)	110 dB
Input Bias Current	±50 pA typ
Bias Current Drift	Doubles every 10°C
Input Offset Current	±25 pA typ,
Offset Current Drift	Doubles every 10°C
Input Offset Voltage	±2 mV
Offset Voltage Drift	(20 + 7G)μ V/°C
Voltage Noise (RTI)[2]	
G = 1	150μ V (RMS)[3]
G = 1000	1.6μ V (RMS)[3]
Input Resistance	10^{12}
Input Capacitance	
OFF Channel	10 pF
ON Channel 9403-8	50 pF
9403-16	100 pF

DIGITAL INPUTS	
Logic Levels	
Logic "1"	+2V min,+5.5V max
Logic "0"	-0.3Vmin,+0.8V max
Logic Loading	
Logic "1"	20 μA
Logic "0"	-0.2 mA

STATIC PERFORMANCE[4]	
No Missing Codes	Guaranteed over operating temperature range
Integral Linearity Error	±¼ LSB typ, ±½ LSB max
Differential Linearity Error	±¼ LSB typ, ±½ LSB max
Unipolar Offset Error[5]	±0.025% FSR typ, ±0.1% FSR[6] max
Bipolar Zero Error[5]	±0.025% FSR typ, ±0.1% FSR[6] max
Gain Error[5]	±0.025% typ, ±0.2% max

+10V REFERENCE	
Output Voltage	+10.000V ±10 mV
Output Voltage Drift	±3 ppm/°C typ, ±8 ppm/°C max

DYNAMIC PERFORMANCE	
Throughput Rate	50KHz min
S/H Acquisition Time[7,11]	9μsec typ. 10μsec max.
A/D Conversion Time	10μsec max.
Aperture Delay	25 nsec typ.
Sample-Hold Droop	0.1μV/μsec
Feedthrough (@ 1 kHz)[8,11]	±0.01% max.
MUX Crosstalk (@ 1 kHz) [11]	-80dB min.
Strobe Command Pulse Width[11]	40 nsec min.
Setup time Digital Inputs to Strobe[11]	50 nsec min.
Hold Time Digital Inputs From Strobe[11]	50nsec max.
ENABLE	
Tri-State to Valid[11]	40 nsec max.
Valid to Tri-State[11]	30 nsec max.

DRIFT CHARACTERISTICS[10]	
Integral Linearity	±1 ppm/°C typ, ±2 ppm/°C max
Differential Linearity	±1 ppm/°C typ, ±2 ppm/°C max
Unipolar Offset	±3 ppm/°C typ, ±7 ppm/°C max
Bipolar Zero	±3 ppm/°C typ, ±10 ppm/°C max
Gain	±8 ppm/°C typ. ±20 ppm/°C max

DIGITAL OUTPUTS	
Logic Levels	
Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Coding	
Unipolar Ranges	Straight binary
Bipolar Ranges	Offset binary
Fanout	5 TTL Loads

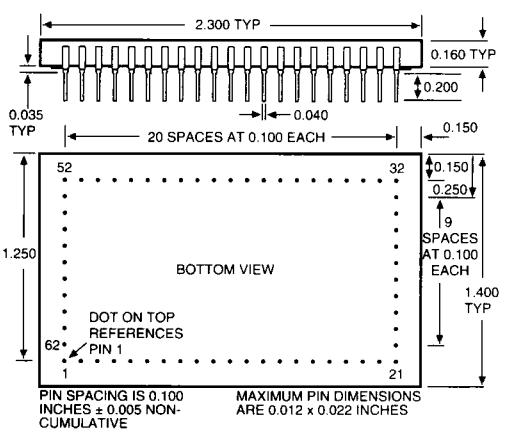
POWER SUPPLIES	
Power Supply Range	
±15V	±14.5V to ±15.5V
+5V	+4.5V to +5.5V
Current Drains	
+15V	55 mA typ, 60 mA max
-15V	60 mA typ, 68 mA max
+5V	32 mA typ, 45 mA max
Power Dissipation	1.4W typ, 2.0W max
P.S.R.R. for 3 supplies	0.005%/% max
P.S.R.R. (+10V ref)	0.01%/% max

TEMPERATURE RANGE	
Operating C-Option	0°C to +70°C
Operating B-Option	-55°C to +125°C
Storage	-65°C to +150°C

ABSOLUTE MAXIMUM RATINGS	
$+V_{CC}$	-0.5V to +18V
$-V_{CC}$	+0.5V to -18V
V_{DD}	-0.3 to +7V
Analog Input Channels	±35V
Digital Inputs	-0.3 to V_{DD} +0.3V

Notes:
1. For unity gain.
2. Referred to input.
3. Measured at output of S/H.
4. Specifications refer t0 entire system from MUX input to A/D output with instrumentation amplifier G=1.
5. Initial offset and gain errors are adjustable to zero with optional external potentiometers.
6. FSR = full scale range. Unipolar FSR = 10V, Bipolar FSR = 20V. For a 12-bit system, 1 LSB =0.024% FSR
7. Includes MUX switching and setting time, instrumentation amp unity gain settling time and S/H acquisition time. Specified for 10V step setting to 0.01% FSR
8. Measured at S/H output with S/H in hold mode.
9. Includes MUX address, MUX enable, clear and load inputs.
10. Unipolar 10V FSR is the basis for parts per million specifications.
11. Guaranteed but not tested.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN NO.	FUNCTION HS 9403-16	FUNCTION HS 9403-8
1	CH3 IN	CH3(+)IN
2	CH2 IN	CH2(+)IN
3	CH1 IN	CH1(+)IN
4	CH0 IN	CH0(+)IN
5	MUX ENABLE	
6	R DELAY	
7	$\overline{EOC}$	
8	$\overline{STROBE}$	
9	A8	
10	A4	
11	A2 MUX ADDRESS OUT	
12	A1	
13	RA8	
14	RA4	
15	RA2 MUX ADDRESS IN	
16	RA1	
17	DIGITAL GROUND	
18	+5V	
19	$\overline{LOAD}$ ENABLE	
20	$\overline{CLEAR}$ ENABLE	
21	$\overline{ENABLE}$ (BITS 9-12)	
22	BIT 12 OUT (LSB)	
23	BIT 11 OUT	
24	BIT 10 OUT	
25	BIT 9 OUT	
26	$\overline{ENABLE}$ (BITS 5-8)	
27	BIT 8 OUT	
28	BIT 7 OUT	
29	BIT 6 OUT	
30	BIT 5 OUT	
31	$\overline{ENABLE}$ (BITS 1-4)	
32	BIT 4 OUT	
33	BIT 3 OUT	
34	BIT 2 OUT	
35	BIT 1 OUT (MSB)	
36	GAIN ADJ	
37	OFFSET ADJ	
38	BIPOLAR INPUT	
39	SAMPLE/HOLD OUT	
40	+10V REFERENCE OUT	
41	ANALOG SIGNAL GROUND	
42	ANALOG POWER GROUND	
43	+15V	
44	−15V	
45	EXTERNAL HOLD CAP HIGH	
46	EXTERNAL HOLD CAP LOW	
47	R GAIN LOW	
48	R GAIN HIGH	
49	INSTRU. AMP (+) INPUT	
50	INSTRU. AMP (−) INPUT	
51	CH15 IN	CH7(−)IN
52	CH14 IN	CH6(−)IN
53	CH13 IN	CH5(−)IN
54	CH12 IN	CH4(−)IN
55	CH11 IN	CH3(−)IN
56	CH10 IN	CH2(−)IN
57	CH9 IN	CH1(−)IN
58	CH8 IN	CH0(−)IN
59	CH7 IN	CH7(+)IN
60	CH6 IN	CH6(+)IN
61	CH5 IN	CH5(+)IN
62	CH4 IN	CH4(+)IN

DIGITAL PIN FUNCTIONS

FUNCTION	PIN NO.	LOGIC STATE	DESCRIPTION
MUX ENABLE	5	"0"	Disables internal MUX
		"1"	Enables internal MUX
$\overline{EOC}$	7	"0"	Signal acquisition cycle in progress
		"1"	A/D conversion in progress
		"1" to "0"	Conversion complete
$\overline{STROBE}$	8	"1" to "0"	Initiates acquisition and conversion of analog signal
MUX ADDRESS OUT	9-12		Output of MUX address register. Straight binary coding
MUX ADDRESS IN	13-16		Selects MUX for random address mode. Straight binary coding
$\overline{LOAD}$	19	"0"	Random address mode initiated on falling edge of $\overline{STROBE}$
		"1"	Sequential address mode
$\overline{CLEAR}$	20	"0"	Forces MUX address to CH0 on next falling edge of $\overline{STROBE}$ regardless of $\overline{LOAD}$ and MUX address inputs
$\overline{ENABLE}$ (BITS 9-12)	21	"0"	Enables three-state outputs bits 9-12
		"1"	Disables three-state outputs bits 9-12
$\overline{ENABLE}$ (BITS 5-8)	26	"0"	Enables three-state outputs bits 5-8
		"1"	Disables three-state outputs bits 5-8
$\overline{ENABLE}$ (BITS 1-4)	31	"0"	Enables three-state outputs outputs bits 1-4
		"1"	Disables three-state outputs bits 1-4

ANALOG PIN FUNCTIONS

FUNCTION	PIN NO.	DESCRIPTION
R DELAY	6	Connect external resistor to lengthen S/H acquisition time when instrumentation AMP is set for high gain (for normal operation, R DELAY tied to +5V).
GAIN ADJUST	36	External gain adjust (optional)
OFFSET ADJUST	37	External offset adjust (optional)
BIPOLAR INPUT	38	For unipolar operation (0 to +10V), connect to pin 39 (S/H OUT). For Bipolar operation (±10V), connect to pin 40 (+10V REF OUT)
S/H OUTPUT	39	Sample-Hold output
+10V REF OUT	40	Buffered +10V reference output
EXTERNAL HOLD CAPACITOR	45, 46	Add external polypropylene, polystyrene or teflon hold capacitor to improve S/H droop rate (optional)
R GAIN	47, 48	Optional gain selection point. R = 20k/(G − 1). Leave open for G = 1
INSTRUMENTATION AMP INPUTS	49, 50	Use when adding additional external multiplexers for expanded single-ended or differential operation (see Applications Information). Connect pin 50 to analog common for HS 9403-16

11

APPLICATIONS INFORMATION

NOTES:

1. Input channels are protected to 20V beyond power supplies.
2. To improve sample-hold droop rate, an external hold capacitor may be connected between external hold cap pins 45 and 46. Polypropylene or teflon capacitors are recommended for best results. Acquisition time must be increased accordingly.
3. $R\ GAIN\ (\Omega) = \frac{20{,}000}{(GAIN - 1)}$ ($\pm 0.1\%$ typical)
4. To increase acquisition time allotment, connect a resistor from R DELAY (pin 6) to +5V (pin 18).

$$R\ DELAY\ (\Omega) = \frac{AMP\ settling\ time}{10^{-9}} - 9K\ (see\ Table\ 1)$$

INPUT RANGE	GAIN	R GAIN (R)	AMP SETTLING TIME	R DELAY	THROUGHPUT	SYSTEM ACCURACY
±10V	1	None	9 μsec	None	55.5 kHz	0.009%
±5V	2	20.0k	9 μsec	None	55.5 kHz	0.009%
±2.5V	4	6.667k	9 μsec	None	55.5 kHz	0.009%
±1V	10	2.222k	9 μsec	None	55.5 kHz	0.009%
±200 mV	50	408.2	16 μsec	7K	40.0 kHz	0.010%
±100 mV	100	202.0	30 μsec	21K	25.6 kHz	0.011%
± 50 mV	200	100.5	60 μsec	51K	14.5 kHz	0.016%
± 20 mV	500	40.08	144 μsec	135K	6.5 kHz	0.035%
± 10 mV	1000	20.02	288 μsec	279K	3.3 kHz	0.069%

Table 1. Input Range Parameters

MUX CHANNEL ADDRESSING

The HS 9403-8 and HS 9403-16 are capable of having their input multiplexer channels either randomly or sequentially addressed.

ADDRESS MODE	MUX ENABLE	$\overline{LOAD}$	$\overline{CLEAR}$	ADDRESS INPUTS	ADDRESS OUTPUTS	$\overline{STROBE}$
Random	1	0	1	Next channel	On channel	"1" to "0"
Sequential	1	1	1	Don't care	On channel	"1" to "0"
Free-Running Sequential	1	1	1	Don't care	On channel	"1" to "0"

Table 2.

RANDOM ADDRESS

Set $\overline{LOAD}$ (pin 19) to LOGIC "0". The next falling edge of $\overline{STROBE}$ will load the MUX channel address present on pin 13 to pin 16. Address inputs must be stable 50 nsec before and after falling edge of $\overline{STROBE}$ pulse.

TRIGGERED SEQUENTIAL ADDRESS

Set $\overline{LOAD}$ (pin 19) and $\overline{CLEAR}$ (pin 20) to LOGIC "1". Applying a falling edge trigger pulse to $\overline{STROBE}$ (pin 8). This negative transition causes the contents of the address counter to increment by one followed by a sample-hold acquisition and A/D conversion. Changing digital data appearing at the address inputs will not affect the HS 9403 when it is in the sequential address mode.

FREE-RUNNING SEQUENTIAL ADDRESS

Set $\overline{LOAD}$ (pin 19) and $\overline{CLEAR}$ (pin 20) to LOGIC "1". Connect $\overline{EOC}$ (pin 7) and $\overline{STROBE}$ (pin 8) together. The falling edge of $\overline{EOC}$ will increment channel address. When the $\overline{EOC}$ goes low, the digital output data is valid for the previous channel for approximately 10 sec while the multiplexer is switching channels and the S/H is acquiring the new signal.

VALID OUTPUT

During the conversion ($\overline{EOC}$ high), the output of the A/D is changing during the successive approximation sequence. If the outputs are connected to a Data Bus, the enable inputs (pins 21, 26 and 31) must be held high to prevent invalid data from reaching the bus. If data is to be read immediately after conversion is completed, connect $\overline{EOC}$ to $\overline{ENABLE}$ (bits 1-4), $\overline{ENABLE}$ (bits 5-8) and $\overline{ENABLE}$ (bits 9-12), pins 21, 26 and 31. This will tri-state the outputs during conversion and enable them during the acquisition period.

ADDRESS INPUTS				MUX ENABLE	CHANNEL SELECTED	
A8	A4	A2	A1			
X	X	X	X	0	None	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	
0	1	1	1	1	7	HS 9403-8
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	
1	1	1	1	1	15	HS 9403-16

Table 3. MUX Channel Addressing

APPLICATIONS INFORMATION (continued)

INPUT EXPANSION

The HS 9403 can be easily expanded to 32 single-ended channels or 16 differential channels. When extending channel capacity, the multiplexer settling time must be extended through the use of R DELAY (pin 6).

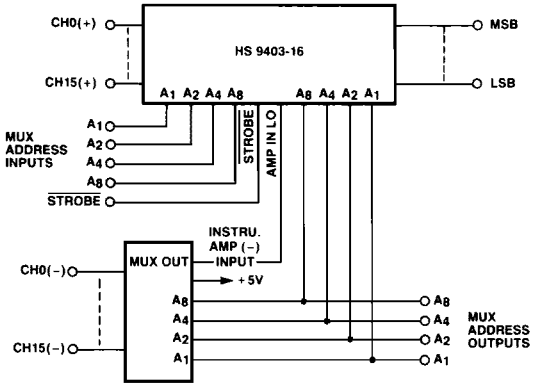


Figure 2. 16-Channel Differential Input Expansion

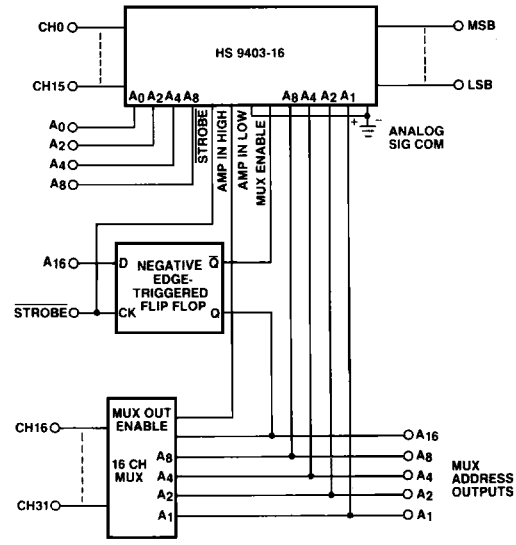


Figure 3. 32-Channel Single-Ended Input Expansion

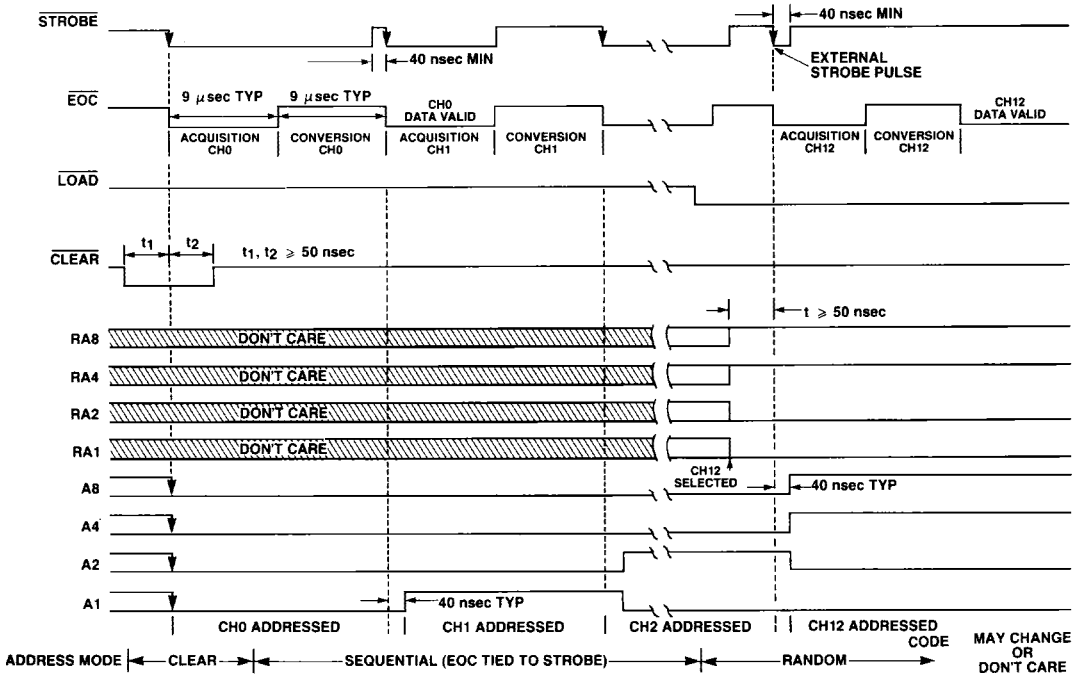
ORDERING INFORMATION

MODEL NUMBER	TEMPERATURE RANGE	DESCRIPTION
HS 9403C-8	0°C to +70°C	8 differential input, 12-bit, data acqusition system (DAS)
HS 9403C-16	0°C to +70°C	16 single-ended input, 12-bit, DAS
HS 9403B-8	-55°C to +125°C	8 differential input, 12-bit, DAS MIL-STD-883C
HS 9403B-16	-55°C to +125°C	16 single-ended input, 12-bit, DAS MIL-STD-883C
HS 9403C-16 FP	0°C to +70°C	16 single-ended input in flat pack
HS 9403B-16 FP	-55°C to +125°C	16 single-ended input, in flat pack, MIL-STD-883C

Specifications subject to change without notice

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below – volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

TIMING DIAGRAM



OFFSET AND GAIN ADJUST CONNECTIONS

The HS 9403 offset and gain adjustments may be made by connecting two 20K trim potentiometers as shown below:

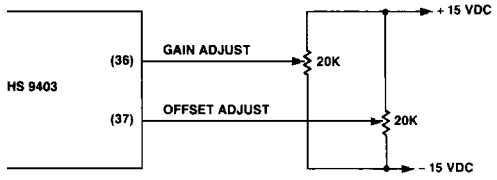


Figure 1. Offset and Gain Adjust Connections

Offset Adjustment — Connect the OFFSET potentiometer as shown above and apply an analog input voltage equivalent to + ½ LSB if operating in a unipolar mode or − FS + ½ LSB if operating in a bipolar mode. While performing repeated conversions, adjust the offset potentiometer down until all output bits are "0". Then adjust up until the LSB just turns to a "1".

Gain Adjust — Connect the gain potentiometer as shown and apply an analog input voltage equivalent to + FS − 1½ LSB. While performing repeated conversions, adjust the gain potentiometer up until all the output bits are "1". Then adjust down until the LSB just turns to "0".

NOTE:
Since the offset adjustments effects the gain of the system, offset voltage must be adjusted first.

DIGITAL OUTPUT CODING

	UNIPOLAR 0 to + 10V	0 to + 5V	STRAIGHT BINARY		
+ FS − 1 LSB	+ 9.9976	+ 4.9988	1111	1111	1111
+ ½ FS	+ 5.0000	+ 2.5000	1000	0000	0000
+ 1 LSB	+ 0.0024	+ 0.0012	0000	0000	0001
ZERO	0.0000	0.0000	0000	0000	0000
	BIPOLAR ± 10V	**± 5V**	**OFFSET BINARY**		
+ FS − 1 LSB	+ 9.9951	+ 4.9976	1111	1111	1111
+ ½ FS	+ 5.0000	+ 2.5000	1100	0000	0000
+ 1 LSB	+ 0.0049	+ 0.0024	1000	0000	0001
ZERO	0.0000	0.0000	1000	0000	0000
− FS + 1 LSB	− 9.9951	− 4.9976	0000	0000	0001
− FS	− 10.000	− 5.0000	0000	0000	0000

GROUNDING CONSIDERATIONS

The HS 9403 brings out separate pins for analog power ground, analog signal grounds, and digital ground. All three should be connected together as close to the unit as possible and connected to system analog ground. If the ground pins cannot be connected directly at the package, wide low resistive ground lines should be used and a non-polarized capacitor (0.1 to 1 μF) should be connected between analog and digital ground directly at the package.

Internal 0.01 μF ceramic decoupling capacitors are used in the device. However, it is advisable to add a 1 μF or 10 μF tantalum capacitor to each power supply pin from the central ground point to minimize power supply noise problems.