CAT-ADP12B160M-T65G
CAT-ADP12B123M-T65G
CAT-ADP12B80M-T65G

12-Bit, 160Msps, Pipeline ADC IP Core in 65nm

General Description

The CAT-ADP12B160M-T65G is an ultra-low-power, high-performance analog-to-digital converter (ADC) IP core that operates up to 160Msps. It is ideally suited for applications that require low power and high precision.

The ADC IP core employs patented and proven low-power techniques based on zero-crossing-based switched-capacitor circuitry that allows for ultra-low power operation, while enabling implementation in a smaller silicon footprint.

The CAT-ADP12B160M-T65G operates from a standard core supply voltage and is manufactured in a state-of-the-art CMOS process. The CAT-ADP12B160M-T65G has very low noise and excellent spurious-free dynamic range that makes it ideal for multicarrier systems.

The ADC is optimized for ease of use and integration in complex SoCs and power consumption scales significantly with sampling rate.

This ADC can be used in combination with other IP blocks as part of a complete analog front-end (AFE).

Applications

- LTE/Multimode Cellular
- Wireless LAN
- Wireline Communication
- Tuners/Demodulators

Silicon Proven

***Ordering Information* appears at end of product brief.**

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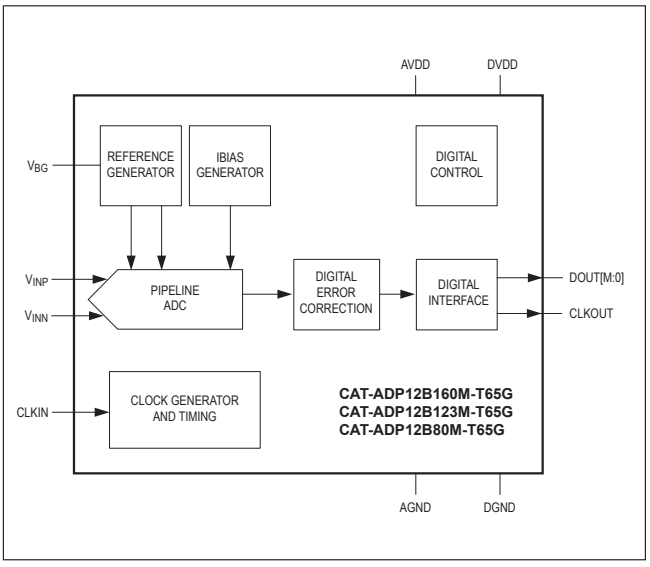
Benefits and Features

- 12-Bit ADC with Sampling Rate Up to 160Msps
- Ultra-Low-Power Operation with Revolutionary Zero-Crossing-Based Pipeline Operation (PUMA™)
- Power Scalability with Sample Rate
- Available in Dual Core (IQ) or Array Configuration
- Guaranteed Monotonicity with No Missing Codes
- Built-In Low Power and Sleep Modes
- Operates Off Core Supply Voltage
- Small Silicon Footprint (Disclosed Under NDA)
- Small Pin Count and Minimal Off-Chip Components Required

Functional Diagram



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Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{AVDD}	Relative to AGND	0.95	1.0	1.1	V
Digital Supply Voltage	V_{DVDD}	Relative to DGND	0.95	1.0	1.1	V
Junction Temperature Range	T_J		-40		+125	ºC
Analog Input Common-Mode Voltage	V_{CM}			$V_{AVDD}/2$		V
Differential Analog Input Voltage	V_{INP} - V_{INN}		-0.7		+0.7	V
DIGITAL LOGIC LEVELS						
Input Voltage High	V_{IH}		0.9 x V_{DVDD}			V
Input Voltage Low	V_{IL}				0.1 x V_{DVDD}	V
Output Voltage High	V_{OH}		V_{DVDD} - 10mV			V
Output Voltage Low	V_{OL}				V_{DGND} + 10mV	V

Electrical Characteristics

(Over recommended operating junction temperature range, V_{AVDD} = 1.0V, f_S = 160Msps, A_{IN} = -1dBFS, V_{CM} = $V_{AVDD}/2$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (Note 1)						
V_{INP}/V_{INN} Input Resistance and Capacitance		Resistance at 160Msps		20		kΩ
		Fixed capacitance		0.5		pF
		Switching capacitance		1.5		pF
No Missing Codes				Guaranteed		
Monotonicity				Guaranteed		
Differential Nonlinearity	DNL			±0.5	±1	LSB
Integral Nonlinearity	INL			±2.0		LSB
AC CHARACTERISTICS (Note 2)						
Effective Number of Bits	ENOB	f_{IN} = 10MHz, DC to 10MHz		10.3		Bits
		f_{IN} = 10MHz, DC to 160MHz		9.8		
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz, DC to 10MHz		65		dB
		f_{IN} = 10MHz, DC to 160MHz		62		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz		> 65		dB
Total Harmonic Distortion	THD	f_{IN} = 10MHz		≤ -65		dB
Clock Frequency					160	Msps
Clock Duty Cycle			48		52	%

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Electrical Characteristics (continued)

(Over recommended operating junction temperature range, V_{AVDD} = 1.0V, f_S = 160Msps, A_{IN} = -1dBFS, V_{CM} = V_{AVDD}/2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DISSIPATION (per ADC)						
I_{AVDD}		f_S = 80Msps		Disclosed under NDA		mA
		f_S = 123Msps		Disclosed under NDA		mA
		f_S = 160Msps		Disclosed under NDA		mA
		Sleep mode (T_J = +25ºC)		Disclosed under NDA		µA
I_{DVDD}		f_S = 80Msps		Disclosed under NDA		mA
		f_S = 123Msps		Disclosed under NDA		mA
		f_S = 160Msps		Disclosed under NDA		mA
		Sleep mode (T_J = +25ºC)		Disclosed under NDA		µA

Note 1: Monotonicity, INL, and DNL are measured through at speed histogram testing.
Note 2: Measured through fast Fourier transform testing.

Deliverables

- Fully Characterized Hard GDS (gds2)
- Simulation Netlist (to Enable SoC Simulations)
- Abstract View at Layout Level (for Top Level Connectivity)
- Behavioral Models (on Request)
- Data Sheets
- Integration Application Notes
- Integration Support
- Silicon Proven and Ready to Order

Support

Maxim Integrated provides active on-site and off-site support for integrating its IP core into the customer's system on a chip (SoC). Initial support is included in the licensing structure; additional support beyond the IP transaction is also available. For more information, contact **aipsinfo@maximintegrated.com**.

Ordering Information

PART	SAMPLE RATE (Msps)	PROCESS* (nm)
CAT-ADP12B160M-T65G	160	TSMC 65G
CAT-ADP12B123M-T65G	123	TSMC 65G
CAT-ADP12B80M-T65G	80	TSMC 65G

**Multiple foundries available.*