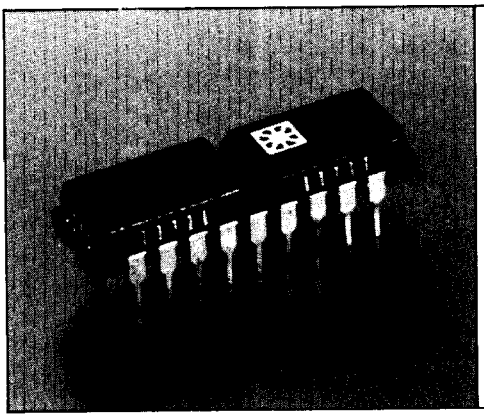


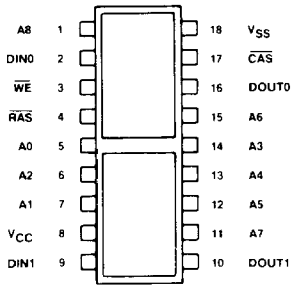
EDH42256-12/15

256K x 2 DRAM

PRELIMINARY

The EDH42256 is intended for use in any application where large quantities of memory are required and/or board space is of prime concern. General uses include computer memories, consumer and automotive electronics. Sample applications include stand alone systems for word processing, inventory control, color graphics or point of sales terminals.

PINOUTS



FEATURES

262,144 x 2 bit
Dynamic Random Access Memory

- 120 ns access time; 230ns cycle (EDH42256-12)
- 150 ns access time; 260ns cycle (EDH42256-15)
- Max power dissipation: 550mW active; 33mW standby
- Separate DIN/DOUT lines with common $\overline{RAS}$ and $\overline{CAS}$ control

18 Pin Dual In-Line Package (DIP)

- Increases density 2:1 over DIPs
- Utilizes two industry standard 256K RAMs in leadless chip carriers
- Pin compatible with 64K and 256K monolithics, as well as EDH4264

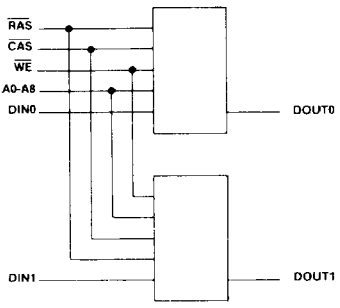
Single +5 volts (±10%) supply operation

- 256 refresh cycle
- All inputs TTL compatible

Available with MIL-STD 883 level B equivalent processing

PIN NAMES

A0-A8	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WE}$	READ/WRITE INPUT
DIN0-DIN1	DATA INPUT
DOUT0-DOUT1	DATA OUTPUT
V_{CC}	POWER (+5V)
V_{SS}	GROUND



ABSOLUTE MAXIMUM RATINGS* (see note 1)

Voltage on V_{CC} supply with respect to V_{SS} ..... -1.0V to +7.0V
Power dissipation ..... 2 Watts
Short circuit output current ..... 50 mA
Operating temperature range ..... 0°C to +70°C
Storage temperature range ..... -55°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS OVER OPERATING TEMPERATURE RANGE

(see note 1)

PARAMETER	SYM	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	Volts Volts
High Level Input Voltage	V_{IH}	2.4		V_{CC}+1	Volts
Low Level Input Voltage	V_{IL}	-1.0		0.8	Volts

DC ELECTRICAL CHARACTERISTICS OVER ALL RECOMMENDED OPERATING CONDITIONS

(see note 2)

PARAMETER	SYM	MIN	MAX	UNITS
Average Operating Current (Min. cycle time)	I_{CC1}		100	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	I_{CC2}		6	mA
$\overline{RAS}$-only Refresh Current ($\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, Min. cycle time)	I_{CC3}		80	mA
Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling, Min. cycle time)	I_{CC4}		40	mA
$\overline{CAS}$—only Refresh Current ($\overline{CAS}$ before $\overline{RAS}$, Min. cycle time)	I_{CC5}		90	mA
Input Leakage Current (0V < V_{IN} < V_{CC}, V_{CC} = 5.5V, all other pins = 0V)	I_{IL}	-10	10	μA
Output Leakage Current (D_{OUT} = High Z, 0V < V_O < 5.5V)	I_{OL}	-10	10	μA
Output Levels High Output (I_{OH}=-5mA) Low Output (I_{OL}=4.2mA)	 V_{OH} V_{OL}	 2.4	 0.4	 Volts Volts

CAPACITANCE

(see note 3)

PARAMETER	SYM	TYP	MAX	UNITS
Input Capacitance, (A0-A7)	C_{IA}	18	22	pF
Input Capacitance, (D_{IN})	C_{ID}	5	6	pF
Input Capacitance, (Clocks)	C_{IC}	20	24	pF
Output Capacitance, (DOUT)	C_{OD}	6	8	pF

DYNAMIC CHARACTERISTICS OVER ALL RECOMMENDED OPERATING CONDITIONS

(see notes 4, 5, 6)

PARAMETER	SYM	EDH42256-12		EDH42256-15		UNIT	NOTES
		MIN	MAX	MIN	MAX		
Random Read/Write Cycle Time	tRC	230		260		ns	
Read-Write Cycle Time	tRW	230		260		ns	
Page Mode Cycle Time	tPC	120		150		ns	
Access Time from $\overline{RAS}$	tRAC		120		150	ns	7,8
Access Time from $\overline{CAS}$	tCAC		60		75	ns	7,9
Output Buffer Turn Off Delay	tOFF		25		30	ns	
Transition Time	tT	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	100		100		ns	
$\overline{RAS}$ Pulse Width	tRAS	120	100K	150	100K	ns	
$\overline{RAS}$ Hold Time	tRSH	60		75		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	22	60	25	75	ns	8,10
$\overline{CAS}$ Precharge (Page Mode)	tCP	50		65		ns	
$\overline{CAS}$ Precharge Time (Non Page Mode)	tCPN	25		30		ns	
$\overline{CAS}$ Pulse Width	tCAS	60	100K	75	100K	ns	
$\overline{CAS}$ Hold Time	tCSH	120		150		ns	
Row Address Set Up Time	tASR	0		0		ns	
Row Address Hold Time	tRAH	12		15		ns	
Column Address Set Up Time	tASC	0		0		ns	
Column Address Hold Time	tCAH	20		25		ns	
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	tCRS	20		20		ns	
Read Command Set Up Time	tRCS	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0		0		ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	20		20		ns	13
Write Command Set Up Time	tWCS	0		0		ns	11
Write Command Hold Time	tWCH	20		25		ns	
Write Command Pulse Width	tWP	20		25		ns	
Write Command to $\overline{RAS}$ Lead Time	tRWL	50		60		ns	
Write Command to $\overline{CAS}$ Lead Time	tCWL	50		60		ns	
Data In Set Up Time	tDS	0		0		ns	
Data In Hold Time	tDH	20		25		ns	

DYNAMIC CHARACTERISTICS OVER ALL RECOMMENDED OPERATING CONDITIONS

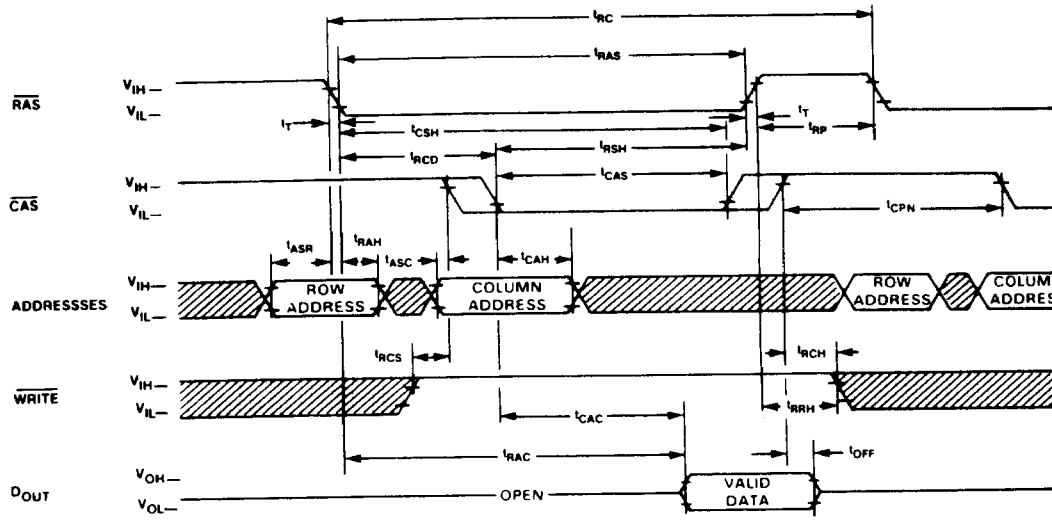
(see notes 4, 5, 6)

PARAMETER	SYM	EDH42256-12		EDH42256-15		UNIT	NOTES
		MIN	MAX	MIN	MAX		
$\overline{CAS}$ to $\overline{WRITE}$ Delay	tCWD	20		25		ns	11
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	tCPR	25		30		ns	
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$	tFCS	25		30		ns	
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$	tFCH	25		30		ns	
Page Mode Read-Write Cycle Time	tPRWC	120		150		ns	
Refresh Counter Test RAS Pulse Width	tTRAS	265	10,000	320	10,000	ns	12
Refresh Counter Test Cycle Time	tRTC	375		430		ns	12
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	tRPC	20		20		ns	
Refresh Counter Test $\overline{CAS}$ Precharge Time	tCPT	60		70		ns	12
Refresh Period	tREF		4		4	ms	

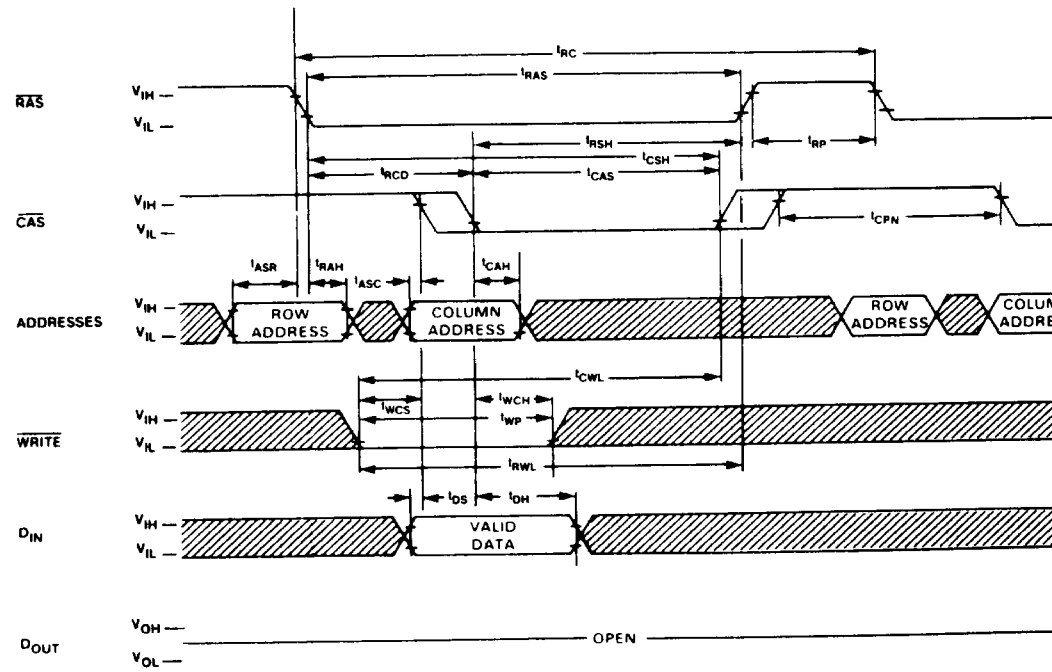
NOTES:

1. All voltage referenced to V_{SS}.
2. I_{CC} is dependent on cycle rates and output loading. Specified values are obtained with outputs open.
3. High capacitance is due to two (2) parallel loads. This must be taken into consideration during system design.
4. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
5. AC Characteristics assume tT=5ns.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
7. Measured with a load equivalent to 2 TTL loads and 100 pF.
8. Assumes that tRCD≤ tRCD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
9. Assumes that tRCD ≥tRCD (max).
10. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
11. tWCS and tCWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If tCWD ≥tCWD (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
12. Test mode write cycle only.
13. Either tRCH or tRRH must be satisfied for a read cycle.

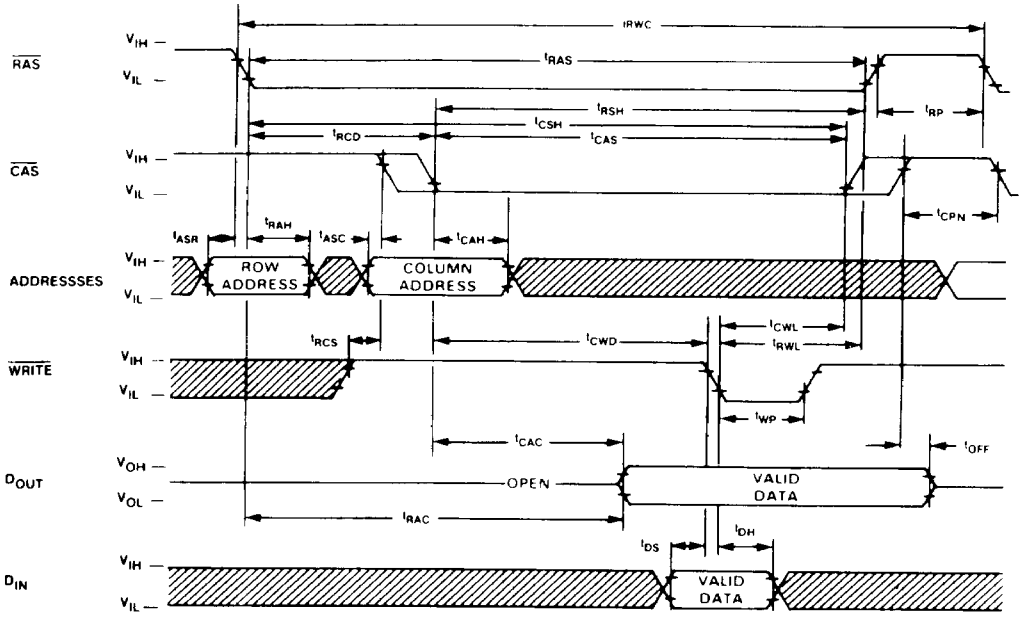
READ CYCLE



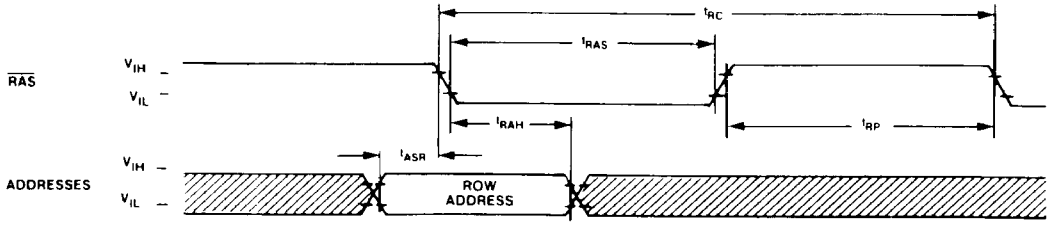
WRITE CYCLE (EARLY WRITE)



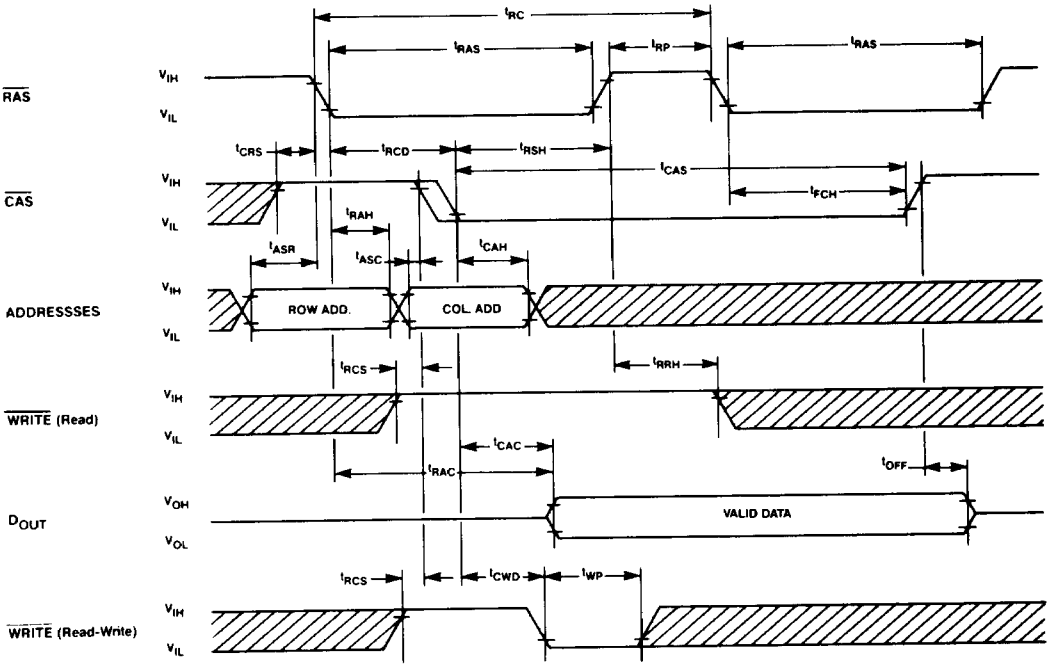
READ-WRITE/READ-WRITE CYCLE



"RAS-ONLY" REFRESH CYCLE

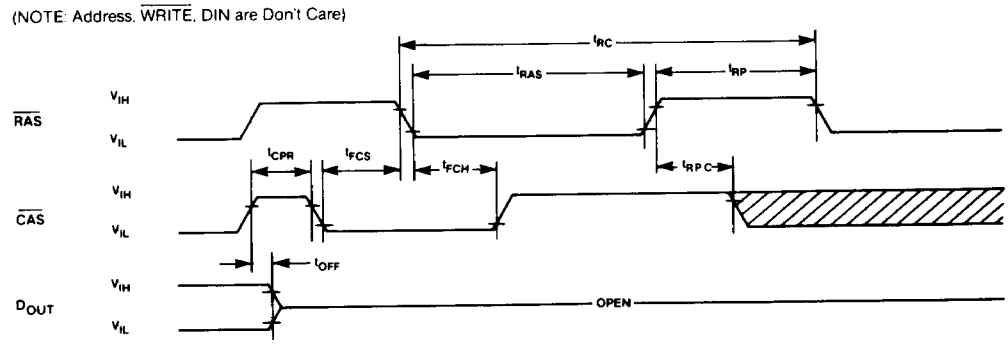


HIDDEN REFRESH CYCLE

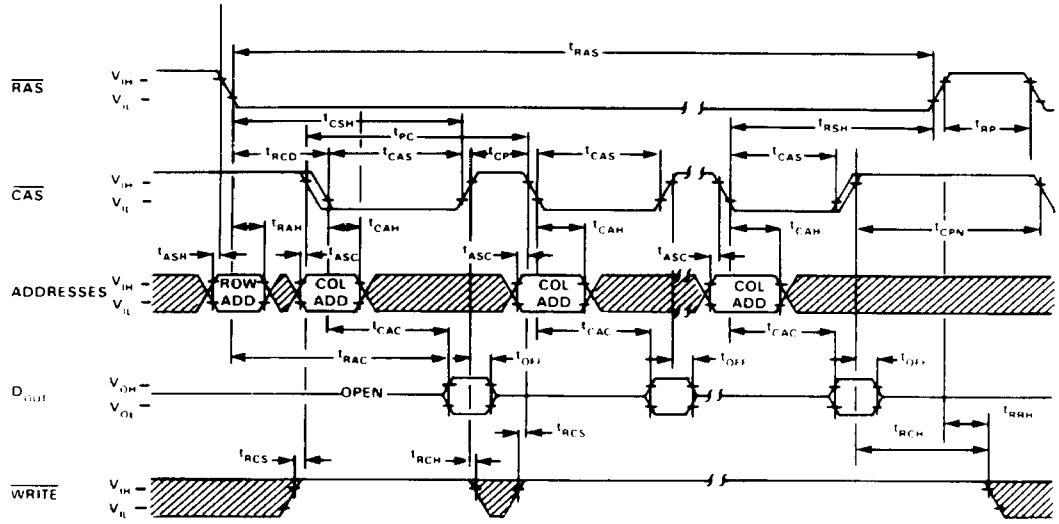


"CAS-BEFORE-RAS" REFRESH CYCLE

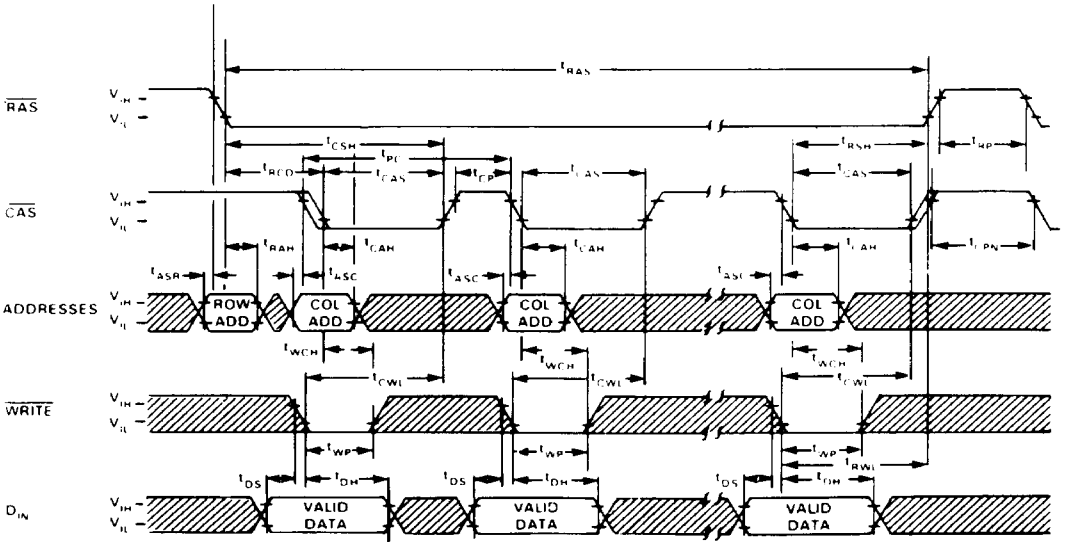
(NOTE: Address, WRITE, DIN are Don't Care)



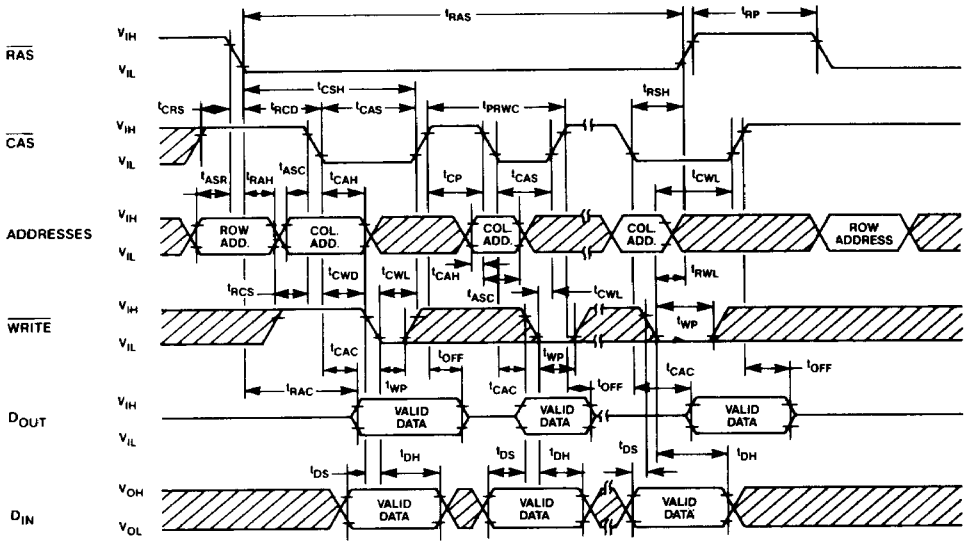
PAGE MODE READ CYCLE



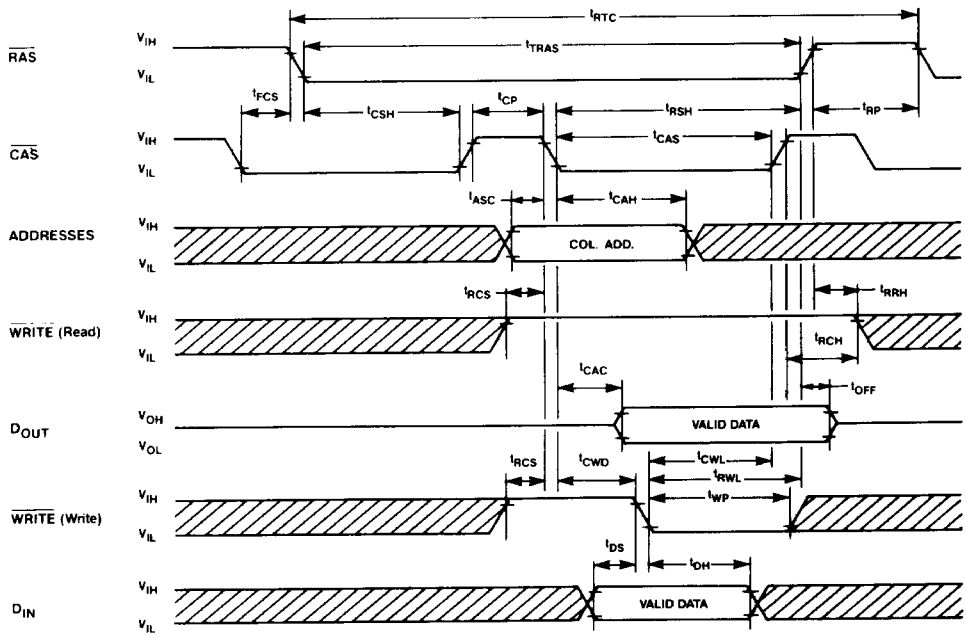
PAGE MODE WRITE CYCLE



PAGE MODE READ-WRITE CYCLE



"CAS-BEFORE-RAS" REFRESH COUNTER TEST CYCLE



OPERATION

Operation of the EDH42256 is identical to the operation of industry standard 256K dynamic RAMs in DIP packages. The unique packaging method provides the engineer with industry standard RAMs in a one bit wide configuration at a 2:1 density increase.

The high density memory consists of two industry standard 256K x 1 dynamic RAMs in leadless chip carriers mounted on a ceramic dual in-line package (DIP). The data inputs and outputs are separate with common $\overline{RAS}$ and $\overline{CAS}$.

The EDH42256 memory offers system oriented features, such as: single supply operation, ±10% tolerance on power supply, direct interfacing capability with high performance logic families, such as Shottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on chip address and data registers and two chip select methods. The EDH42256 also incorporates the following standard operating modes: read, write, read-write, early write, page-mode operation, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and hidden refresh. Proper control of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$ allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

SIMPLIFIED TIMING REQUIREMENT

The EDH42256 has improved circuitry that eases timing requirements for high speed access operations. The EDH42256 can operate under the condition of $t_{RCD}(max) = t_{CAC}$, thus providing optimal timing for address multiplexing. In addition, the EDH42256 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The EDH42256 provides higher throughput in inter-leaved memory system applications. The timing requirements that are referenced to $\overline{RAS}$ are non-restrictive and are deleted from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, DIN and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

FAST READ-WRITE CYCLE

The EDH42256 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes "low". When $\overline{WE}$ is "low" during a $\overline{CAS}$ transition to "low" the EDH42256 goes into the early write mode in which the output floats and common I/O bus can be used on the system level. When $\overline{WE}$ goes "low" after t_{CWD} following a $\overline{CAS}$ transition to "low", the EDH42256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from DIN is written into the cell selected. Therefore, a very fast read-write cycle ($t_{RWC} = t_{RC}$) is possible with EDH42256.

ADDRESS INPUTS

User access of two memory locations from 524,288 available cells is accomplished by multiplexing 18 address bits onto 9 address inputs and by proper control of the $\overline{RAS}$ and $\overline{CAS}$ clocks. Nine row-address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the failing edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

WRITE ENABLE

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

DATA INPUT

Data is written into the EDH42256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the data-in register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, DIN is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus DIN is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in the high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD}(max)$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

PAGE MODE

Page mode operation permits strobing the row address into the EDH42256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-ONLY REFRESH

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the row-addresses (A_0~A_7) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses (A_0~A_7) with RAS will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the EDH42256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

HIDDEN REFRESH

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the EDH42256, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A ROW ADDRESS

Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A COLUMN ADDRESS

All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

SUGGESTED $\overline{CAS}$-BEFORE-$\overline{RAS}$ COUNTER TEST PROCEDURE

The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1). Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2). Write a test pattern of "low"s into memory cells at a single column address and 256 row address.

(3). Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.

(4). Read the "high"s written at the last operation (Step 3).

(5). Complement the test pattern and repeat steps (2), (3) and (4).