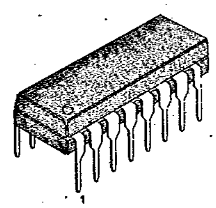
TV HORIZONTAL PROCESSOR

The KA2137 is a horizontal processor circuit for B/W. and color television receiver. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package.

16 DIP



FEATURES

- Noise gated horizontal sync separator.
- Noise gated vertical sync separator.
- Horizontal oscillator with frequency range limiter.
- Phase comparator between sync pulses and oscillator pulses (PLL).
- Phase comparator between flyback pulses and oscillator pulses (PLL).
- Loop gain and time constant switching (VCR).
- Composite blanking and key pulse generator.
- Protection circuits.
- Output stages with high current capability.

BLOCK DIAGRAM

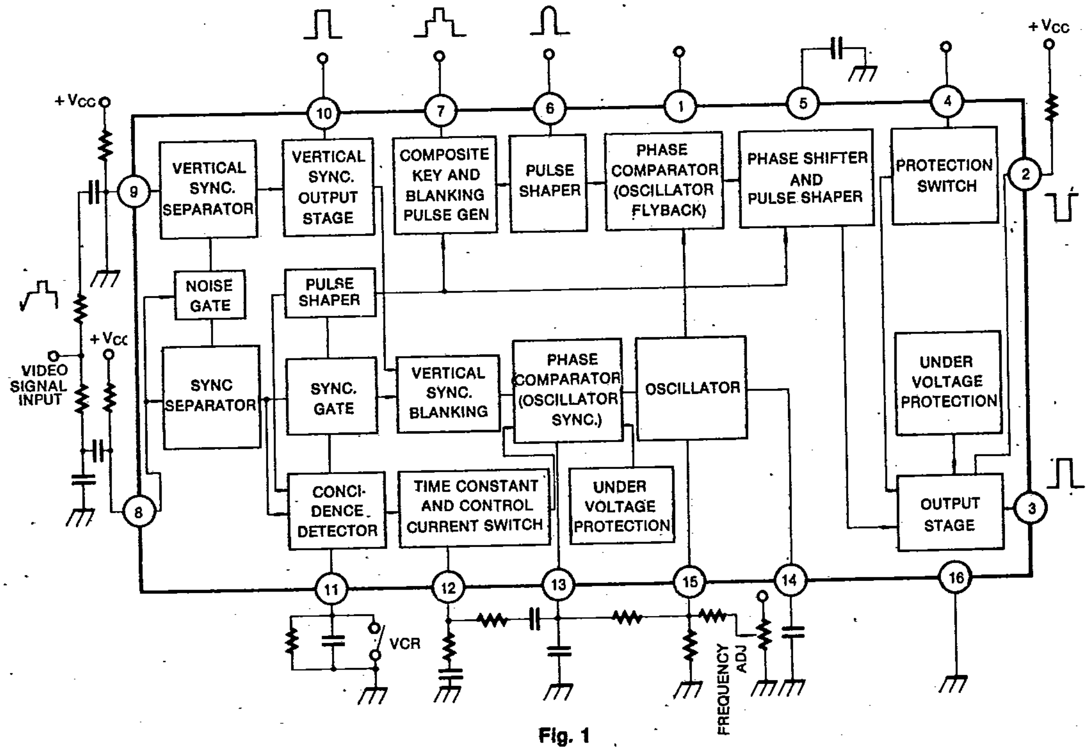


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage at Pin 1	V_{CC}	15	V
Voltage at Pin 2	V_2	18	V
Voltage at Pin 4	V_4	V_{CC}	
Voltage at Pin 8	V_8	{ V_{CC} / −6	V
Voltage at Pin 9	V_9	{ +6 / −6	V
Voltage at Pin 11	V_{11}	V_{CC}	
Pin 2 Peak Current	I_2	1	A
Pin 3 Peak Current	I_3	0.5	A
Pin 6 Current	I_6	30	mA
Pin 7 Current	I_7	20	mA
Pin 10 Current	I_{10}	30	mA
Total Power Dissipation at Ta≤70°C	P_D	1	W
Storage and Junction Temperature	T_{stg}, T_j	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, V_{CC} = 12V, T_{amb} = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
COINCIDENCE DETECTOR						
Output Voltage	V_{11}	with coincidence		6.8		V
		without coincidence			4	V
Peak Output Current	I_{11}			0.5		mA
VCR SWITCH						
Input Voltage	V_{11}		0 to 4 or 8.5 to 12			V
Output Current	$-I_{11}$		35			μA
Output Current	I_{11}		0.4			mA
TIME CONSTANT SWITCH						
Output Voltage	V_{12}			3		V
Output Resistance	R_{12}	$4.5V < V_{11} < 8V$		100		Ω
		$V_{11} > 8.5V$ or $V_{11} < 4V$		40		KΩ
OSCILLATOR						
Low Level Threshold Voltage	V_{14}			5.4		V
High Level Threshold Voltage	V_{14}			8.2		V
Charge Current	I_{14}			0.6		mA
Discharge Current	I_{14}			0.3		mA
Current Source Supply Voltage	V_{15}			3		V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Source Supply Current	I_{15}			0.3		mA
Free Running Frequency	f_o			15625		Hz
Adjustment Range	$\frac{\Delta f_o}{f_o}$			±10		%
Frequency Control Sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$			52		$\frac{Hz}{\mu A}$
Frequency Change when V_{CC} Drops to 4V	Δf_o				±10	%

FLYBACK PULSE

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Threshold Voltage of Blanking Generator	V_6			1.5		V
Input Threshold Voltage of Phase Comparator	V_6			7.6		V
Input Switching Current	I_6	$V_6 \geq 1.7V$		0.23		mA

OUTPUT PULSE

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Peak to Peak Output Voltage	V_3	$I_3 = 150mApp$		10		V
Output Current	I_3	$V_3 = 5V$		500		mA
Output Resistance	R_3	at leading edge of output pulse		3		Ω
		at trailing edge of output pulse		20		Ω
Output Pulse Duration	t_p		20	22	26	μs

COMPOSITE BLANKING AND KEY PULSE

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Key Pulse Output Peak Voltage	V_{7K}		9	11		V
Blanking Pulse Output Voltage	V_{7B}		4.2	4.5	4.8	V
Output Resistance	R_7			100		Ω
Phase Relation Between Trailing Edge of Key Pulse and Middle of Sync Input Pulse	t_{SK}			2.7		μs
Key Pulse Duration	t_K		3.5	3.8		μs
Delay Between Flyback Pulse and Blanking Pulse	t_{fb}	$V_6 = 1.7V$			0.2	μs

INTERNAL GATING PULSE

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Gating Pulse Duration	t_g			7.5		μs
Phase Relation Between Middle of Sync Pulse and Leading Edge of Gating Pulse	t			3.75		μs

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR-FLYBACK PULSE PHASE COMPARATOR						
Control Voltage Range	V_5		9.4 to 8.2			V
Peak Control Current	I_5				±0.5	mA
Input Current (blocked phase detector)	I_5				5	μA
Permissible Delay Between Output Pulse Leading Edge and Flyback Pulse Leading Edge	t_d			t_p-t_f		μs
Static Control	$\frac{\Delta t}{\Delta t_d}$				0.2	%
SYNC PULSE-OSCILLATOR PHASE COMPARATOR						
Control Voltage Range	V_{13}		4.6 to 1.4			V
Control Peak Current	I_{13}			±2		mA
Phase Lock Loop Gain	$\frac{\Delta f}{\Delta t}$			2		$\frac{KHz}{\mu s}$
Catching and Holding Range	f			±700		Hz
OVERALL PHASE RELATIONSHIP						
Phase Relation Between Middle of Flyback Pulse and Middle of Sync Pulse	t_o			2.6		μs
Adjustment Sensitivity	$\frac{\Delta V_5}{\Delta t_o}$			65		$\frac{mV}{\mu s}$
Adjustment Sensitivity	$\frac{\Delta I_5}{\Delta t_c}$			10		$\frac{\mu A}{\mu s}$
PROTECTION CIRCUIT						
Input Voltage for Switching Off the Output Pulses	V_4	Output Pulses OFF			0.5	V
		Output Pulse ON	1			
Input Resistance	R_4			200		KΩ
Input Current	I_4		5			μA
Supply Voltage	V_{CC}		10	12	13.2	V
Supply Current	I_{CC}	$I_3=0$		40	52	mA
Supply Voltage at which the Output Pulses (at pin 2 and 3) are Switched Off	V_{CC}				4	V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
HORIZONTAL SYNC. SEPARATOR AND NOISE GATE						
Peak to Peak Input Signal	V_i		1	3	6	V
Input Switching Voltage	V_8	$I_8 = 80\mu A$		1.5		V
Input Switching Current	I_8	$V_8 = 1.4V$		10		μA
Input Blocking Current for Noise Suppression	I_8			0.9		mA
Input Switching Voltage for Noise Suppression	V_8			2.1		V
Leakage Current	I_8	$V_8 = -5V$			1	μA
VERTICAL SYNC. SEPARATOR						
Peak to Peak Input Signal	V_i		1	3	6	V
Input Switching Voltage	V_9	$I_9 = 80\mu A$		1.5		V
Input Switching Current	I_9	$V_9 = 1.4V$		5		μA
Leakage Current	I_9	$V_9 = -5V$			1	μA
Vertical Sync. Pulse Output Voltage	V_{10}	No load at pin 10	11			V
Output Resistance	R_{10}			10		KΩ
Delay Between Leading Edge of Input and Output Signals	t_{LV}			17		μs
Delay Between Trailing Edge of Input and Output Signals	t_{TV}			50		μs
Vertical Sync. Pulse Duration	t_V			190		μs

TEST CIRCUIT

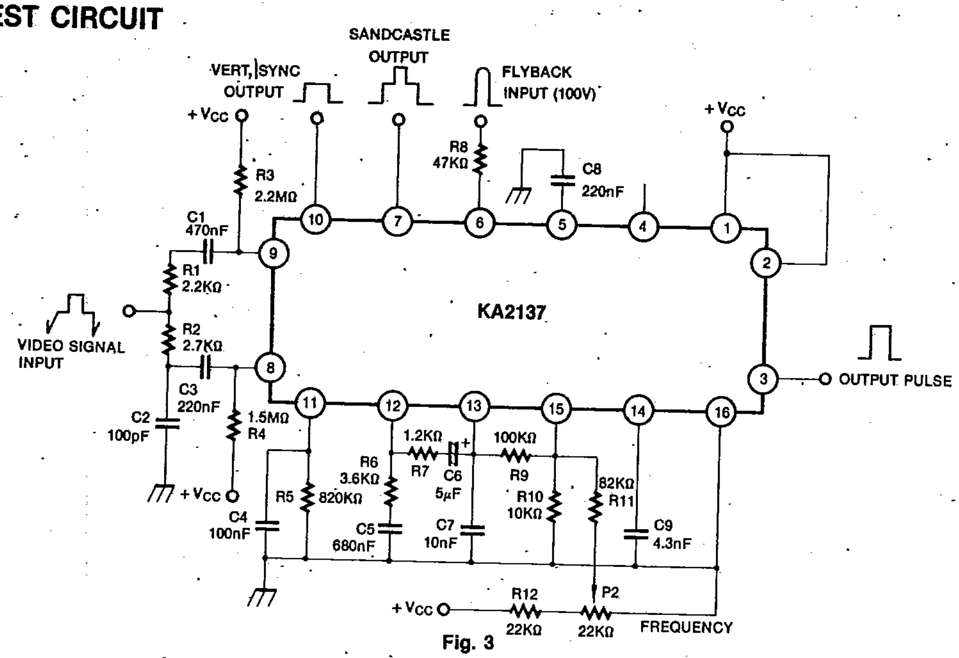


Fig. 3

TYPICAL APPLICATION CIRCUIT

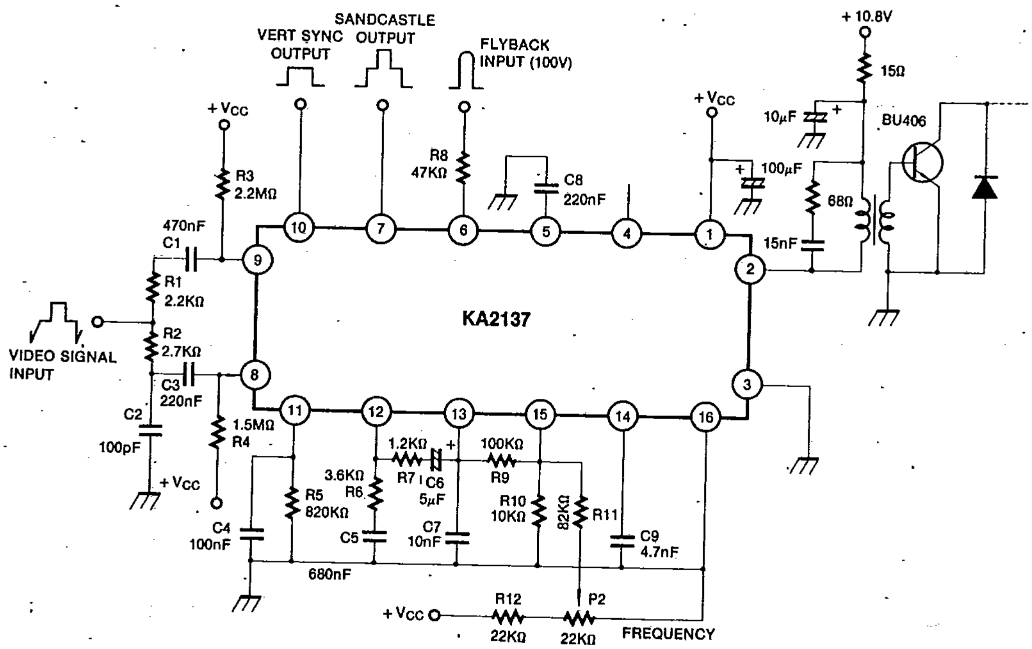


Fig. 2

Application circuit for large screen B/W and color TV

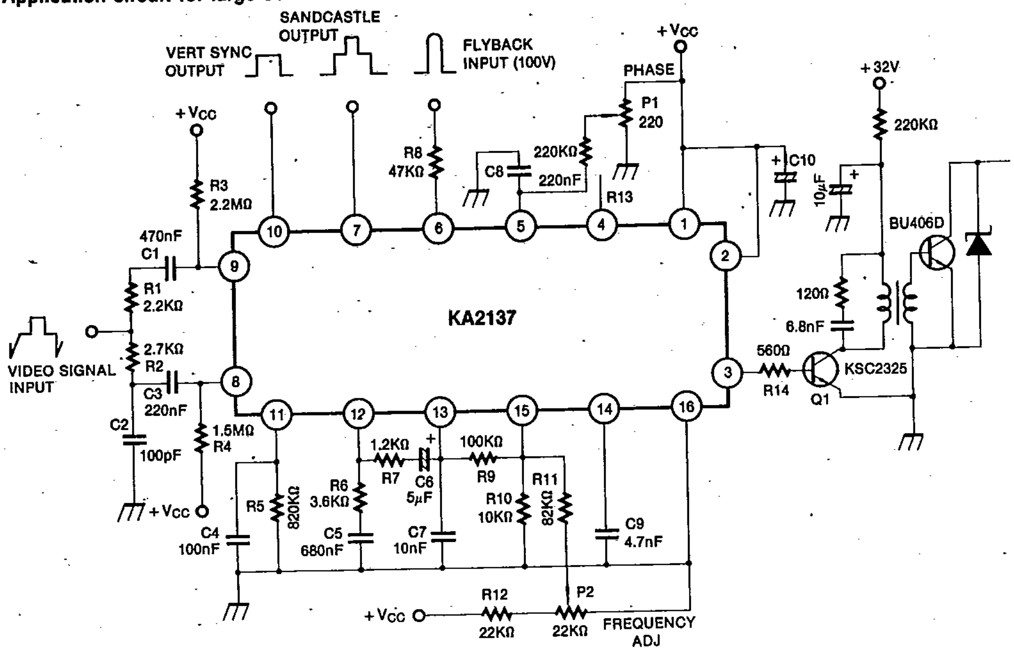


Fig. 4

Application circuit for power mosfet output stage

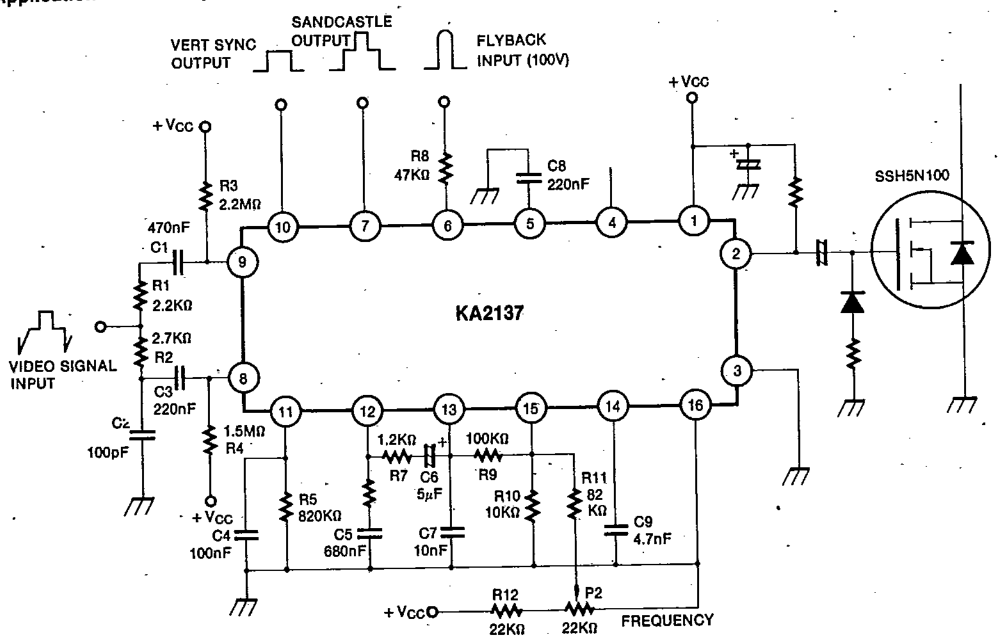


Fig. 5

Vertical sync. output pulse

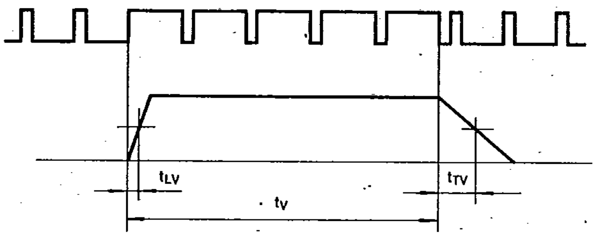


Fig. 6

Relationship of main waveform phases

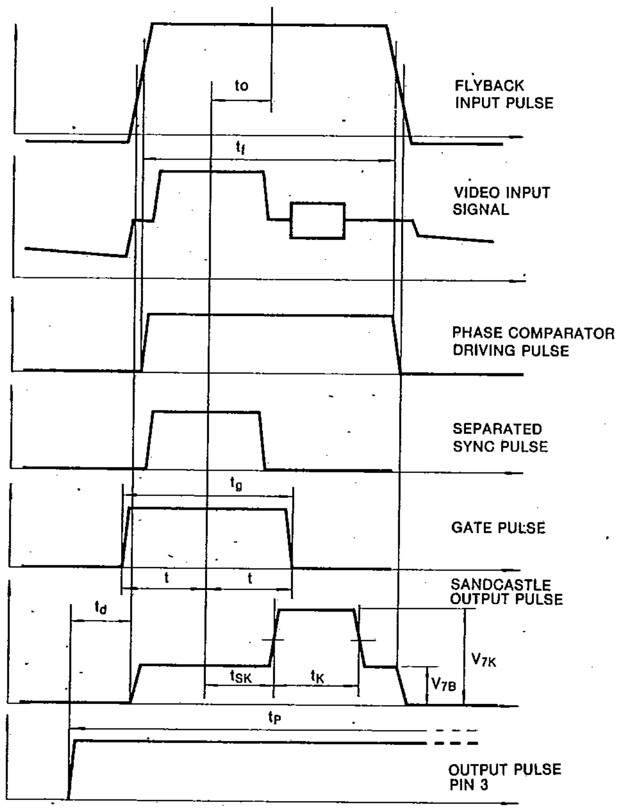


Fig. 7

4

FREE RUNNING FREQUENCY VS. SUPPLY VOLTAGE

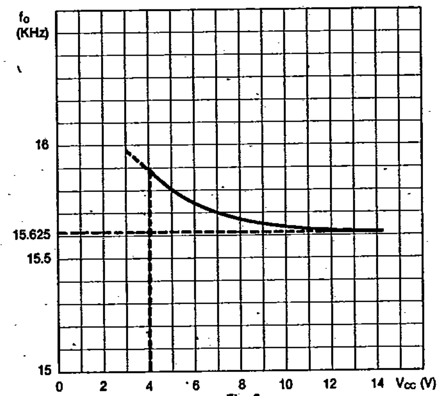


Fig. 8

OVERALL PHASE RELATION VS. SUPPLY VOLTAGE

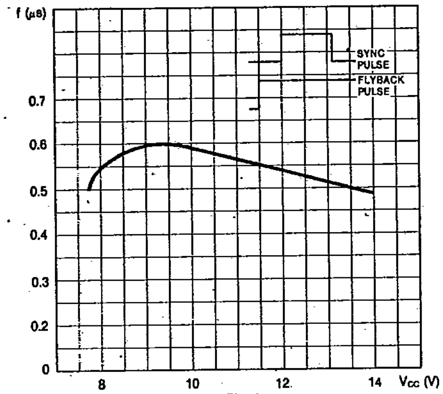


Fig. 9

LOOP GAIN

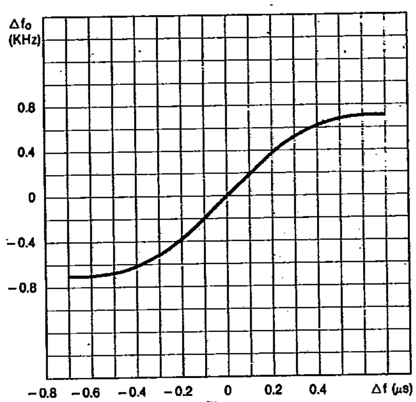


Fig. 10

APPLICATION INFORMATION

Pin 1 — Positive supply

The operating supply voltage of the device ranges from 10V to 13.2V.

Pin 2 and 3 — Output

The outputs of KA2137 are suitable for driving transistor output stages, they deliver positive pulse at pin 3 and negative pulse at pin 2.
The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required. The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.
Furthermore the output stages are internally protected against short circuit.

Pin 4 — Protection circuit input

By connecting pin 4 of the IC to earth the output pulses at pin 2 and 3 are shut off this function has been introduced to protect the final stages from overloads.
The same pulses are also shut off when the supply voltage falls below 4V.

Pin 5 — Phase shifter filter

To compensate for the delay introduced by the line final stages, the flyback pulses to pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator..
The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.
The maximum phase shift allowed is:

$$t_d = t_p - t_f$$

where t_f is the flyback pulse duration.
Pin 5 has high input and output resistance (current generator).

Pin 6 — Flyback input

The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.
The flyback input pulses are processed by a double threshold circuit; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

Pin 7 — Key and blanking pulse output

The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.
The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at pin 6. The sum of the two signals (sandcastle pulse) is available on low impedance at output pin 7.

Pin 8 and 9 — Sync separators inputs

The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.
The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing. An amplitude detector also connected to pin 8, blocks operation of the sync separators when interference or noise peaks exceed a certain preset value.

Pin 10 — Vertical sync output

The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin. The output impedance is typically 10KΩ and the lowest amplitude without load is 11V.

Pin 11 — Coincidence detector

From the oscillator waveform a gate pulse 7 μs wide is taken whose phase position is centered on the horizontal syncronism. The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.
This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync. When the two signals are not accurately aligned in time it means that the oscillatgor is not synchronized. In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on pin 12 (small time constant of low-pass filter).
This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.
In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.
Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on pin 12 and reduces the sensitivity of the phase comparator.
In these conditions the phase lock has high noise immunity (narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.
To optimize the behaviour of the IC if a video receorder is used, the state of the detector can be forced by connecting pin 11 to earth or to $+VV_{CC}$. The characteristics of the phase lock thus correspond to the lack of synchronization.

Pin 12 — Time constant switch, (see pin 11)

Pin 13 — Control current output

The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current I_{13} (proportional to the phase difference between the two signals) to pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.
The time constant of the filter can be switched between two values according to the impedance presented by pin 12. The voltage limiter at the output of the phase comparator limits the voltage excursion on pin 13 and therefore the frequency range in which the oscillator remains held-in.
The output resistance of pin 13 is:

low when $V_{13} < 4.3V$ or $V_{13} < 1.6V$
high when $1.6V < V_{13} < 4.3V$

To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync, a signal which inhibits the phase detectgor during the vertical interval is taken from the vertical output stage; inhibition remains even if the video signal is not present.
The free running frequency of the oscillator is determined by the values of the capacitor and of the resistor connected to pins 14 and 15 respectively.
To generate the line frequency output pulses, two thresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

Pin 14 — Oscillator (see pin 13)

Pin 15 — Oscillator control current input (see pin 13)

Pin 16 — Ground