October 1989
Edition 2.0

FUJITSU

DATA SHEET

MB98623RC/98624RC/98625RC
ONE TIME PROGRAMMABLE ROM CARD

CMOS 512K-BIT AND 1M-BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY CARD

The MB98623/624/625 are memory cards which are composed of one or two MBM27C512P OTP ROM in 38-pin plastic package. These cards have TTL compatible Input/Output and three state output level with fully static operation and a single +5V power supply is required.
They are capable of storing large amount of data and be interfaced to a host or personal computer. Their unique size and portability make them ideal for a wide variety of applications.

- Dimensions of the card are Fujitsu standard:
  2.216 width x 3.370 length x 0.081 height (inches)
- Fujitsu's original recessed edge connector helps to prevent chip damage from static electricity.
- Available various ZIF/LIF (Zero/Low Insertion Force) connectors for electrical interface between card and system
- Applications
  Printer, Typewriter, Word Processor Fonts and Type Styles
  Software Programs for Electronic Games
  Cooking Program cards for Electronic Ovens
  Program Control for Test Equipment

PLASTIC CARD
CRD-38P-M03

2

Construction		MB98623RC	MB98624RC	MB98625RC	Unit
Organization (word x bit)		65,536 x 8	131,072 x 8	65,536 x 16	bit
Access Time (max.)		250	250	250	ns
Power Dissipation	Active	158	158	315	mW
	TTL input level: Standby	5.25	10.5	10.5	mW
	CMOS input level: Standby	0.53	1.05	1.05	mW

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Programming Voltage	V_{PP}	-0.6 to +14.0	V
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{CC}+0.3	V
Temperature under Bias	T_{BIAS}	-10 to +60	°C
Storage Temperature	T_{STG}	30 to +70	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB98623RC

CMOS 512K (524,288)-BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY CARD

The MB98623 is a memory card which is composed of one MBM27C512P OTP ROM organized as 65,536 words x 8 bits housed in 38-pin plastic package. This card has TTL compatible Input/Output and three state output level with fully static operation and a single +5V power supply is required.

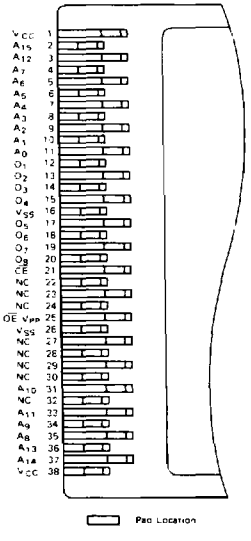
- Card size: 2.216 width x 3.370 length x 0.081 height (inches)
- Organization: 65,536 words x 8 bits
- Access time: 250 ns max.
- Full static operation: No clock required
- Three state output
- TTL compatible Input/Output
- Single +5V power supply
- Power dissipation: 158 mW max. (Active)
  5.25 mW max. (Standby, TTL input level)
  0.53 mW max. (Standby, CMOS input level)

2

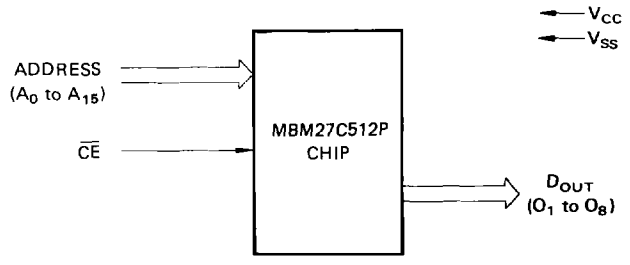
PIN DESCRIPTION

Symbol	Pin Number	Parameter
A_0 to A_{15}	2, 3, 4, 5, 6, 7, 8, 9, 10, 11 31, 33, 34, 35, 36, 37	Address Input
O_1 to O_{16}	12, 13, 14, 15, 17, 18, 19, 20	Data Input/Output
$\overline{CE}$	21	Chip Enable
$\overline{OE}/V_{PP}$	25	Output Enable/ Programming Supply Voltage
V_{CC}	1, 38	Supply Voltage (+5V)
V_{SS}	16, 26	Ground
NC	22, 23, 24, 27, 28, 29, 30, 32	Non Connection

PIN ASSIGNMENT
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



2

FUNCTIONAL TRUTH TABLE

Function / Mode	Address Input	Data I/O	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	V_{SS}
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	+5V	GND
Program	A_{IN}	D_{IN}	V_{IL}	+12.5V	+6V	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	+12.5V	+6V	GND

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
V_{CC} Active Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	I_{CC1}		4	30	mA
	f = 4MHz, I_{OUT} = 0mA	I_{CC2}		10	30	mA
V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	I_{SB1}			1	mA
	$\overline{CE}$ = V_{CC}±0.3V, I_{OUT} = 0mA	I_{SB2}		1	100	μA
Input Leakage Current	V_{IN} = 5.25V	I_{LI}			10	μA
Output Leakage Current	V_{OUT} = 5.25V	I_{LO}			10	μA
Output High Voltage	I_{OH} = -400μA	V_{OH1}	2.4			V
Output High Voltage	I_{OH} = -100μA	V_{OH2}	V_{CC}-0.7			V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}			0.45	V

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V, except $\overline{OE}/V_{PP}$)	C_{IN1}	–	15	20	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0V)	C_{IN2}	–	25	35	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	15	20	pF

MB98624RC

CMOS 1M (1,048,576)-BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY CARD

The MB98624 is a memory card which is composed of two MBM27C512P OTP ROM organized as 131,072 words x 8 bits housed in 38-pin plastic package. This card has TTL compatible Input/Output and three state output level with fully static operation and a single +5V power supply is required.

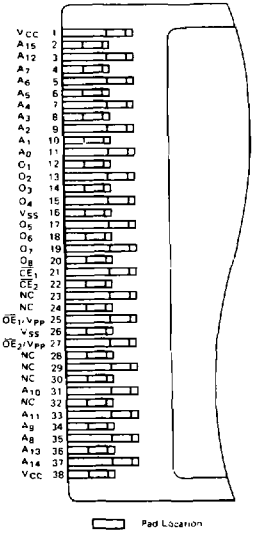
- Card size: 2.216 width x 3.370 length x 0.081 height (inches)
- Organization: 131,072 words x 8 bits
- Access time: 250 ns max.
- Full static operation: No clock required
- Three state output
- TTL compatible Input/Output
- Single +5V power supply
- Power dissipation: 158 mW max. (Active)
  10.5 mW max. (Standby, TTL input level)
  1.05 mW max. (Standby, CMOS input level)

2

PIN DESCRIPTION

Symbol	Pin Number	Parameter
A_0 to A_{15}	2, 3, 4, 5, 6, 7, 8, 9, 10, 11 31, 33, 34, 35, 36, 37	Address Input
O_1 to O_{16}	12, 13, 14, 15, 17, 18, 19, 20	Data Input/Output
$\overline{CE}_1$, $\overline{CE}_2$	21, 22	Chip Enable
$\overline{OE}_1/V_{PP}$, $\overline{OE}_2/V_{PP}$	25, 27	Output Enable/ Programming Supply Voltage
V_{CC}	1, 38	Supply Voltage (+5V)
V_{SS}	16, 26	Ground
NC	23, 24, 28, 29, 30	Non Connection

PIN ASSIGNMENT
(TOP VIEW)



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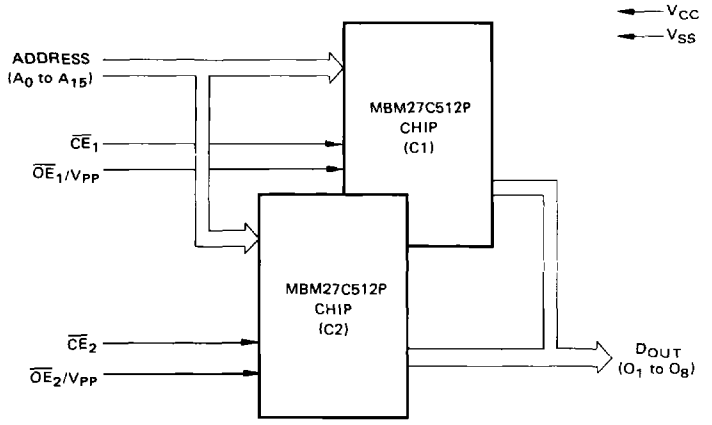
FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE

Function / Mode	Address Input	Data I/O	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}_1/V_{PP}$	$\overline{OE}_2/V_{PP}$	V_{CC}	V_{SS}
Read 1	A_{IN}	D_{OUT}	V_{IL}	V_{IH}	V_{IL}	Don't Care	+5V	GND
Read 2	A_{IN}	D_{OUT}	V_{IH}	V_{IL}	Don't Care	V_{IL}	+5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}	+5V	GND
Standby	Don't Care	High-Z	V_{IH}	V_{IH}	Don't Care	Don't Care	+5V	GND
Program 1	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{PP}	Don't Care	+6V	GND
Program 2	A_{IN}	D_{IN}	V_{IH}	V_{IL}	Don't Care	V_{PP}	+6V	GND
Program Verify 1	A_{IN}	D_{OUT}	V_{IL}	V_{IH}	V_{IL}	Don't Care	+6V	GND
Program Verify 2	A_{IN}	D_{OUT}	V_{IH}	V_{IL}	Don't Care	V_{IL}	+6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	V_{IH}	V_{PP}	V_{PP}	+6V	GND

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
V_{CC} Active Current	$\overline{CE} = V_{IL}$*, I_{OUT} = 0mA	I_{CC1}		4	30	mA
	f = 4MHz, I_{OUT} = 0mA	I_{CC2}		10	30	mA
V_{CC} Standby Current	$\overline{CE_1} = \overline{CE_2} = V_{IH}$	I_{SB1}			2	mA
	$\overline{CE_1} = \overline{CE_2} = V_{CC}$±0.3V, I_{OUT} = 0mA	I_{SB2}		2	200	μA
Input Leakage Current	V_{IN} = 5.25V	I_{LI}			20	μA
Output Leakage Current	V_{OUT} = 5.25V	I_{LO}			20	μA
Output High Voltage	I_{OH} = −400μA	V_{OH1}	2.4			V
Output High Voltage	I_{OH} = −100μA	V_{OH2}	V_{CC}−0.7			V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}			0.45	V

Note: * Either $\overline{CE_1}$ or $\overline{CE_2}$ must be satisfied V_{IH}.

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V, except $\overline{OE}/V_{PP}$)	C_{IN1}	–	25	30	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0V)	C_{IN2}	–	25	35	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	20	25	pF

MB98625RC

CMOS 1M (1,048,576)-BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY CARD

The MB98625 is a memory card which is composed of two MBM27C512P OTP ROM organized as 65,536 words x16bits housed in 38-pin plastic package. This card has TTL compatible Input/Output and three state output level with fully static operation and a single +5V power supply is required.

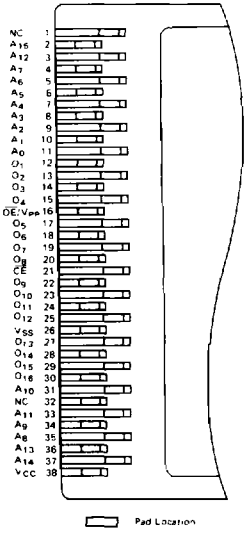
- Card size: 2.216 width x 3.370 length x 0.081 height (inches)
- Organization: 65,536 words x 16 bits
- Access time: 250 ns max.
- Full static operation: No clock required
- Three state output
- TTL compatible Input/Output
- Single +5V power supply
- Power dissipation: 315 mW max. (Active)
  10.5 mW max. (Standby, TTL input level)
  1.05 mW max. (Standby, CMOS input level)

2

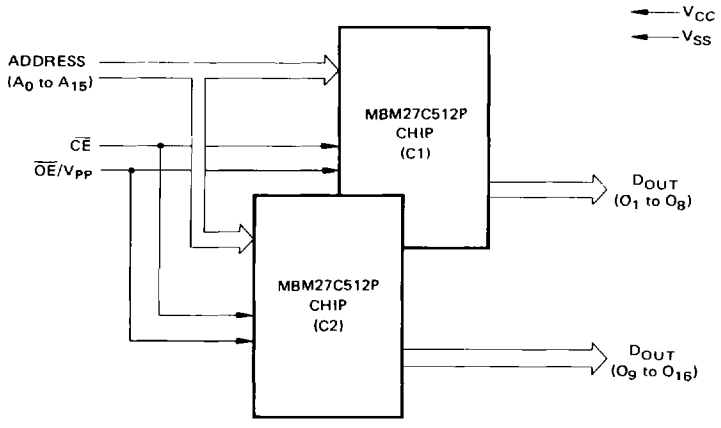
PIN DESCRIPTION

Symbol	Pin Number	Parameter
A_0 to A_{15}	2, 3, 4, 5, 6, 7, 8, 9, 10, 11 31, 33, 34, 35, 36, 37	Address Input
O_1 to O_{16}	12, 13, 14, 15, 17, 18, 19, 20 22, 23, 24, 25, 27, 28, 29, 30	Data Input/Output
$\overline{CE}$	21	Chip Enable
$\overline{OE}/V_{PP}$	16	Output Enable/ Programming Supply Voltage
V_{CC}	38	Supply Voltage (+5V)
V_{SS}	26	Ground
NC	1, 32	Non Connection

PIN ASSIGNMENT
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL TRUTH TABLE

Function / Mode	Address Input	Data I/O	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	V_{SS}
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	+5V	GND
Program	A_{IN}	D_{IN}	V_{IL}	+12.5V	+6V	GND
Program Verify	A_{IN}	D_{OUT}	V_{iL}	V_{IL}	+6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	+12.5V	+6V	GND

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
V_{CC} Active Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	I_{CC1}		8	60	mA
	f = 4MHz, I_{OUT} = 0mA	I_{CC2}		20	60	mA
V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	I_{SB1}			2	mA
	$\overline{CE}$ = V_{CC}±0.3V, I_{OUT} = 0mA	I_{SB2}		2	200	µA
Input Leakage Current	V_{IN} = 5.25V	I_{LI}			20	µA
Output Leakage Current	V_{OUT} = 5.25V	I_{LO}			20	µA
Output High Voltage	I_{OH} = -400µA	V_{OH1}	2.4			V
Output High Voltage	I_{OH} = -100µA	V_{OH2}	V_{CC}-0.7			V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}			0.45	V

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN}=0V, expect $\overline{OE}/V_{PP}$)	C_{IN1}		25	30	pF
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}		50	60	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		15	20	pF

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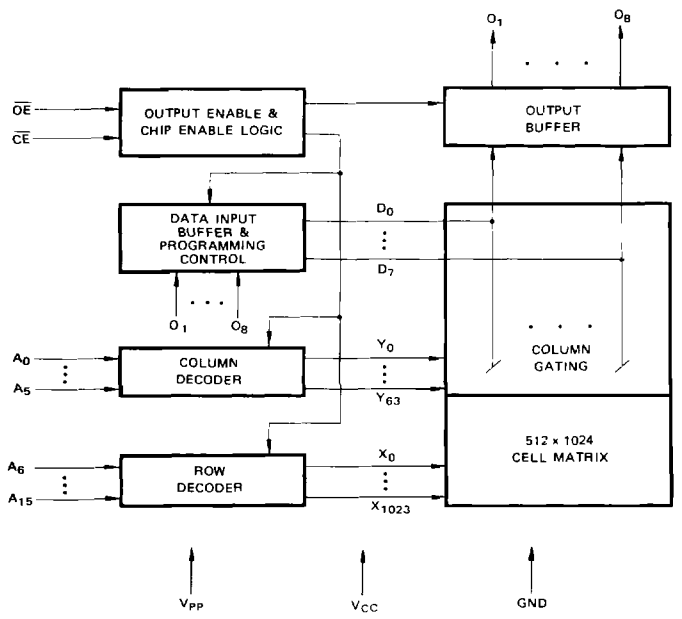
COMMON CHARACTERISTICS (MBM27C512P)

BLOCK DIAGRAM FOR EACH CHIP



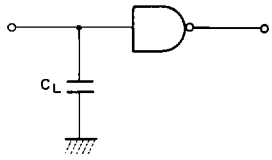
RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	V
Ambient Temperature	T_A	0		50	°C

AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Level	:	0.8 to 2.2V
Input Pulse Rise/Fall Time	:	$t_T \leq 20ns$
Timing Reference Levels		
Input	:	V_{IL} = 1.0V, V_{IH} = 2.2V
Output	:	V_{OL} = 0.8V, V_{OH} = 2.0V
Output Load	:	1TTL gate and 100pF



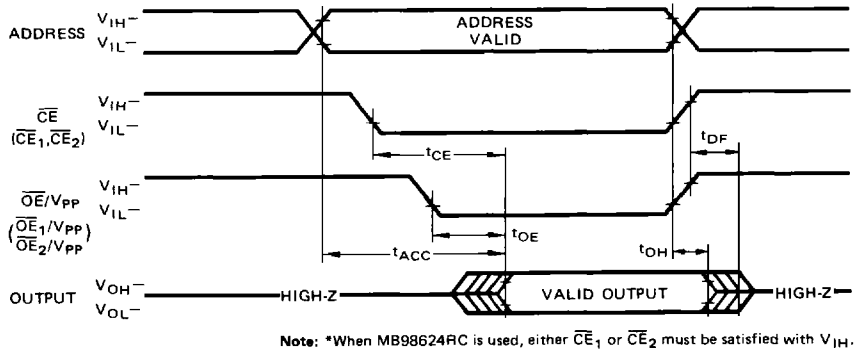
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit
		Min	Max	
Address Access Time*1	t_{ACC}		250	ns
Chip Enable Access Time	t_{CE}		250	ns
Output Enable Access Time*1	t_{OE}		100	ns
Output Disable Time*2	t_{DF}	0	60	ns
Output Hold Time	t_{OH}	0		ns

Note: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

READ WAVEFORM



Note: *When MB98624RC is used, either $\overline{CE}_1$ or $\overline{CE}_2$ must be satisfied with V_{IH}.

PROGRAMMING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, the MB98623/624/625 has all bits in the "1", or high state. "0's" are loaded into the MB98623/624/625 through the procedure of programming.

The MB98623/624/625 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ is V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart).

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{CE}$ = V_{IH}.
3) Clear the programming pulse counter (X←0).
4) Input data to respective pins.
5) Apply one programming pulse (t_{PW} = 1ms Typ) to $\overline{CE}$.
6) Increment the counter (X←X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X=25 and programmed data is not verified, the device fails. If X<25 and programmed data is not varified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3Xms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G←G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V) because it is required that one programming pulse width does not exceed 78.75ms at each address.

Quick Pro™ is a trademark of FUJITSU LIMITED

PROGRAMMING INFORMATION (continued)

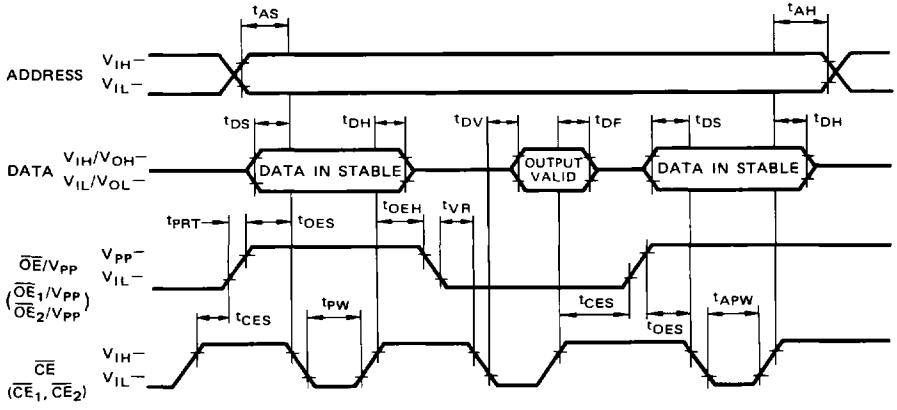
DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC}*1 = 6 ± 0.25V, V_{PP}*2 = 12.5 ± 0.3V)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Max		
				MB98623	MB98624/625	
Input Leakage Current	V_{IN} = 5.25V/0.45V	I_{LI}		10	20	μA
V_{CC} Supply Current		I_{CC}		30	60	mA
V_{PP} Supply Current during Programming Pulse	$\overline{CE}$ = V_{IL}	I_{PP}		50	100	mA
Input High Level		V_{IH}	2.2	V_{CC}+0.3	V_{CC}+0.3	V
Input Low Level		V_{IL}	-0.1	0.8	0.8	V
Output High Voltage during Verify	I_{OH} = -400μA	V_{OH}	2.4			V
Output Low Voltage during Verify	I_{OL} = 2.1mA	V_{OL}		0.45	0.45	V

Note: *1 V_{CC} *must be applied either coincidently or before* V_{PP} *and removed either coincidently or after* V_{PP}.

*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

PROGRAMMING WAVEFORM



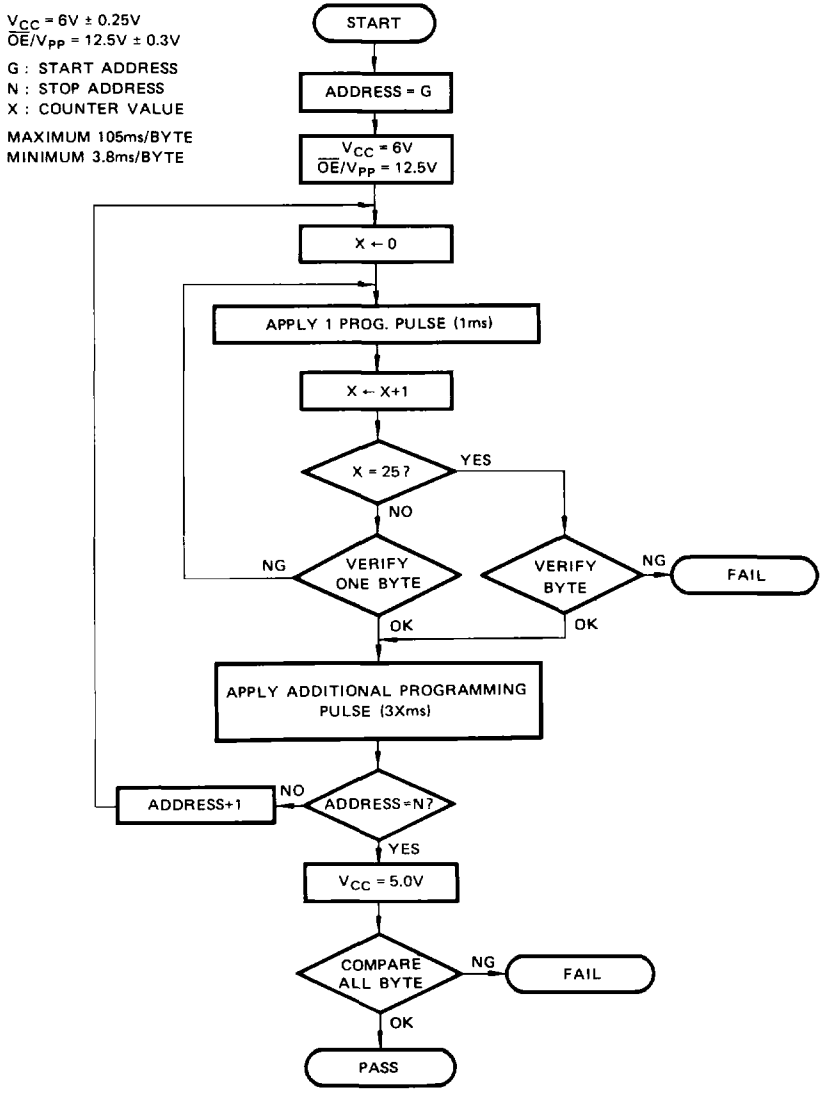
PROGRAMMING INFORMATION (continued)

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6 ± 0.25V, V_{PP} = 12.5 ± 0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Setup Time	t_{VS}	2			μs
Address Setup Time	t_{AS}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Hold Time	t_{OEH}	2			μs
V_{PP} Recovery Time	t_{VR}	2			μs
Chip Enable to Data Valid	t_{DV}			1	ns
Output Disable to Output Float Delay	t_{DF}			130	ns
V_{PP} Program Pulse Rise Time	t_{PRT}	50			ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Additional Programming Pulse Width	t_{APW}	2.85	3	78.75	ms

PROGRAMMING INFORMATION (continued)

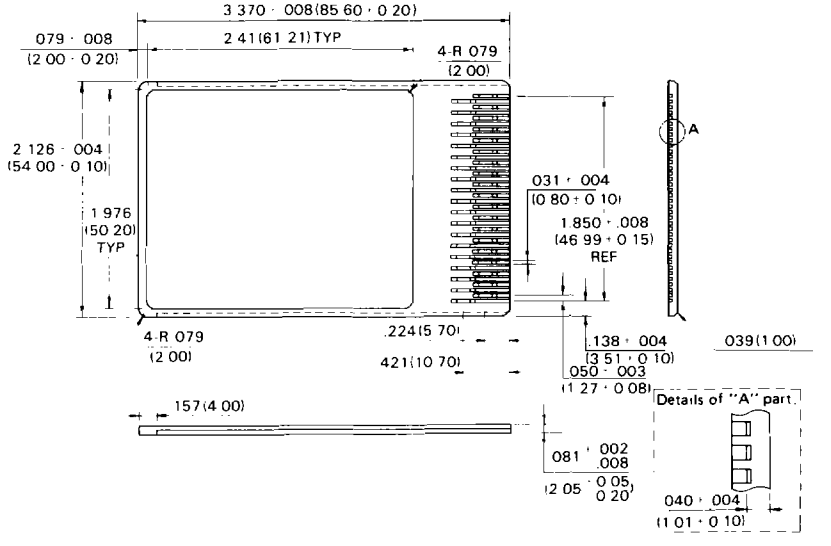
PROGRAMMING FLOW CHART FOR Quick Pro™



Quick Pro™ is a trademark of FUJITSU LIMITED

PACKAGE DIMENSIONS

38-PAD PLASTIC CARD
(CASE No.: CRD-38P-M03)



Dimensions in inches (millimeters)

Memory Card Use Notice

- When not in use, it is recommended that the memory card be stored in its anti-static vinyl bag to prevent damage from static electricity.
- The card should be inserted before power-on to avoid possible data conflicts between the card and equipment. If the card is inserted or extracted with power-on, data may be output on the data pins even though $\overline{CE}$ and $\overline{OE}$ is at an "H".