National Semiconductor

August 1996

74ABT16541 16-Bit Buffer/ Line Driver with TRI-STATE® Outputs

General Description

The 'ABT16541 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/ receiver. The device is byte controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

Features

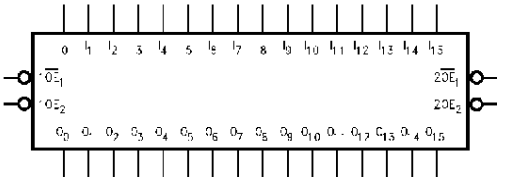
- Separate control logic for each nibble
- 16-bit version of the 'ABT541
- Outputs sink capability of 64 mA, source capability of 32 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Commercial	Package Number	Package Description
74ABT16541CSSC (Note 1)	MS48A	48-Lead (0.300" Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT16541CMTD (Notes 1, 2)	MTD48	48-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

Note 1: Devices also available in 13" reel. Use suffix = SSCX and MTDX.

Note 2: Contact factory for package availability.

Logic Symbol



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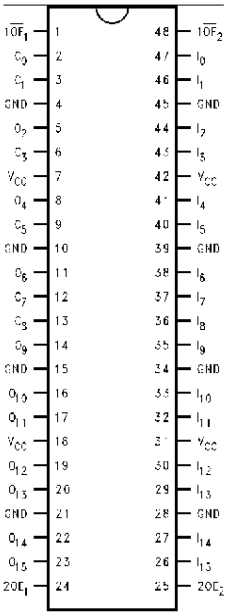
Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

Pin Assignment for SSOP



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Functional Description

The 'ABT16541 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is byte (8 bits) controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

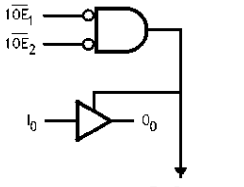
Truth Tables

Inputs			Outputs
$\overline{1OE}_1$	$\overline{1OE}_2$	I_0–I_7	O_0–O_7
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Inputs			Outputs
$\overline{2OE}_1$	$\overline{2OE}_2$	I_8–I_{15}	O_8–O_{15}
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



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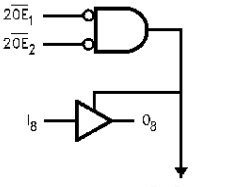

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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT16541 Min	ABT16541 Typ	ABT16541 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74ABT	2.5			V	Min	I_{OH} = −3 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	74ABT			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 1)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 1)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V All Other Pins GND
I_{CCH}	Power Supply Current				100	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				100	μA	Max	$\overline{OE}_n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 1)	No Load			0.1	mA/MHz	Max	Outputs Open, $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed but not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT16541			Units	V_{CC}	Conditions C_L = 50 pF R_L = 500Ω
		Min	Typ	Max			
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.4	0.7	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−1.0		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.7	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.4		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT T_A = +25°C V_{CC} = +5V C_L = 50 pF			74ABT T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation	1.0	2.3	3.9	1.0	3.9	ns
t_{PHL}	Delay Data to Outputs	1.0	2.7	3.9	1.0	3.9	
t_{PZH}	Output Enable	1.5	3.5	6.3	1.5	6.3	ns
t_{PZL}	Time	1.5	3.5	6.3	1.5	6.3	
t_{PHZ}	Output Disable	1.0	4.2	6.7	1.0	6.7	ns
t_{PLZ}	Time	1.0	3.2	6.7	1.0	6.7	

Extended AC Electrical Characteristics

Symbol	Parameter	74ABT −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 50 pF 16 Outputs Switching (Note 4)			74ABT T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 250 pF 1 Output Switching (Note 5)		74ABT T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 250 pF 16 Outputs Switching (Note 6)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{toggle}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.0	ns
t_{PHL}	Data to Outputs	1.5		5.3	1.5	6.0	2.5	8.0	
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.8	2.5	9.5	ns
t_{PZL}		1.5		6.5	2.5	7.8	2.5	8.5	
t_{PHZ}	Output Disable Time	1.0		6.7	(Note 7)		(Note 7)		ns
t_{PLZ}		1.0		6.7					

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT	74ABT	Units
		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 3)	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 4)	
		Max	Max	
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	1.5	ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.5	ns
t_{PS} (Note 5)	Duty Cycle LH−HL Skew	1.5	1.5	ns
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.7	2.0	ns
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0	2.5	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). The specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

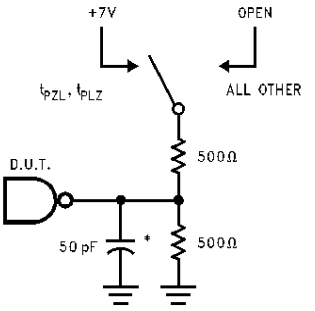
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 5.0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz; per MIL STD-883B, Method 3012.

AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

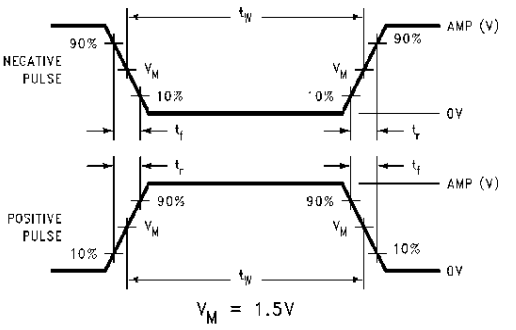

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FIGURE 2a. Test Input Pulse Requirements

Amplitude	Rep Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements

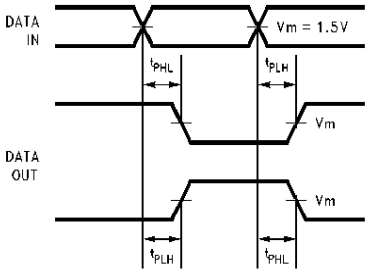

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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

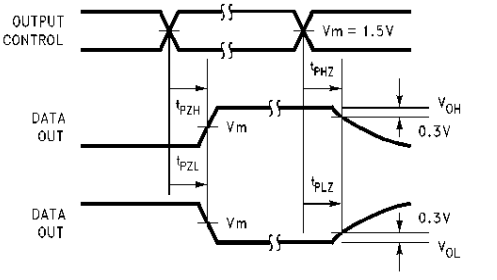

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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

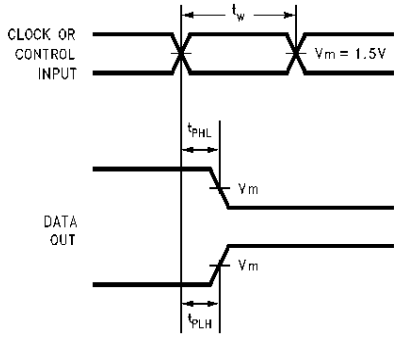

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FIGURE 4. Propagation Delay, Pulse Width Waveforms

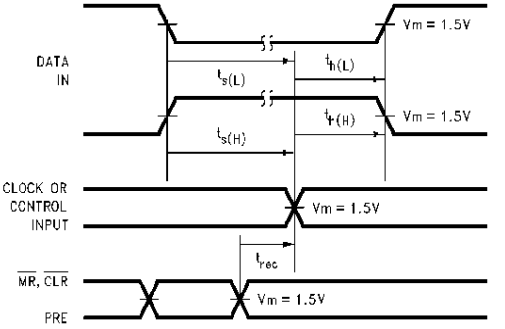

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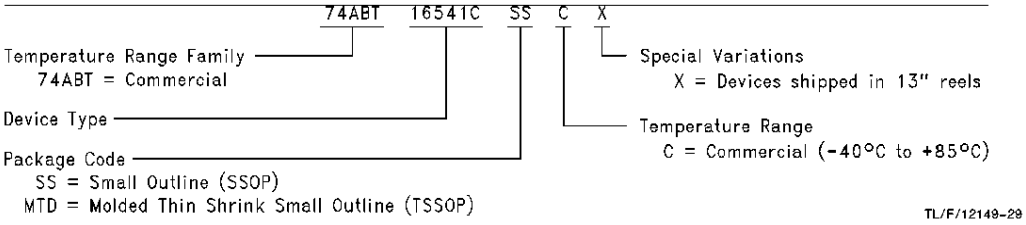
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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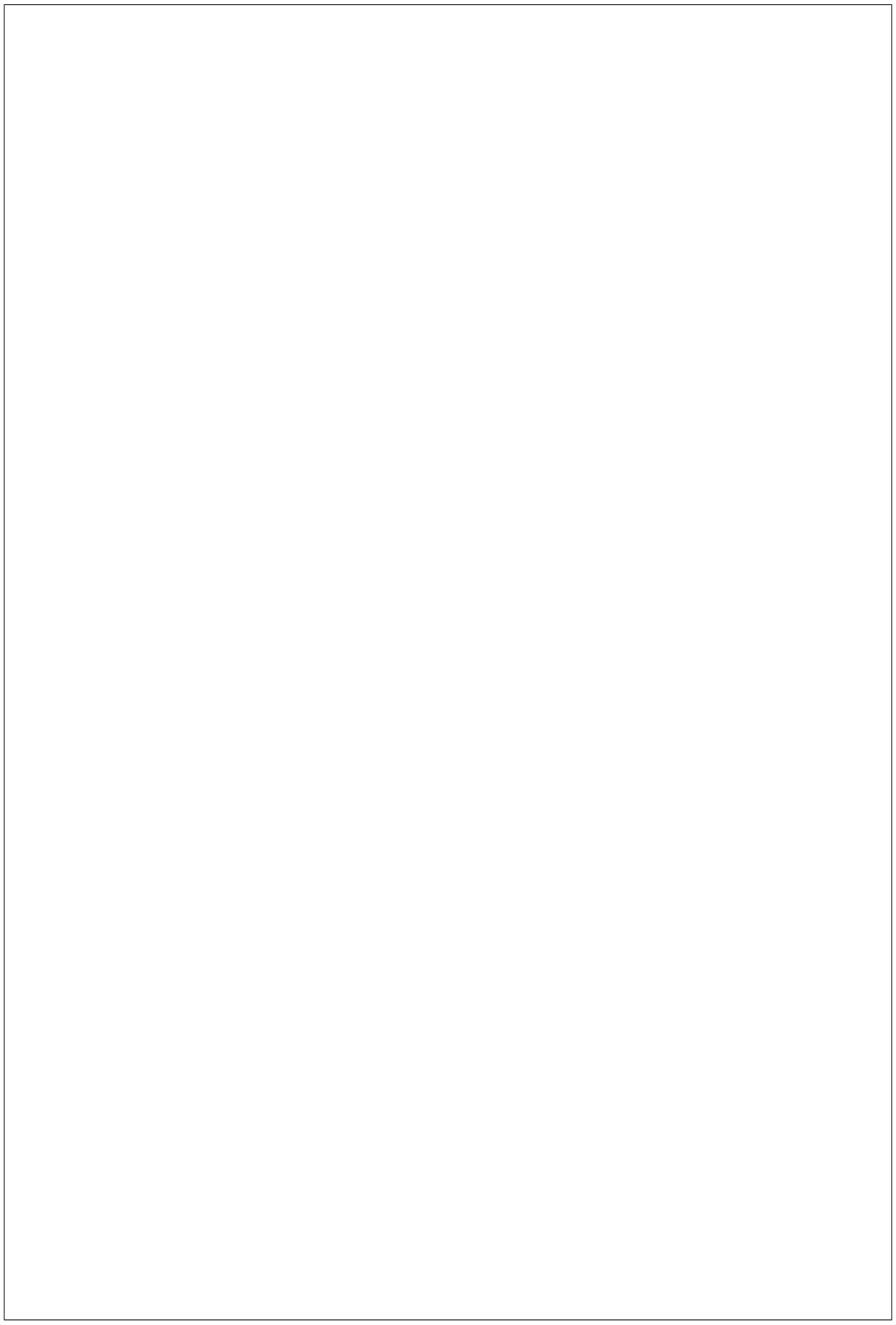
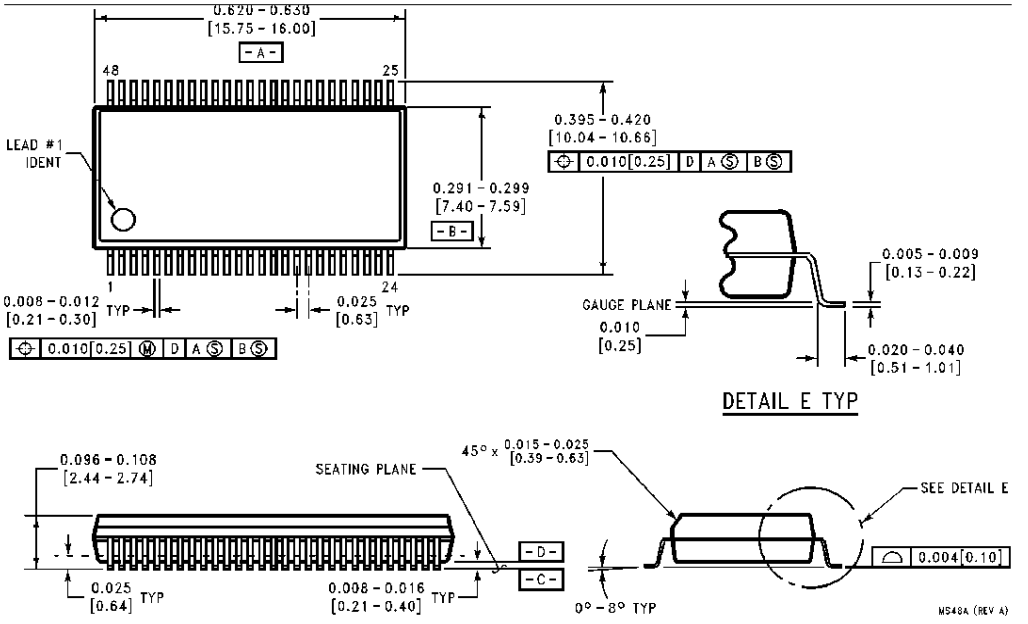
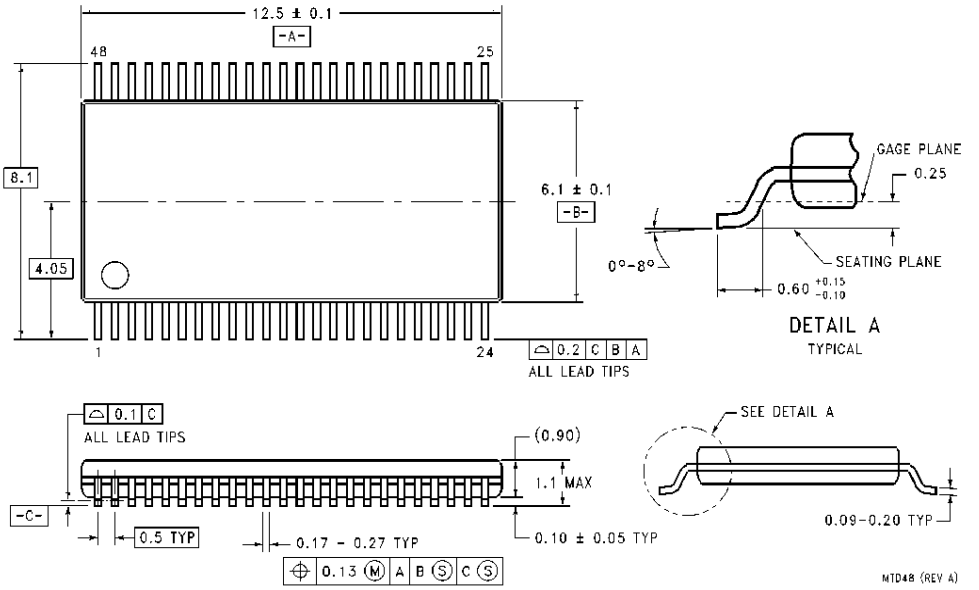


Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead SSOP (0.300" Wide) (SS)
NS Package Number MS48A

Physical Dimensions millimeters (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48

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