M 3002

Low Power 4-Bit 32 kHz RTC with Battery Pin

Features

- Battery pin, bus disabled on power down
- Easy to use like a RAM with fast access time
- Interface compatible with both Intel and Motorola microprocessors
- TTL/CMOS compatible
- Standby on power down typically 5 μA
- Chrono and alarm time interrupt
- Can be synchronized to a master clock pulse
- Pulse output once per second, minute or hour
- $\overline{\text{BUSY}}$ pin can be used as a 1 Hz strobe for display control
- BCD data format
- Leap-year and auto roll-over of week number
- Packages DIP 16 and SO 16
- $\overline{\text{SYNC}}$ pin to tune the device to an external time reference
- Frequency tuning and test modes

Description

The M 3002 is a monolithic low power CMOS device which functions as a 4 bit real time clock. The device is accessed by chip select ($\overline{\text{CS}}$) with read and write function timing provided by $\overline{\text{OE}}$ and R/$\overline{\text{W}}$. The M 3002 is driven by an external 32.768 kHz crystal, and uses the 24 hour system. An alarm can be preprogrammed up to one month in advance. The timer can measure elapsed time up to 24 hours. Time data is stored in a 15 by 8 bit RAM in BCD format. An 8 bit status word in the RAM controls the mode of operation.

Applications

- Single board computers
- Industrial controllers
- PABX and telephone systems
- Taximeters, lorry tachos
- Data loggers

Typical Operating Configuration

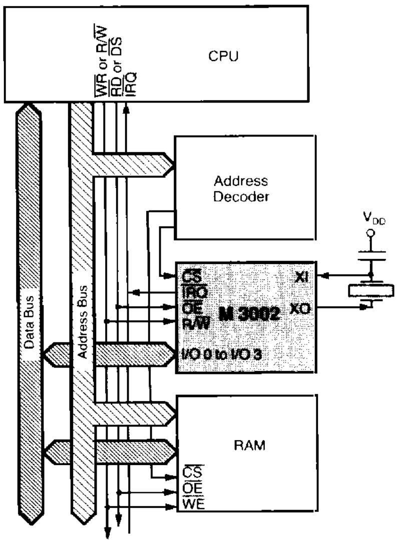


Fig. 1

Pin Assignment

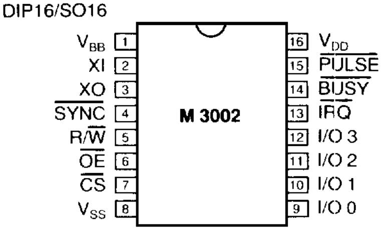


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD}	$V_{DD\,max}$	$V_{SS} + 8.0$ V
Minimum voltage at V_{DD}	$V_{DD\,min}$	$V_{SS} - 0.3$ V
Maximum voltage at XI and XO	V_{max}	$V_{DD} + 0.3$ V
Minimum voltage at XI and XO	V_{min}	$V_{BB} - 0.3$ V
Max. voltage at any signal pin	V_{max}	$V_{DD} + 0.3$ V
Min. voltage at any signal pin	V_{min}	$V_{SS} - 0.3$ V
Maximum storage temperature	T_{STOmax}	+ 150°C
Minimum storage temperature	T_{STOmin}	-65°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature[1]	T_A	−40		+85	°C
Logic supply voltage	V_{DD}	+2.4	+5.0	+5.5	V
Battery voltage[2]	$V_{DD}-V_{BB}$	+2.4		+5.0	V
Crystal Characteristics					
Frequency[3]	f		32.768		kHz
Load capacitance	C_L	8	10	13	pF
Series resistance	R_S		20	50	kΩ
Trimmer capacitance	C_T	5	15	40	pF

Table 2

[1] The maximum operating temperature is confirmed by sampling at initial device qualification. In production, all devices are tested at +70°C. On request devices tested at +85°C can be supplied.

[2] See Fig. 10 and Fig. 11

[3] Parallel resonant crystal

Electrical Characteristics

$V_{DD} = 5.0$ V ± 10%, $V_{SS} = 0$ V, $V_{BB} = 3.0$ V, and $T_A = 0$°C to +70°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Total static supply	I_{DD}	all outputs open, all inputs at V_{DD}			10	µA
Standby current	I_{BB}	$V_{DD} = 0$ V		5	8	µA
Inputs and Outputs						
Input logic low	V_{IL}				0.8	V
Input logic high	V_{IH}		2.4			V
Output logic low on I/O pins	V_{OL}	$I_{OL} = 3.2$ mA			0.4	V
Output logic low	V_{OL}				0.4	V
Output logic high on I/O pins	V_{OH}	$I_{OH} = 2$ mA	2.4			V
Output logic high on $\overline{IRQ}$	V_{OH}	100k pullup to V_{DD}	2.4			V
Output logic high	V_{OH}		2.4			V
Input leakage	I_{IN}	$0.0 < V_{IN} < 5.0$			1	µA
Oscillator						
Starting voltage	V_{STA}	$C_T = 18$pF	1.8			V
Input capacitance on XI	C_{IN}			3.7		pF
Output capacitance on XO	C_{OUT}			25		pF
Start-up time	T_{STA}	$C_T = 18$pF		0.6	5	s
Frequency stability	Δf/f	$2.0 \leq V_{BB} \leq 5.0$ V $C_T = 5$ pF		5	10	ppm/V

Table 3

Timing Characteristics

V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = 3.0 V, and T_A = 0°C to +70°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Chip select duration	t_{CS}		280			ns
RAM access time[1]	t_{ACC}			150	270	ns
Time between two transfers	t_W		1000			ns
Data valid to Hi-impedance[2]	t_{DF}			180	300	ns
Write data settle time[3]	t_{DW}		200			ns
Data hold time[4]	t_{DH}		0			ns

Table 4

[1] t_{ACC} starts from $\overline{OE}$ or $\overline{CS}$, whichever activates last.

[2] t_{DF} starts from $\overline{OE}$ or $\overline{CS}$, whichever deactivates first.

[3] t_{DW} ends at R/$\overline{W}$ or $\overline{CS}$, whichever deactivates first.

[4] t_{DH} starts from R/$\overline{W}$ or $\overline{CS}$, whichever deactivates first.

Timing Waveforms

Read Timing for Both Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola (Advanced R/$\overline{W}$ with $\overline{OE}$ Tied to $\overline{CS}$)

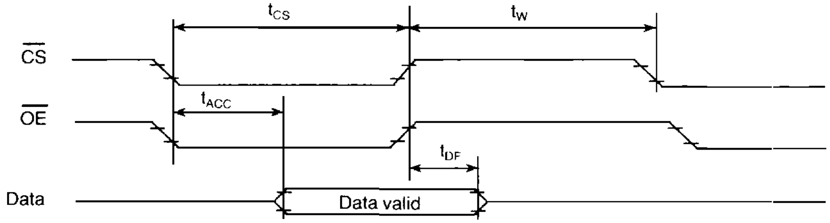


Fig. 3a

Write Timing for Both Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola (Advanced R/$\overline{W}$ with $\overline{OE}$ Tied to $\overline{CS}$)

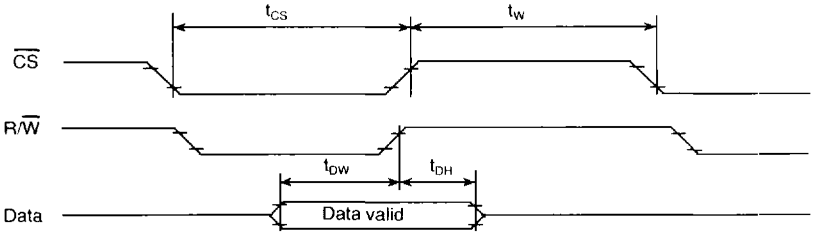


Fig. 3b

Block Diagram

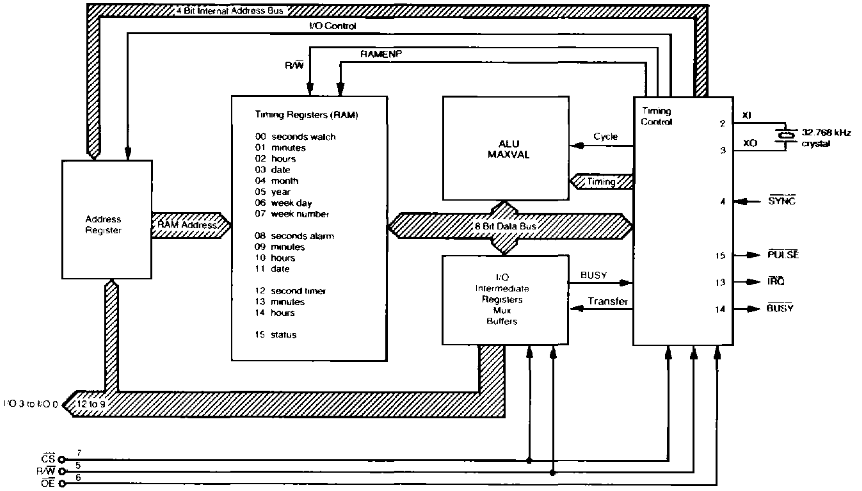


Fig. 4

Pin Description

Pin	Name	Function
1	V_{BB}	Negative battery terminal
2	XI	32.768 kHz quartz input
3	XO	32.768 kHz quartz output
4	$\overline{\text{SYNC}}$	Time synchronization input
5	R/$\overline{\text{W}}$	$\overline{\text{WR}}$ (Intel) or R/$\overline{\text{W}}$ (Motorola), see Fig. 10 and 11
6	$\overline{\text{OE}}$	$\overline{\text{RD}}$ (Intel) or $\overline{\text{DS}}$ (Motorola), see Fig. 10 and 11
7	$\overline{\text{CS}}$	Chip select input
8	V_{SS}	Ground terminal
9	I/O 0	Data bus input/output lines Address bus input lines
10	I/O 1	
11	I/O 2	
12	I/O 3	
13	$\overline{\text{IRQ}}$	Interrupt request output (open drain)
14	$\overline{\text{BUSY}}$	Internal update cycle status output
15	$\overline{\text{PULSE}}$	Programmable timing pulse output
16	V_{DD}	Positive supply terminal (substrate)

Table 5

Functional Description

Power Supply and Data Retention

The M 3002 can be powered with a supply voltage between 2.4 and 5.5 V, and backed up with a battery or supercap (2.4 to 5.0 V), as indicated in Fig. 10 and 11, to ensure operation and data retention during power-down. Because of the low power consumption of the device, lithium cells or standard rechargeable cells give many years of effective life. If the battery is not required then connect V_{BB} to V_{SS}. When the voltage at the V_{BB} pin drops below the voltage at the V_{SS} pin, access to the device is disabled. The I/O lines and the outputs $\overline{\text{BUSY}}$ and $\overline{\text{PULSE}}$ are set to a high impedance state. The open-drain output $\overline{\text{IRQ}}$ will be inactive until V_{DD} is restored. Care should be taken to avoid the occurance of improper states on interfacing signal lines.

RAM

The 16 x 8 RAM is used to store all clock, alarm, timer and status data. The allocation of RAM addresses is shown in Table 6. All time data are stored in Binary Coded Decimal (BCD) format. The transfer of this data between the internal 8-bit bus and the I/O lines is performed by the bidirectional I/O buffer (see Block Diagram Fig. 4). If the alarm and timer functions are not needed, then the RAM section from these functions, addresses 8 to E hex, may be used as non-volatile system storage by software. It should be noted however that, if the unused function is inadvertently activated by altering the status word, the stored data may be modified.

I/O Address Locations

Address Hex	Address Dec	Data	Group	Max. Value	Operations
0	0	Seconds	Watch	59	Time data incremented under control of status bit 0
1	1	Minutes		59	
2	2	Hours		23	
3	3	Date		28, 29, 30, 31	
4	4	Month		12	
5	5	Year		99	
6	6	Week day		07	
7	7	Week no.		53	
8	8	Seconds	Alarm	59	Alarm data, providing an IRQ under control of status bit 1
9	9	Minutes		59	
A	10	Hours		23	
B	11	Date		28, 29, 30, 31	
C	12	Seconds	Timer	59	Timer data incremented under control of status bit 4
D	13	Minutes		59	
E	14	Hours		23	
F	15	Status	Status		Control

Table 6

Status and Control

The function of the individual bits of the status word are shown in Table 7. The status word, address F hex, controls the timekeeping functions performed in the ALU section of the M 3002 (see Block Diagram Fig. 4). The status word must be written on recovery from a total power loss, V_{DD} and the battery voltage < 2.4 V.

Status Word

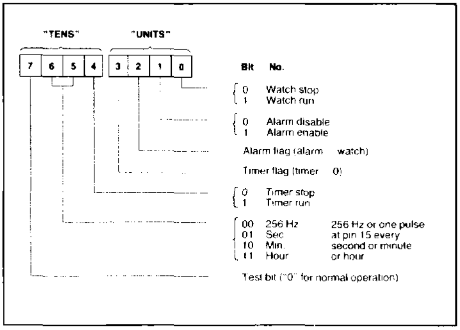


Table 7

RAM Access

The interface between the M 3002 and the host microprocessor consists of four bidirectional multiplexed data/address lines (I/O lines), three control lines ($\overline{CS}$, $\overline{OE}$, R/$\overline{W}$), and an interrupt request line ($\overline{IRQ}$). Three steps are required to access a RAM address. The first access transfers the 4-bit address of the data location, the second reads or writes data bits 7 to 4 (tens) to or from the address written in step one, and the third reads or writes data bits 3 to 0 (units). Fig. 5 shows the 3 step access sequence.

3 Step Access Sequence

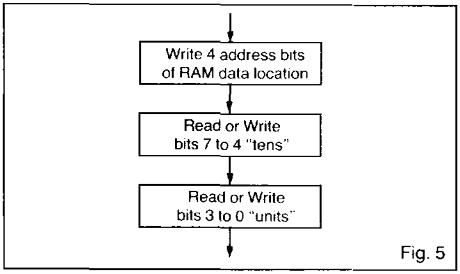


Fig. 5

An internal multiplexer defines the 3 step access sequence position. A 3 step access sequence is began by writing the RAM 4-bit address and then the M 3002 treats the next two accesses as the 4-bit data transfers, tens first, units second. A read access, while the multiplexer is expecting an address write, will not begin a 3 step access sequence. The multiplexer can be initialized (expecting an address write) by two read accesses. Read accesses will complete a 3 step access sequence, but will not begin one. The multiplexer must be initialized by software on every power up of the system including power up of the M 3002 from a power loss (V_{DD} and the battery voltage < 2.4 V) condition.

RAM Access and Internal Update Cycles

Every second an internal update occurs and lasts between 0.73 ms and 6 ms. During this update cycle, the multiplexer is initialized, the $\overline{BUSY}$ output is active, and a read will give F hex on the I/O pins. The RAM is allocated to the ALU (see Block Diagram Fig. 4). If an external data transfer is in progress (see RAM Access section), the internal update cycle is delayed for a maximum of one second. After a delay of one second the external data transfer will be aborted and the RAM assigned to the internal update cycle. With the multiplexer in its initial state, reading the M 3002 will give 0 hex if an internal update cycle is not in progress and F hex if in progress. Thus prior to beginning a 3 step access sequence, software must read the I/O pins to determine if the RAM is available. Additionally the $\overline{BUSY}$ pin goes active while an internal update cycle is in progress. To prevent an update during a sequence of transfers, for example hours, minutes and seconds, there must be less than 2 ms between each transfer (i.e. 3 step access sequence). If software continuously polls the M 3002 to seek an event or refresh a display then the delay between two poll sequences (e.g. read hours, minutes, seconds) should be greater than 6 ms to allow an update cycle to occur.

RAM Access and Interrupts

Any false or aborted access will make the M 3002 jump incorrectly to the next step in the 3 step access sequence. Access to the M 3002 is not re-entrant and so the software routine accessing the M 3002 must complete the 3 step access sequence before another software routine can access the device. Interrupt software routines must not access the M 3002 unless it can be guaranteed that the M 3002 is not in a 3 step access sequence. Additionally interrupt software routines must not delay the 3 step access sequence in the background routine longer than one second or an internal update cycle will occur within the M 3002. It is recommended that all software routines reading or writing to the M 3002 call one of the software routine structures, shown in Fig. 6, for each device access.

M 3002 Software Access Routines

```
M 3002 _ WRITE:
    Disable maskable interrupts
        Wait for Bus = 0 hex
        Write address to M 3002
        Write data bits 7 to 4 to M 3002
        Write data bits 3 to 0 to M 3002
    Enable maskable interrupts
M 3002 _ READ:
    Disable maskable interrupts
        Wait for Bus = 0 hex
        Write address to M 3002
        Read data bits 7 to 4 from M 3002
        Read data bits 3 to 0 from M 3002
    Enable maskable interrupts
```

Fig. 6

Non maskable interrupt routines must not access the M 3002 as it cannot be guaranteed that the M 3002 is not in the middle of a 3 step access sequence. In a multitasking software environment the task accessing the M 3002 must not be interrupted during a 3 step access sequence.

Alarm and $\overline{\text{IRQ}}$

An alarm date and time may be preset in RAM addresses 8 to B hex. During every update cycle, the ALU (see Block Diagram Fig. 4) compares the contents of the watch addresses, 0 to 3 hex, with the preset alarm time data. If the alarm is enabled (status word bit 1) and the alarm time data matches the watch addresses 0 to 3 hex, the $\overline{\text{IRQ}}$ pin goes active and the alarm flag (status word bit 2) is set to indicate to the software the source of the interrupt. $\overline{\text{IRQ}}$ will remain active until the software acknowledges the interrupt by clearing the alarm flag (status word bit 2). If the alarm is enabled (status word bit 1), and an alarm RAM location set to FF hex, this location is not compared with the associated watch location. Thus it is possible to achieve a repeat feature where an alarm occurs every programmed number of, seconds, or seconds and minutes, or seconds, minutes and hours. The M 3002 does not generate interrupts until the 3 step access sequence is complete.

Timer and $\overline{\text{IRQ}}$

By setting the status word bit 4 (timer enable bit), the preset time data in RAM addresses C hex to E hex, increments every second with the update cycle. When passing from 23:59:59 to 00:00:00, the timer flag (status word bit 3) is set and the $\overline{\text{IRQ}}$ output goes active. $\overline{\text{IRQ}}$ will remain active until software acknowledges the interrupt by clearing the timer flag (status word bit 3). The M 3002 does not generate interrupts until the 3 step access sequence is complete.

$\overline{\text{PULSE}}$ Output

The $\overline{\text{PULSE}}$ output can be programmed with bits 5 and 6 of the status word, as shown in Table 7, to produce a negative pulse of 64 μs duration, every second, minute, or hour, while the watch is running. Clearing bits 5 and 6 of the status word will produce a 256 Hz square wave on the $\overline{\text{PULSE}}$ pin. The latter feature is intended for frequency tuning, see section Frequency Tuning.

$\overline{\text{SYNC}}$ Input

If the $\overline{\text{SYNC}}$ input is set low for longer than 200 μs, the watch will synchronize to the falling edge of this $\overline{\text{SYNC}}$ signal with a precision of ± 2 ms. The seconds RAM location (address 0 hex) will be cleared and if the contents were ≥ 30, the minutes location (address 1 hex) will be incremented.

Frequency Tuning

The $\overline{\text{PULSE}}$ pin will output a 256 Hz square wave signal if the bits 5 and 6 of the status word are cleared. The period of the signal on the $\overline{\text{PULSE}}$ pin can be adjusted by the crystal trimmer. The nominal period for 256 Hz is 3.90625 ms (see Fig. 7)

Calibration Circuit

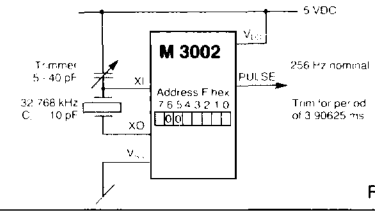


Fig. 7

Crystal Layout

In order to ensure proper oscillator operation we recommend the following standard practices.

- Keep traces as short as possible
- Use a guard ring around the crystal and capacitor or trimmer.

Fig. 8 shows the recommended layout.

P.C.B. Layout

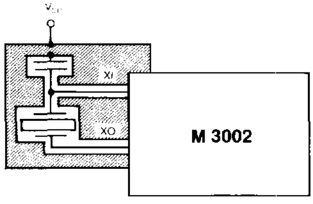


Fig. 8

Test

Some of the various test features added to the M 3002, some can be activated by software. Table 8 shows the available test modes and how they may be activated.

Test Modes

Status bit 7	Status bit 5	$\overline{\text{SYNC}}$ input	Function
0	0	V_{SS}	Normal operation
1	0	V_{SS}	First 5 stages of divider chain bypassed: acceleration by a factor of 32[1]
1	1	V_{SS}	Parallel increment of all time and timer data at 1 Hz depending on the status of bit 0 and bit 4[2]
1	1	V_{DD}	Parallel increment of all time and timer data at 32 Hz depending on the status of bit 0 and bit 4 First 5 stages of divider chain bypassed: thus acceleration by a factor of 32[1]

Table 8

[1] External signal generator to be used

[2] Crystal or extended signal generator

An external signal generator can be used to drive the M 3002. Fig. 9 shows how to connect the signal generator. The speed can be increased by increasing the signal generator frequency to a maximum of 128 kHz. Test modes can be activated while using an external signal generator if required. To leave test, the test bit (status word bit 7) must be cleared by software. Test corrupts the watch and timer data and so all parameters should be reloaded after a test session.

Signal Generator Connection

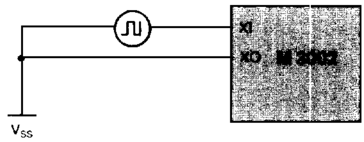


Fig. 9

Typical Application

Intel Microprocessor Interfaced with the M 3002 in a Typical Configuration

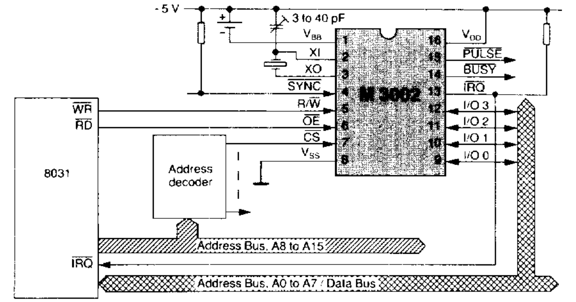
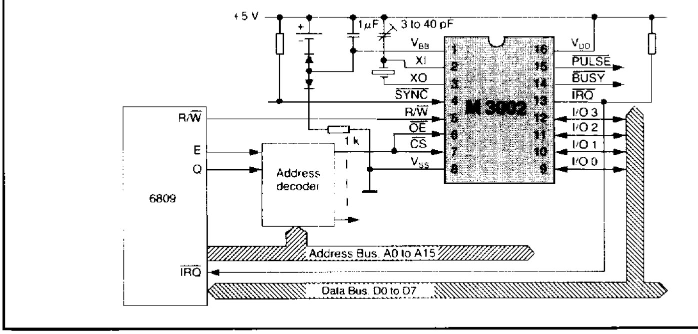


Fig. 10

Motorola Microprocessor Interfaced with the M 3002 in a Low Battery Current Configuration



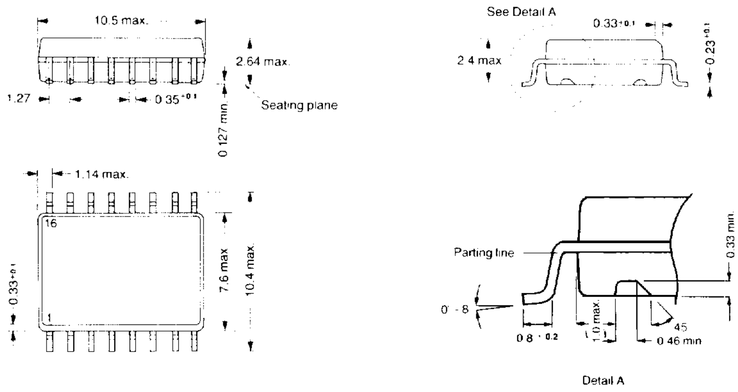
Note 1: The 1 µF and 1 kΩ protect pin V_{SS} against excessive voltage fluctuations during violent switchovers to or from battery supply.

Note 2: The minimum standby voltage ($V_{DD} - V_{BB}$) is 2.4 V, and thus in the low current configuration the battery voltage must be 2.4 V + the diode voltage.

Fig. 11

Package and Ordering Information

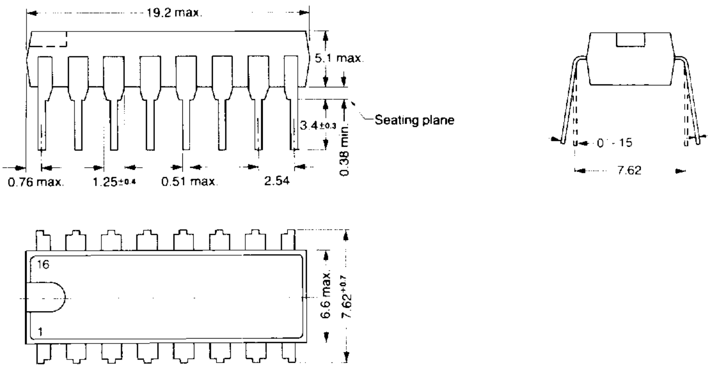
Dimensions of SO Package



Dimensions in mm

Fig. 12

Dimensions of DIP Package



Dimensions in mm

Fig. 13

Ordering Information

The M 3002 is available in the following packages:

DIP 16-pin plastic package	M 3002 16P
SO 16-pin wide plastic package	M 3002 16S

Chip form on request.

When ordering, please specify the complete part number and package.