1.0 INTRODUCTION

The AHA3710 is a single chip lossless/lossy compression coprocessor IC for systems requiring compression of 24-bit color image data in Red-Green-Blue (RGB) or Color-By-Line (CBL) formats. The device is also capable of compressing 8-bit Grayscale (GS) images. No external SRAM is required.

The Color Adaptive Data Compression (CADC™) algorithm implemented in the AHA3710 is based on an adaptive DPCM algorithm that includes an optional lossy mode. The lossy mode is completely controllable by user parameters. The data throughput rate remains constant regardless of compression mode.

Decompression is performed in software provided at no charge to certified AHA3710 customers. No charge license and development support is available from AHA for the decompression software.

This document contains functional descriptions, system configurations, register descriptions, electrical characteristics and ordering information. It is intended for system designers considering a compression coprocessor in their embedded applications. Software simulation of both compression and decompression are available for evaluation. A comprehensive Designer's Guide complements this document to assist with the system design. Section 9.0 contains a list of related technical publications.

1.1 CONVENTIONS, NOTATIONS AND DEFINITIONS

- Active low signals have an "N" appended to the end of the signal name. For example, CSN.
- "Signal assertion" means the output signal is logically true.
- Hex values are represented with a prefix of "0x", such as Register "0x00". Binary values do not contain a prefix.
- A range of signal names or register bits is denoted by a set of colons between the numbers. Most significant bit is always shown first, followed by least significant bit. For example, UD[7:0] indicates signal names UD7 through UD0.
- Mega Bytes per second is referred to as MBytes/sec or MB/sec.
- Reserved bits in registers are referred as "*res*".

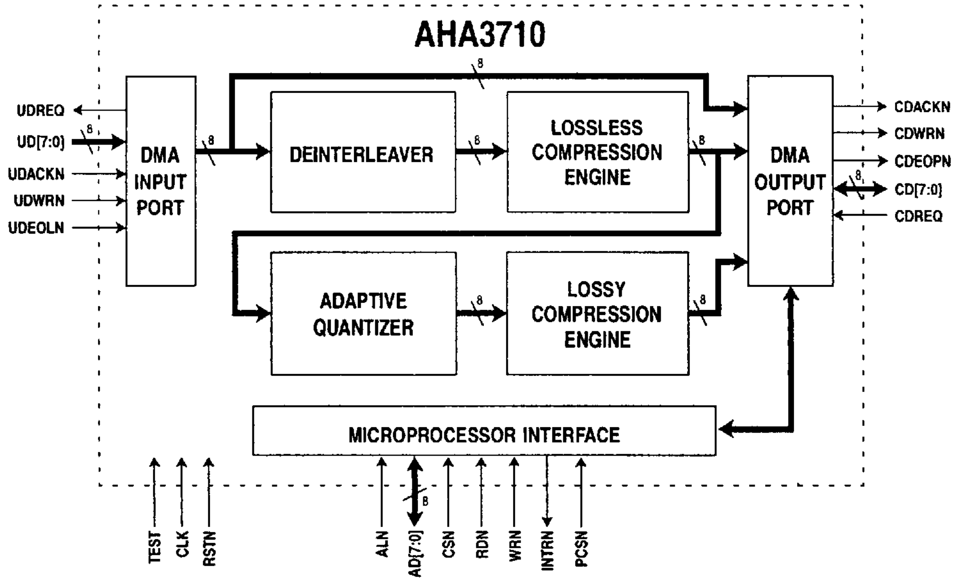
1.2 FEATURES

PERFORMANCE:
- 6 MBytes/sec maximum rate
- No external SRAM required
- Average compression ratio using CADC™ lossless for an 8.5"x11.0" color image is 2 to 1; lossy is 4 to 1
- 1200 x 1200 dpi resolution for 11″ x 17″ images

FLEXIBILITY:
- Programmable Line Length, Page Length, Header Length and Scan Line Offset
- Programmable DMA acknowledge length
- Pass-through mode passes raw data through compression engine
- Compressed image size in bytes maintained by internal registers
- Peripheral Access Mode - for interfacing to devices that do not have separate data and microprocessor ports
- Interrupt for End-of-Page
- Single-chip compression solution – no external SRAM required
- Multiple input formats: RGB,CBL and GS

OTHER:
- Small footprint: 56 pin TSSOP package
- Low Power dissipation
- Software emulation available

Figure 1: Functional Block Diagram



1.3 FUNCTIONAL OVERVIEW

The AHA3710 coprocessor device has two DMA ports for the transfer of data. These are the 8-bit Uncompressed Data (UD) port and Compressed Data (CD) port.

The device accepts uncompressed data through the UD port. Compressed data or Pass-Through data is available on the CD port. The sustained data rate through the compression engine is 6 MBytes/sec.

The Sections 2.0 through 3.0 describe the various configurations, programming and other special considerations in developing a compression system using the AHA3710.

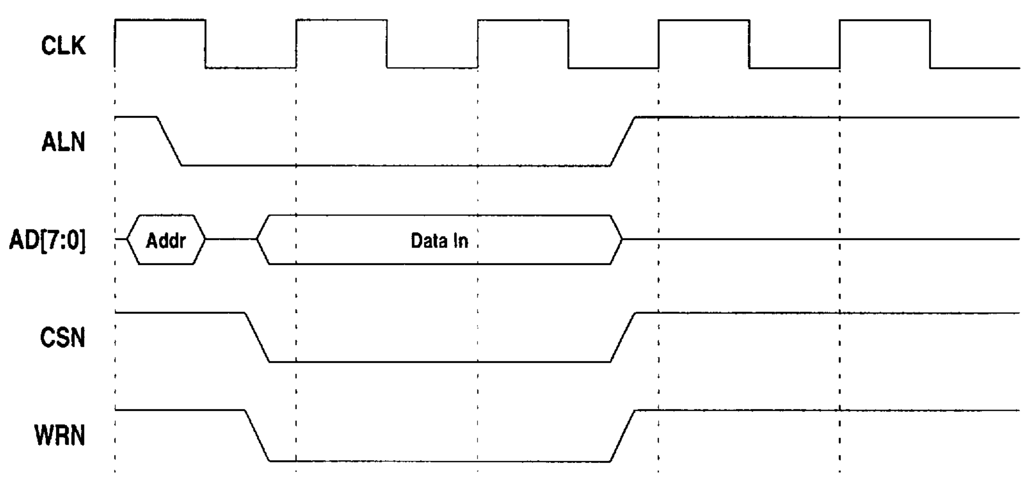
2.0 SYSTEM CONFIGURATION

This section provides information on connecting the AHA3710 to various microprocessors.

2.1 MICROPROCESSOR INTERFACE

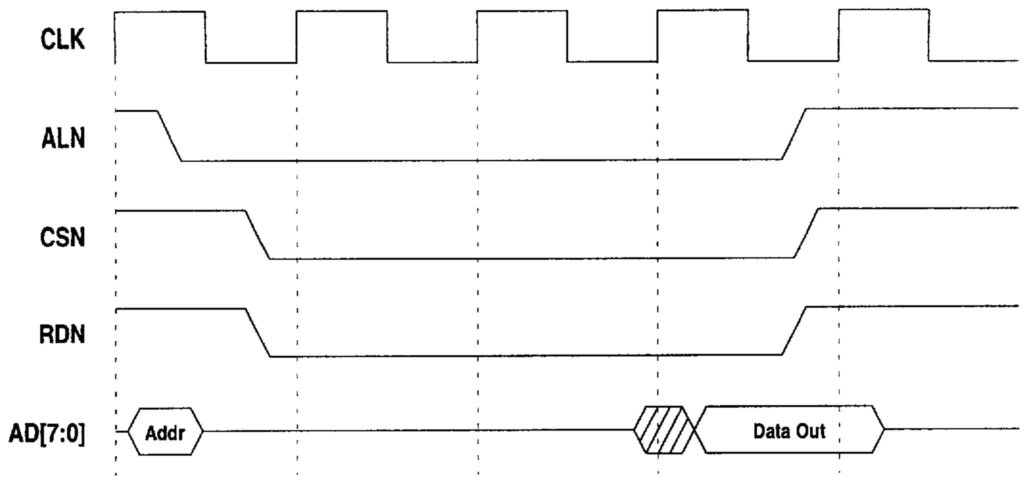
The AHA3710 is capable of interfacing directly to a microprocessor for embedded applications. All register accesses to the AHA3710 are performed on an 8-bit bidirectional bus, using an Intel® style interface. Both address and data are multiplexed on this bus. See Figure 2 and Figure 3 for a functional description of register accesses.

Figure 2: Microprocessor Port Write



■ 0255381 0002773 1T5 ■

Figure 3: Microprocessor Port Read



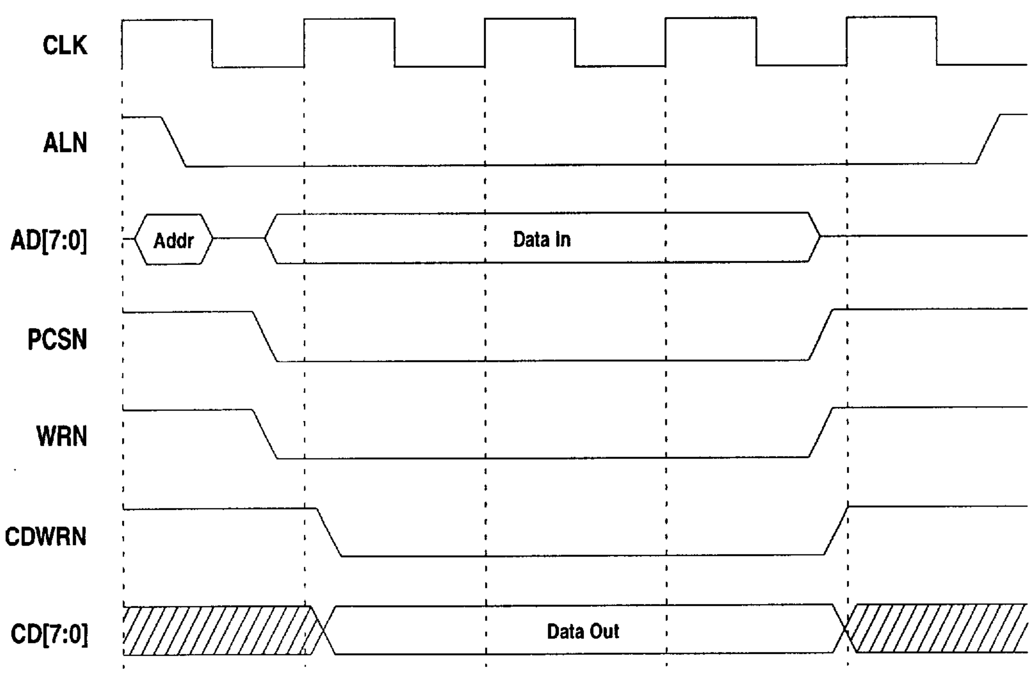
2.2 PERIPHERAL ACCESS MODE

The AHA3710 is capable of accessing the registers of the downstream device connected to the CD Port. This mode is useful when the downstream device does not have separate data and microprocessor ports.

To perform microprocessor reads and writes through the CD Port, the AHA3710 must be paused by writing a one to the PAUSE bit of the *Command* register. Once the PAUSE command has been issued the paused state of the AHA3710 is reflected in the CD Port Paused (CDPP) and UD Port Paused (UDPP) bits of the *Status* register. The microprocessor must verify that the CD Port of the AHA3710 has paused before attempting a peripheral access. An interrupt will be issued if a peripheral access is attempted through the CD Port when it is not paused. UDPP is provided for status of the AHA3710 only and does not impact Peripheral Access Mode.

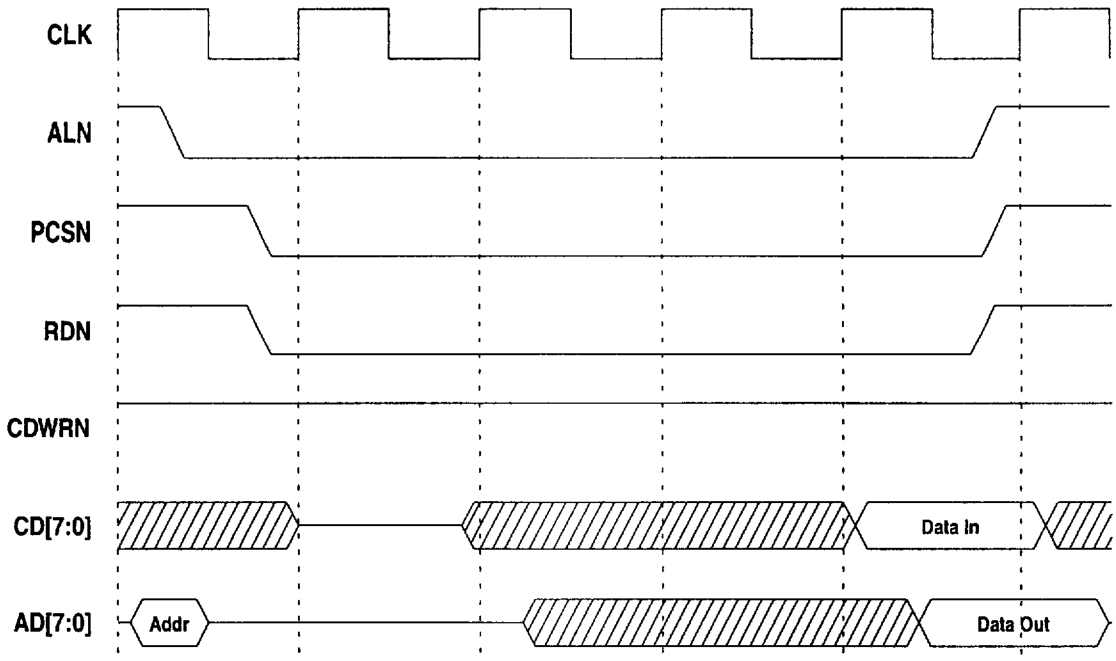
See Figure 4 and Figure 5 for a functional description of peripheral accesses.

Figure 4: Peripheral Access Write



0255381 0002774 031

Figure 5: Peripheral Access Read



This section describes the Uncompressed Data (UD) and Compressed Data (CD), DMA ports and their data formats.

2.3 DATA PORT TRANSFERS

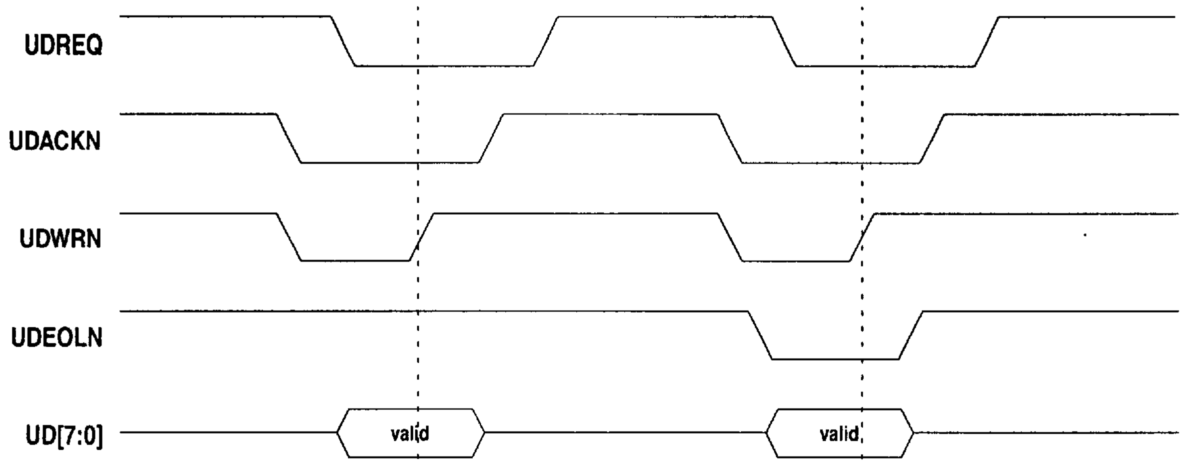
Data transfers are controlled by asynchronous handshake between the AHA3710 and the system. Figure 6 shows two byte transfers into the AHA3710. Figure 7 shows two single byte transfers out of the AHA3710 and Figure 8 shows a multi-byte transfer (CDREQ held high).

The AHA3710 requests input data by asserting UDREQ. The upstream device acknowledges the transfer by driving UDACKN low. Data is latched into the UD Port on the rising edge of the UDWRN or UDACKN signal, whichever is first. Both UDREQ and UDACKN must transition for each byte transferred.

The device downstream from the AHA3710 requests data transfers by asserting CDREQ high. The AHA3710 acknowledges the transfer by driving CDACKN low. Data is transferred out of the CD Port on the rising edge of CDWRN.

When the byte on CD[7:0] is the last byte of a compressed page, the CDEOPN signal is asserted.

Figure 6: Uncompressed Data Input Port Transfer



0255381 0002775 T78

2.4 DMA INPUT PORT FORMAT

The UD Port expects one of three image formats; red-green-blue (RGB), color-by-line (CBL) or grayscale (GS). Graphical representation of each input stream format can be found in Figure 9.

In all formats, the input data stream may contain a header that must pass through the device uncompressed. The header may be from 0 to 255 bytes. The length of the header is programmed by writing the length in bytes to the *Image Header Length* register.

RGB (24 bit) format represents each pixel with three bytes. All three bytes for one pixel are received in order of red, green then blue. Since only a stream of bytes that are the same color may be compressed, the input data stream must be deinterleaved. Deinterleaving is handled automatically by the AHA3710 when RGB is selected as the Color Mode in the *System Configuration* register.

Grayscale format represents each pixel as a single byte. In order to compress a grayscale input stream the Deinterleaver must be disabled. This is done automatically when GS is selected as the Color Mode in the *System Configuration* register.

CBL format represents each pixel with three bytes, however the color planes are separated. This means that an entire line of red bytes will be received before the first green byte is received. Then an entire line of green bytes is received before the first blue byte.

The input data stream may contain a scan offset in CBL mode. This means that several lines of red will be received before receiving a green line. Then several red/green line pairs are received before a blue line is received. The input stream will then alternate between red, green and blue lines.

The reverse happens at the end of a page. Once all the red lines have been received, several green/blue line pairs will be received, and finally the remaining blue lines are received.

The AHA3710 can be programmed to handle scan offset values from zero (no offset) to 255. The scan offset value is programmed by writing the number of lines to offset in the *Scan Offset* register.

2.5 DMA OUTPUT PORT FORMAT

The CD Port output stream has a single format as shown in Figure 10.

During normal operation the AHA3710 prepends a seven byte header to the output stream. The AHA3710 Header format is also shown in Figure 10. After the seven byte header, the AHA3710 outputs the uncompressed Image Header and finally the compressed image.

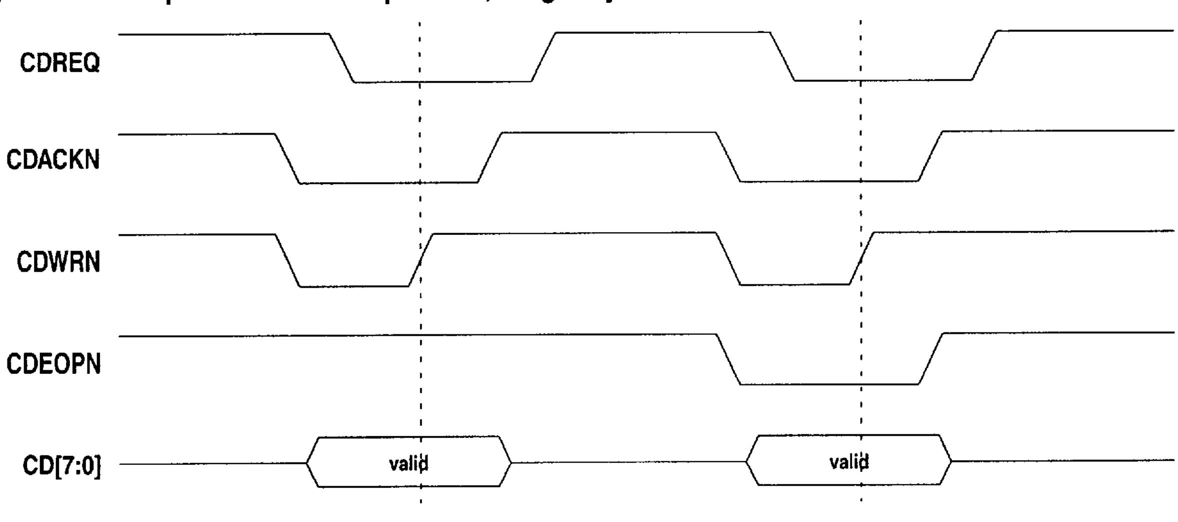
2.6 PASS THROUGH MODE

The AHA3710 supports pass through mode operations allowing data to be transferred directly from the UD port to the CD port. If the AHA3710 has been programmed to be in Pass-Through mode, there is no header prepended to the data. The input stream (on the UD bus) will exactly match the output stream (on the CD bus) bye for byte. This mode effectively makes the AHA3710 transparent to the system data path except for approximately 5 clocks of delay between input and output byte transfers.

In pass through operation asserting the UDEOLN signal will cause the CDEOPN signal to be asserted when the byte flagged by the UDEOLN signal is output from the CD bus (approximately 5 clocks later).

In pass-through mode, the LINE LENGTH and PAGE LENGTH parameters are ignored.

Figure 7: Compressed Data Output Port, Single Byte Transfer



0255381 0002776 904

Figure 8: Compressed Data Output Port, Multi Byte Transfer

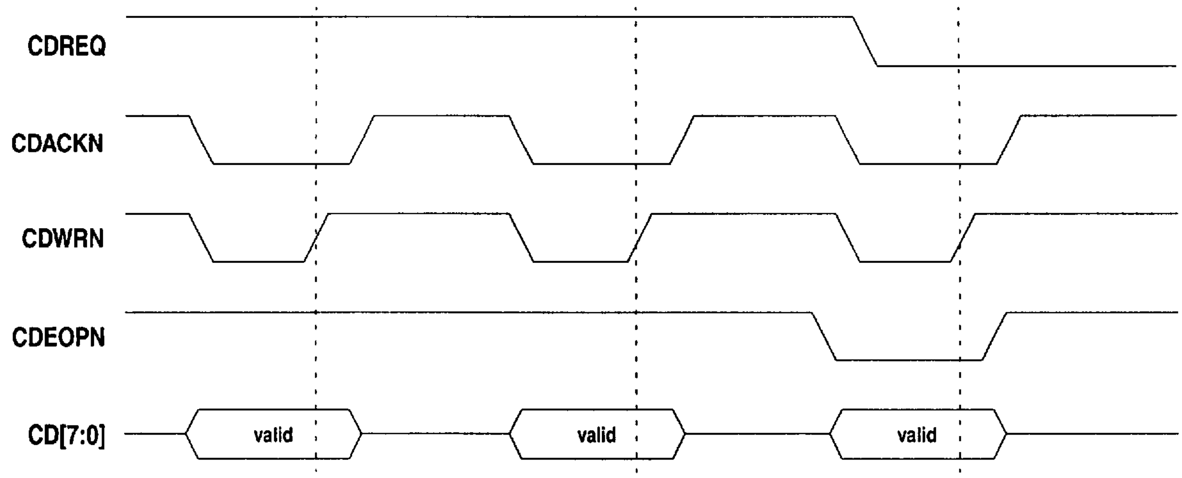


Figure 9: Stream Formats, Uncompressed Data Input Port

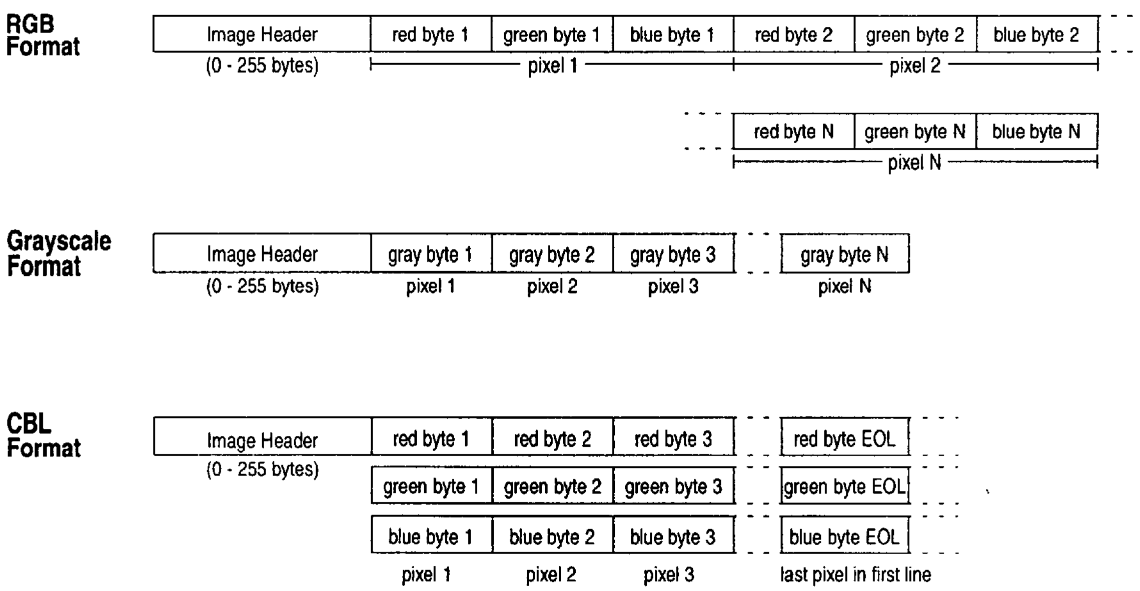
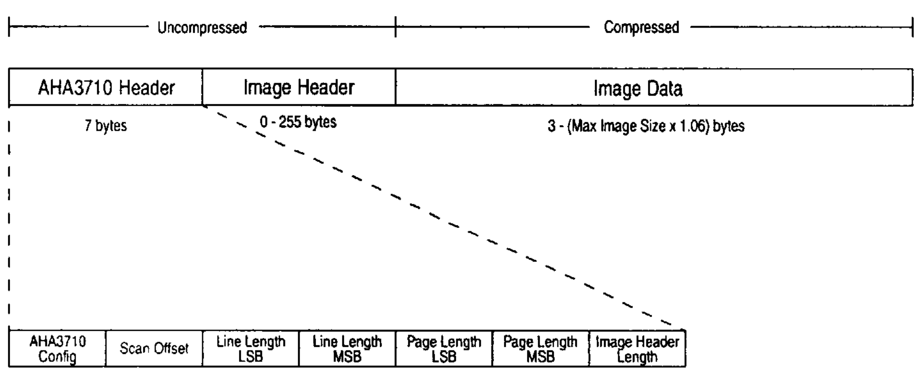


Figure 10: Stream Formats, Compressed Data Output Port



2.7 ALGORITHM

AHA3710 compression is an efficient implementation of an algorithm that has been modified and optimized for color image data. It can also process grayscale formatted image data. The algorithm has an optional lossy mode that will provide higher compression ratios. Software emulation of the algorithm is available for evaluation.

2.8 COMPRESSION ENGINE

The Compression Engine supports either compression or pass-through processes. The mode of operation is selected with the Pass-Through Mode (PTM) bit in the *System Configuration* register. If PTM is set, Pass-Through Mode is selected and data will not be compressed. If PTM is clear, Compression Mode is selected and data will be compressed.

The Compression Engine can compress with or without loss. This is controlled by setting or clearing the LCM bit. With LCM set the image will be compressed with loss. With LCM clear the image will be compressed without loss.

In Lossy Compression Mode the quantization coefficients must be programmed in the *Quantization Coefficient* registers. These coefficients control the amount of loss and the compression ratio.

The Compression Engine is enabled with the *Process Page* command, which is given by writing a one to the PRPG bit in the *Command* register. This command allows the AHA3710 to begin requesting data on the UD Port.

When a *Process Page* command is received in Compression Mode the device will set the PIP bit, output the AHA3710 Header, pass through an Image Header if one exists, clear PIP and set CIP, compress the input data, clear the CIP bit and issue an End-of-Page Interrupt (EOP).

When a *Process Page* command is received in Pass-Through Mode the device will set the PIP bit and pass through every byte it receives. Pass-Through Mode can be exited by writing a zero to the PTM bit in the *System Configuration* register and then issuing a *Soft-Reset* command.

If a microprocessor write occurs to any register other than the *Command, Interrupt Mask* or *Interrupt Status/Control* registers while either PIP or CIP is active, the AHA3710 will issue a Configuration Change Error (CCE) interrupt.

The EMPTY bit indicates that the AHA3710 contains no data. This may be active during compression of a page under certain circumstances when the device is starved for input data. The EMPTY bit should not be used as an indication that the page is complete.

The *Compressed Page Length* register contains the number of bytes that have been transferred out of the CD Port. This count will include the seven byte AHA3710 header and the uncompressed image header. The total compressed byte count for the entire page is valid after an EOP Interrupt is received.

2.9 INTERRUPTS

There are three conditions reported in the *Interrupt Status/Control* register; Peripheral Access Error (PAE), End-of-Page (EOP), and Configuration Change Error (CCE). All interrupts are maskable by setting the corresponding bits in the *Interrupt Mask* register. A one in the *Interrupt Mask* register means the corresponding bit in the *Interrupt Status/Control* register is masked and does not affect the interrupt pin (INTRN). The INTRN pin is active whenever any unmasked interrupt bit is set to a one.

A PAE Interrupt is posted when the microprocessor attempts to perform a read or write to the downstream device connected to the CD Port when the AHA3710 is not paused.

An EOP Interrupt is posted when the last byte in a page is transferred out of the CD Port.

The CCE Interrupt is posted when the microprocessor attempts to perform a write to any of the AHA3710 registers (except *Command, Interrupt Mask* or *Interrupt Status/Control*) while either PIP or CIP bits of the *Status* register are set.

2.10 TEST MODE

In order to facilitate board level testing, the AHA3710 provides the ability to tristate all outputs. This is accomplished by asserting the TEST pin.

0255381 0002778 787

3.0 REGISTER DESCRIPTIONS

The microprocessor configures, controls and monitors IC operation through the use of the registers defined in this section. All registers are reset to zero on RSTN unless otherwise stated. The bits labelled "*res*" are reserved and must be set to zero when writing to registers unless otherwise noted. Reads from registers 0x04 to 0x09 will reflect the programmed values only after a process page (PRPG, addr 0x01) command.

Table 1: Internal Registers

ADDRESS	*R/W*	*DESCRIPTION*	*DEFAULT AFTER RSTN*	*AFTER SOFT RESET*
0x00	R/W	System Configuration	0x00	No Change
0x01	W	Command	N/A	N/A
0x01	R	Status	0x01	0x01
0x02	R/W	Interrupt Mask	0x07	No Change
0x03	R/W	Interrupt Status/Control	0x00	0x00
0x04	R/W	Scan Offset Length	0x00	No Change
0x05	R/W	Image Header Length	0x00	Previous Write
0x06	R/W	Line Length 0	0x00	Previous Write
0x07	R/W	Line Length 1	0x00	Previous Write
0x08	R/W	Page Length 0	0x00	Previous Write
0x09	R/W	Page Length 1	0x00	Previous Write
0x0A	R	Compressed Page Length 0	0x00	0x00
0x0B	R	Compressed Page Length 1	0x00	0x00
0x0C	R	Compressed Page Length 2	0x00	0x00
0x0D	R	Compressed Page Length 3	0x00	0x00
0x0E	R/W	Quantization Coefficient 0	0x00	No Change
0x0F	R/W	Quantization Coefficient 1	0x00	No Change
0x10	R/W	Quantization Coefficient 2	0x00	No Change
0x11	R/W	Quantization Coefficient 3	0x00	No Change
0x12	R/W	Quantization Coefficient 4	0x00	No Change
0x13	R/W	Quantization Coefficient 5	0x00	No Change
0x14	R/W	Quantization Coefficient 6	0x00	No Change
0x15	R/W	Quantization Coefficient 7	0x00	No Change
0x16-0x1E		*Reserved*	Undefined	Undefined
0x1F	R	Version/ID	0x01	0x01

Note: "Previous Write" means the last data from a microprocessor write to this register.

3.1 SYSTEM CONFIGURATION 0, READ/WRITE

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x00	*res*	WAL	AAL	*res*	PTM	LCM	CM[1:0]	

This register is set to 0x00 by reset.

WAL — Write Asserted Length. This bit controls the number of clock cycles that CDWRN is asserted during DMA cycles. If this bit is set, CDWRN will be asserted for two clock cycles. If this bit is clear, CDWRN will be asserted for one clock cycle.

AAL — Acknowledge Asserted Length. This bit controls the number of clock cycles that CDACKN remains asserted after deassertion of CDWRN. If this bit is set, CDACKN will remain asserted for two clock cycles after CDWRN is deasserted. If this bit is clear, CDACKN will remain asserted for one clock cycle after CDWRN is deasserted.

PTM — Pass-Through Mode. When this bit is set, the AHA3710 will not prepend its seven byte header and the Compression Engine will pass data from the UD Port to the CD Port uncompressed. When the bit is clear, the AHA3710 will prepend the seven byte header and the Compression Engine will compress data.

LCM — Lossy Compression Mode. When this bit is set, the system will compress with loss of image quality. When the bit is clear the system will compress without loss.

CM[1:0] — Color Mode. These bits define the input data stream format: 00 = Grayscale, 01 = *Undefined*, 10 = RGB, 11 = CBL.

3.2 COMMAND, WRITE

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x01	*res*				UNPAUSE	PAUSE	PRPG	SOFTRST

This register is write only.

UNPAUSE — Unpause the AHA3710. When a 1 is written to this bit the AHA3710 will resume requesting data by asserting UDREQ and acknowledging requests for data with CDACKN. Writing a 0 to this bit has no effect.

PAUSE — Pause the AHA3710. When a 1 is written to this bit the AHA3710 will complete the current DMA transfer on the CD Port. The CD Port will not acknowledge future requests for data during Paused Mode. If the AHA3710 is requesting data on the UD Port, that transfer will complete, but further requests will not be made. It is possible that the current transfer on the UD Port may never complete if the upstream device does not acknowledge the current request. Writing a 0 to this bit has no effect.

PRPG — Process Page. Writing a 1 to this bit causes the system to begin requesting data with UDREQ on the UD Port. The input data is processed according to the configuration in the *System Configuration* register. Writing a 0 to this bit has no effect.

SOFTRST — Soft Reset. When a 1 is written to this bit the Compression Engine, UD Port and CD Port are reset to the same condition that a hard reset would cause. Any image data in the AHA3710 is lost. Any pending interrupts are cleared, however the *Interrupt Mask* register is not changed. The *Scan Offset, Image Header Length, Line Length,* and *Page Length* registers are reloaded with the previously programmed values, reflecting that no data has been processed. The *Compressed Page Length* registers are reset to 0x00. The *System Configuration* and *Quantization Coefficients* registers will remain unchanged. The *Status* register will be reset to 0x01. The reset will take 4 clock cycles to complete. Writing a 0 to this bit has no effect.

0255381 0002780 335

3.3 STATUS, READ

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x01	res			PIP	CIP	UDPP	CDPP	EMPTY

This register is set to 0x01 by reset.

Note: CIP and PIP will NEVER be active at the same time.

PIP Pass-Through In Progress. When this bit is set, the Compression Engine is passing uncompressed data from the UD Port to the CD Port uncompressed. This may be the result of either the PTM bit being set in the *System Configuration* register or the *Image Header Length* register having any value greater than 0x00. When both PIP and CIP are clear it indicates that the AHA3710 is idle. The AHA3710 is idle after reset or EOP interrupt, and before the next PRPG command.

CIP Compression In Progress. When this bit is set, the Compression Engine has begun compressing the input image data. When both PIP and CIP are clear it indicates that the AHA3710 is idle. The AHA3710 is idle after reset or EOP interrupt, and before the next PRPG command.

CDPP CD Port Paused. When this bit is set, it indicates that the CD Port is paused and the device will not assert CDACKN. It also indicates that the Peripheral Access Mode may be used.

UDPP UD Port Paused. When this bit is set, it indicates that the UD Port is paused and the device will not assert UDREQ. This bit may not set after a PAUSE command since the AHA3710 is dependent on the upstream device to complete the current DMA transfer. This bit has no bearing on Peripheral Access Mode.

EMPTY AHA3710 Empty. When this bit is set, it indicates that the AHA3710 contains no data. When the bit is clear, it indicates that there is at least one byte of data in the device.

3.4 INTERRUPT MASK, READ/WRITE

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x02	*res*					PAEM	CCEM	EOPM

This register is set to 0x07 by reset.

PAEM Peripheral Access Error Mask. When this bit is set, it prevents the INTRN pin from becoming active due to an PAE Interrupt. The interrupt will still be posted in the *Interrupt Status/Control* register. When the bit is clear, it allows the INTRN pin to become active when an PAE Interrupt occurs.

CCEM Configuration Change Error Mask. When this bit is set, it prevents the INTRN pin from becoming active due to an CCE Interrupt. The interrupt will still be posted in the *Interrupt Status/Control* register. When the bit is clear, it allows the INTRN pin to become active when an CCE Interrupt occurs.

EOPM End-of-Page Interrupt Mask. When this bit is set, it prevents the INTRN pin from becoming active due to an EOP Interrupt. The interrupt will still be posted in the *Interrupt Status/Control* register. When the bit is clear, it allows the INTRN pin to become active when an EOP Interrupt occurs.

0255381 0002781 271

3.5 INTERRUPT STATUS/CONTROL, READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x03			*res*			PAE	CCE	EOP

This register is set to 0x00 by reset.

PAE Peripheral Access Error Interrupt. When this bit is set, it indicates that a peripheral read or write access was attempted while the CD Port of the AHA3710 was not paused. This will occur any time the PCSN pin is asserted while the CDPP bit is not set. The PAE Interrupt is cleared by writing a one to this bit.

CCE Configuration Change Error Interrupt. When this bit is set, it indicates that a write to a configuration register occurred before the current page was completely processed and that the page may have been corrupted. Writing to any AHA3710 register (except *Command, Interrupt Mask* and *Interrupt Status/Control*) while PIP or CIP are active will cause this interrupt. The CCE Interrupt is cleared by writing a one to this bit.

EOP End-of-Page Interrupt. When this bit is set, it indicates that an End-of-Page byte has been strobed out of the CD Port. The EOP Interrupt is cleared by writing a one to this bit.

3.6 SCAN OFFSET, READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x04				SO[7:0]				

This register is set to 0x00 by reset.

Note: A read from this register reflects the programmed values only after a process page (PRPG) command.

SO[7:0] Scan Offset. This register is written with the number of lines that each color plane is offset in CBL mode. This register has no effect in RGB or GS Modes. Writing 0x00 to this register will imply that the first red line will be immediately followed by the first green line. Writing 0x01 to this register will imply that two red lines will be received before the first green line.

3.7 IMAGE HEADER LENGTH, READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x05				IHL[7:0]				

This registers are set to 0x00 by reset.

Note: A read from this register reflects the programmed values only after a process page (PRPG) command.

IHL[7:0] Image Header Length. This register is written with the size in bytes of the Image Header that prefixes the input image. The value written will be the number of bytes that are passed through uncompressed. Writing 0x00 to this register implies that there is no Image Header. Reading this register gives a count of the bytes remaining to be passed through before image compression begins.

0255381 0002782 108

3.8 LINE LENGTH, READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x06	LL[7:0]							
0x07	LL[15:8]							

These registers are initialized to 0x00 after reset.

Note: *A read from this register reflects the programmed values only after a process page (PRPG) command.*

Note: *Reads from multi-byte registers are only valid after an EOP Interrupt.*
These registers will also be valid if the UD Port is paused.

LL[15:0] Line Length. This register is written with the length of a line in **bytes**. Reading this register gives a count of the number of bytes remaining to be input from the current line. For CBL and GS modes the number of bytes is equal to the number of pixels in the line. For RGB mode the number of bytes is 3 times the number of pixels.

3.9 PAGE LENGTH, READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x08	PL[7:0]							
0x09	PL[15:8]							

These registers are initialized to 0x00 after reset.

Note: *Reads from multi-byte registers are only valid after an EOP Interrupt.*
These registers will also be valid if the UD Port is paused.

Note: *A read from this register reflects the programmed values only after a process page (PRPG) command.*

PL[15:0] Page Length. This register is written with the length of the page in ***lines***. Reading this register gives a count of the number of lines remaining to be input from the current image. For CBL mode this register must be programmed to be 3 times the actual number of lines on the page.

3.10 COMPRESSED PAGE LENGTH, READ ONLY

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0A	CPL[7:0]							
0x0B	CPL[15:8]							
0x0C	CPL[23:16]							
0x0D	CPL[31:24]							

These registers are initialized to 0x00 after reset.

Note: *Reads from multi-byte registers are only valid after an EOP Interrupt.*
These registers will also be valid if the CD Port is paused.

CPL[31:0] CompressedPage Length. Reading this register gives a count of the number of bytes that have been strobed out of the CD Port, regardless of compression mode. The count will include the AHA3710 Header and the uncompressed Image Header. These registers are reset 0x00 by the PRPG command.

3.11 QUANTIZATION COEFFICIENTS, READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0E			*res*				QC0[2:0]	
0x0F			*res*				QC1[2:0]	
0x10			*res*				QC2[2:0]	
0x11			*res*				QC3[2:0]	
0x12			*res*				QC4[2:0]	
0x13			*res*				QC5[2:0]	
0x14			*res*				QC6[2:0]	
0x15			*res*				QC7[2:0]	

These registers are initialized to 0x00 after reset.

QCx[2:0] Quantization Coefficients. These registers are programmed with the lossy compression mode quantization limits. The coefficients can be in the range of 0x00 to 0x04. Any value out of range will result in unpredictable operation. The coefficients affect image quality and compression ratio. Larger coefficients generally result in higher compression ratio but poorer image quality. Smaller coefficients generally result in lower compression ratio and improved image quality. These registers may be read at any time. Writes may only occur when both the PIP and CIP bits of the *Status* register are clear. Contact AHA Applications Engineering for more information on programming these registers or consult the AHA3710 Designers Guide.

3.12 VERSION ID, READ ONLY

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x1F				VERSION[7:0]				

This register is initialized to 0x01 after reset.

VERSION[7:0] Contains version number of the die.

4.0 SIGNAL DESCRIPTIONS

This section contains descriptions for all the pins. Each signal has a type code associated with it. The type codes are described in the following table.

TYPE CODE	DESCRIPTION
I	Input only pin
O	Output only pin
I/O	Input/Output pin
S	Synchronous signal
A	Asynchronous signal

4.1 MICROPROCESSOR INTERFACE

MICROPROCESSOR INTERFACE			
SIGNAL	TYPE	RESET STATE	DESCRIPTION
AD[7:0]	I/O A/S	Z	Multiplexed Processor Address and Data. All microprocessor reads and writes to the AHA3710 are performed on this bus. Address is asynchronously latched into the AHA3710 by ALN. Data is synchronously registered on the rising edge of CLK when CSN and WRN are active.
CSN	I S	N/A	Chip Select. Selects the AHA3710 as the source or destination of the current microprocessor bus cycle. CSN must be active for the duration of the bus cycle. CSN may remain low continuously during back to back register access cycles.
PCSN	I S	N/A	Peripheral Chip Select. Selects the peripheral device connected to the CD Port as the source or destination of the current microprocessor bus cycle. ***PCSN may only be asserted if the AHA3710 is paused.*** PCSN must be active for the duration of the bus cycle. PCSN may remain low continuously during back to back register access cycles.
ALN	I A	N/A	Address Latch. The microprocessor read/write address is latched by the AHA3710 on the falling edge of this signal. ALN must remain low for the duration of the bus cycle.
RDN	I S	N/A	Read strobe. The combination of CSN low and RDN low initiates a register read from the address previously latched by ALN. The read cycle begins when both CSN and RDN are low, and the setup time to the rising edge of CLK has been met. Read data will appear on the AD[7:0] port during the third clock cycle after RDN goes low. The bus cycle is terminated when a low to high transition on either CSN or RDN meets the required setup time to CLK. During normal operation RDN and WRN should NEVER be active at the same time.
WRN	I S	N/A	Write strobe. The combination of CSN low and WRN low initiates a register write to the address previously latched by ALN. The write cycle begins when both CSN and WRN are low, and the setup time to the rising edge of CLK has been met. The bus cycle is terminated when a low to high transition on either CSN or WRN meets the required setup time to CLK. During normal operation WRN and RDN should NEVER be active at the same time.
INTRN	O S	1	Interrupt. The interrupts (that are not masked) in the *Interrupt Status/Control* register are reported to the microprocessor with this signal.

0255381 0002785 917

4.2 DMA INPUT PORT INTERFACE

UNCOMPRESSED DATA PORT			
SIGNAL	***TYPE***	***RESET STATE***	***DESCRIPTION***
UDREQ	O A	0	Uncompressed Data Request. Active high output indicating that the AHA3710 is requesting data on UD[7:0].
UDACKN	I A	N/A	Uncompressed Data Acknowledge. Active low input indicating the transfer of a byte on UD[7:0].
UDWRN	I A	N/A	Uncompressed Data Write. Active low write strobe. The rising edge of UDWRN is used to latch data into the AHA3710.
UD[7:0]	I A	N/A	Uncompressed Data. The value on this input bus is latched into the AHA3710 on the rising edge of UDWRN.
UDEOLN	I A	N/A	Uncompressed Data End of Line. Active low input indicating that the byte on UD[7:0] is the last byte in a line.

4.3 DMA OUTPUT PORT INTERFACE

COMPRESSED DATA PORT			
SIGNAL	***TYPE***	***RESET STATE***	***DESCRIPTION***
CDREQ	I A	N/A	Compressed Data Request. Active high input indicating that the downstream device is requesting data on CD[7:0]. CDREQ may remain active for consecutive bytes. In Peripheral Access mode, this signal is ignored.
CDACKN	O S	1	Compressed Data Acknowledge. Active low output indicating that the AHA3710 is transferring a byte to the downstream device on CD[7:0]. CDACKN will transition for each byte of data. In Peripheral Access mode, CDACKN will remain high.
CDWRN	O S	1	Compressed Data Write. Active low write strobe. The rising edge of CDWRN should be used to latch CD[7:0] into the downstream device. CDWRN will transition for each byte of data. In Peripheral Access mode, CDWRN will follow the microprocessor write strobe (WRN).
CD[7:0]	I/O S	Z	Compressed Output Data. During normal operation CD[7:0] is being driven whenever CDACKN is low, otherwise it is tristated. CD[7:0] is valid on the rising edge of CDWRN. In Peripheral Access Mode, the direction of CD[7:0] is determined by the microprocessor read and write strobes. When PCSN and RDN are active, this bus is an input. When PCSN and WRN are active this bus is an output.
CDEOPN	O S	1	Compressed Data End-of-Page. Active low output indicating that the byte on CD[7:0] is the last byte in a page. CDEOPN is *NOT* tristated when CDACKN is high or during Peripheral Access.

4.4 SYSTEM CONTROL

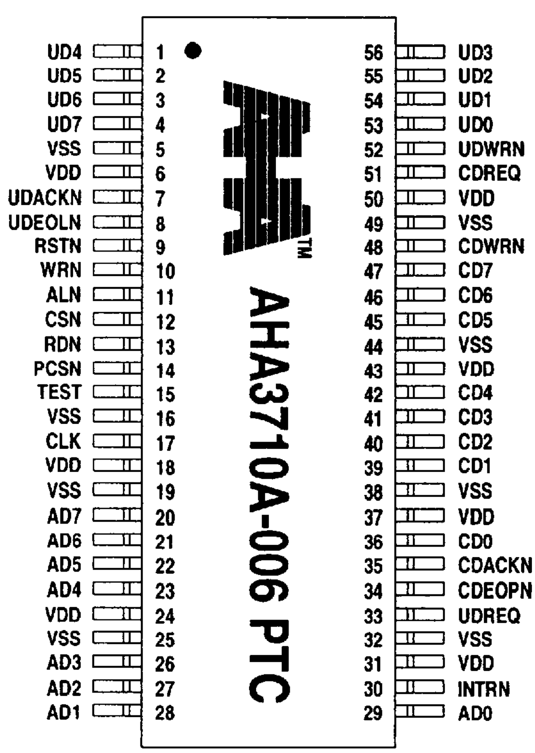
SYSTEM CONTROL			
SIGNAL	***TYPE***	***RESET STATE***	***DESCRIPTION***
CLK	I	N/A	System Clock.
RSTN	I A	N/A	Power on Reset. Active low reset signal. The AHA3710 must be reset before any microprocessor activity is attempted. RSTN should be active for a minimum of 4 CLK periods.
TEST	I A	N/A	Board Test mode. When TEST is high, all outputs are tristated. When TEST is low, the chip performs normally.

5.0 PINOUT

PIN	SIGNAL
1	UD4
2	UD5
3	UD6
4	UD7
5	VSS
6	VDD
7	UDACKN
8	UDEOLN
9	RSTN
10	WRN
11	ALN
12	CSN
13	RDN
14	PCSN
15	TEST
16	VSS
17	CLK
18	VDD
19	VSS
20	AD7
21	AD6
22	AD5
23	AD4
24	VDD
25	VSS
26	AD3
27	AD2
28	AD1

PIN	SIGNAL
29	AD0
30	INTRN
31	VDD
32	VSS
33	UDREQ
34	CDEOPN
35	CDACKN
36	CD0
37	VDD
38	VSS
39	CD1
40	CD2
41	CD3
42	CD4
43	VDD
44	VSS
45	CD5
46	CD6
47	CD7
48	CDWRN
49	VSS
50	VDD
51	CDREQ
52	UDWRN
53	UD0
54	UD1
55	UD2
56	UD3

Figure 11: Pinout



0255381 0002787 79T

6.0 ELECTRICAL SPECIFICATIONS

Information in this section represents design goals. While every effort will be made to meet these goals, values presented should be considered targets until characterization is complete. Please consult with Advanced Hardware Architectures for the most up-to-date values.

6.1 DC CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input low voltage		0.8	V	
V_{IH}	Input high voltage	2.0		V	
I_{IN}	Input leakage current		10	uA	
V_{OL}	Output low voltage (I_{OL}=-2mA)		0.4	V	
V_{OH}	Output high voltage (I_{OH}=2mA)	2.4		V	
I_{OL}	Output low current		2	mA	
I_{OH}	Output high current		2	mA	
I_{OZ}	Output leakage current during tristate		10	uA	
I_{DD}	Supply current (static)		10	µA	1

Notes:
1) *All inputs driven to 5.25V, I_{LOAD} = 0mA.*

6.2 ABSOLUTE MAXIMUM STRESS RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_{STG}	Storage temperature	-50	150	°C	
V_{DD}	Supply voltage	-0.5	7	V	
V_{IN}	Input voltage	V_{SS}-0.5	V_{DD}+0.5	V	

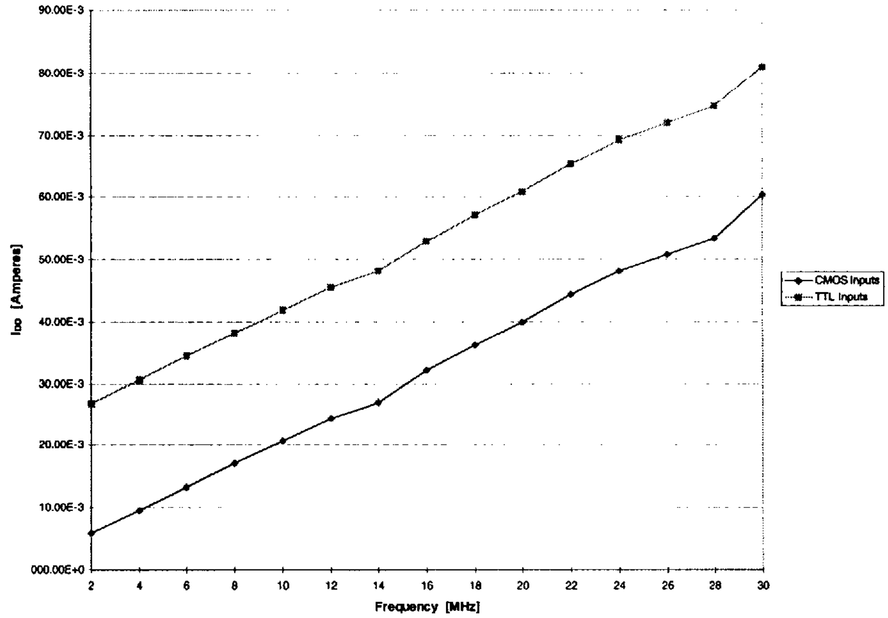
6.3 AC CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{DD}	Supply voltage	4.75	5.25	V	
I_{DD}	Supply current (active) TTL Inputs		95	mA	1
I_{DD}	Supply current (active) CMOS Inputs		70	mA	2
T_A	Ambient Temperature	0	70	°C	

Notes:
1) *f = 30 MHz, C_L = 50 pF, V_{IL} = 0.4V, V_{IH} = 2.4V*
2) *f = 30 MHz, C_L = 50 pF, V_{IL} = 0.1V, V_{IH} = 5.0V*

0255381 0002788 626

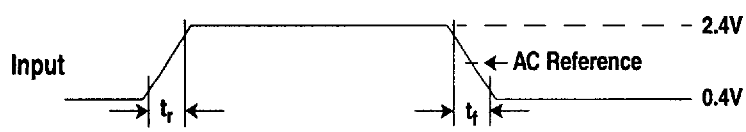
Figure 12: Average Idd



6.4 TEST CONDITIONS

PARAMETER	*VALUE*	*UNITS*
Output Load Capacitance, C_L	50	pF
AC Timing Reference	1.4	V

Figure 13: Input Waveforms



Notes:
1) $t_r \leq 2$ ns, $t_f \leq 2$ ns.

6.5 PIN CAPACITANCE

SYMBOL	*PARAMETER*	*MIN*	*MAX*	*UNITS*
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		10	pF
C_{IO}	I/O Capacitance		10	pF

6.6 TIMING SPECIFICATIONS

Notes:

1) Production test condition is 50 pF.

2) All timings are referenced to 1.4 volts.

Figure 14: Uncompressed Data Input Port Timing

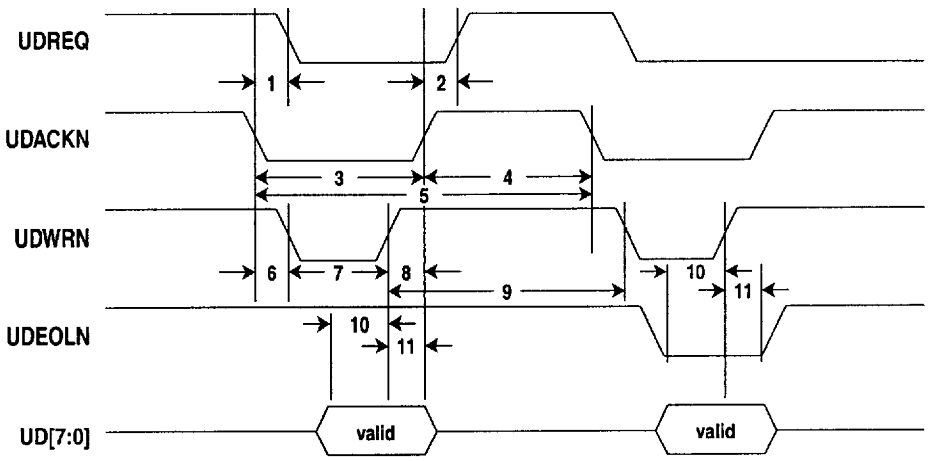


Table 2: Uncompressed Data Input Port Timing Requirements

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*	*NOTES*
1	UDACKN low to UDREQ low	0	30	ns	
2	UDACKN high to UDREQ high	0		ns	
3	UDACKN low pulse width	Tcp+10 ns		ns	2
4	UDACKN high pulse width	Tcp+10 ns		ns	2
5	UDACKN period	5		clocks	
6	UDACKN low to UDWRN low	0		ns	1
7	UDWRN low pulse width	Tcp+10 ns		ns	1, 2
8	UDWRN high to UDACKN high	0		ns	1
9	UDWRN high pulse width	Tcp+10 ns		ns	2
10	UD[7:0]/UDEOLN setup to UDWRN rising edge	15		ns	
11	UD[7:0]/UDEOLN hold from UDWRN rising edge	7		ns	

Notes:

1) UDWRN edges may precede or follow UDACKN edges. If UDWRN is held low or the rising edge follows UDACKN rising edge, then the data setup and hold times (11 and 12) must be referenced to UDACKN rising edge.

2) Tcp = clock period.

0255381 0002790 284

Figure 15: Compressed Data Output Port Timing

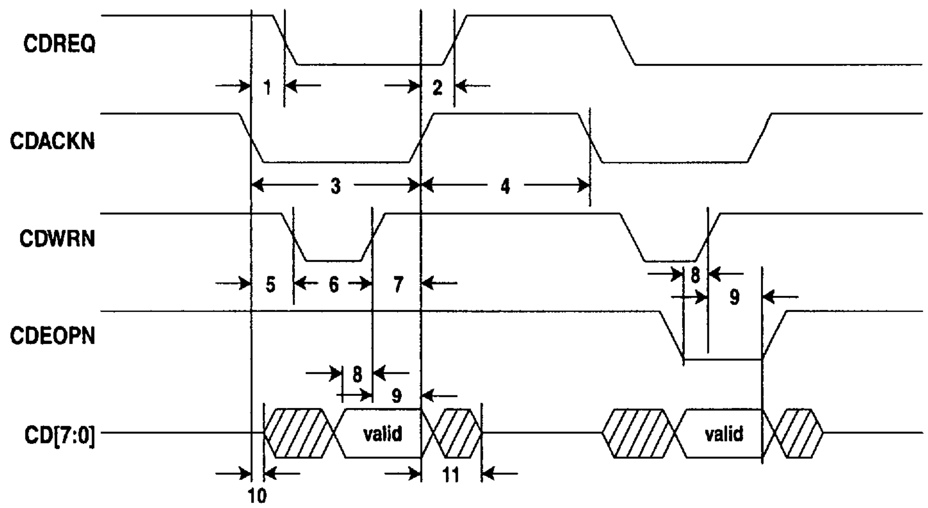


Table 3: Compressed Data Output Port Timing Requirements

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*	*NOTES*
1	CDACKN low to CDREQ low	0	34	ns	1,2
2	CDACKN high to CDREQ high	0	Tcp	ns	3,4
3	CDACKN low pulse width (WAL=0, AAL=0)	2 Tcp–8ns		ns	4
3	CDACKN low pulse width (WAL=0, AAL=1)	3 Tcp–8ns		ns	4
3	CDACKN low pulse width (WAL=1, AAL=0)	3 Tcp–8ns		ns	4
3	CDACKN low pulse width (WAL=1, AAL=1)	4 Tcp–8ns		ns	4
4	CDACKN high pulse width	3 Tcp–5ns		ns	4
5	CDACKN low to CDWRN low	–5	5	ns	
6	CDWRN low pulse width (WAL=0)	Tcp–8ns		ns	4
6	CDWRN low pulse width (WAL=1)	2 Tcp–8ns		ns	4
7	CDWRN high to CDACKN high (AAL=0)	Tcp–7ns	Tcp+7ns	ns	4
7	CDWRN high to CDACKN high (AAL=1)	2 Tcp–7ns	2 Tcp+7ns	ns	4
8	CD[7:0]/CDEOPN valid to CDWRN rising edge	15		ns	
9	CDWRN rising edge to CD[7:0] invalid (AAL=0)	Tcp–5ns	Tcp+5ns	ns	4
9	CDWRN rising edge to CD[7:0] invalid (AAL=1)	2 Tcp–5ns	2 Tcp+5ns	ns	4
9	CDWRN rising edge to CDEOPN invalid (AAL=0)	Tcp–5ns	Tcp+5ns	ns	4
9	CDWRN rising edge to CDEOPN invalid (AAL=1)	2 Tcp–5ns	2 Tcp+5ns	ns	4
10	CDACKN falling edge to CD[7:0] driven	–7		ns	
11	CDACKN rising edge to CD[7:0] tristate		15	ns	

Notes:
1) *CDREQ may remain active for multiple bytes.*
2) *When CDREQ is deasserted, it must meet this time or another byte may be transferred.*
3) *If Tcp is not met, maximum throughput will not be maintained.*
4) *Tcp = clock period.*

Figure 16: Microprocessor Interface Timing (Write)

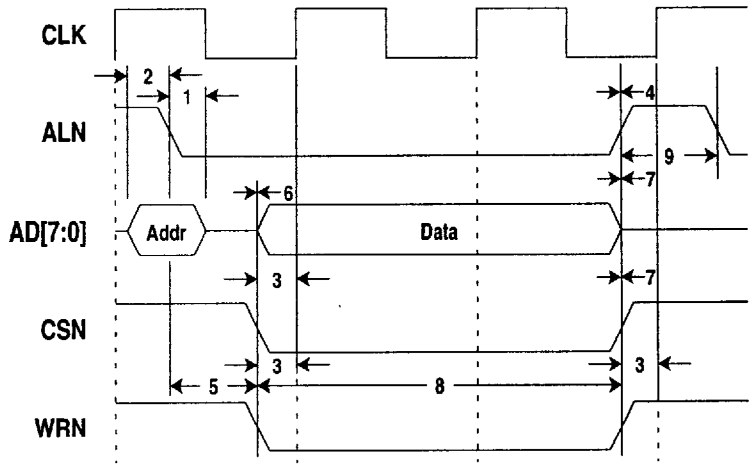


Table 4: Microprocessor Interface Timing Requirements - Write

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	Address hold from ALN falling edge	10		ns	
2	Address setup to ALN falling edge	7		ns	
3	CSN/WRN setup to CLK rising edge	10		ns	4
4	ALN hold from WRN rising edge	0		ns	
5	ALN setup to WRN falling edge	10		ns	
6	Write data setup to WRN falling edge	0		ns	
7	AD[7:0] and CSN hold from WRN rising edge	0		ns	
8	WRN low width	2		clocks	
9	ALN high width	30		ns	

Notes:

1) *Write cycle begins when both CSN and WRN are low and meet setup to rising edge of CLK.*
2) *CSN may be held low continuously for back to back accesses.*
3) *Neither RDN nor WRN may pulse high or low for less than one clock period.*
4) *Only required to be recognized on current clock edge. If less than this number, cycle will be recognized on the next clock.*
5) *CSN must go low prior to WRN going low to begin a Write cycle.*

0255381 0002792 057

Figure 17: Microprocessor Interface Timing (Read)

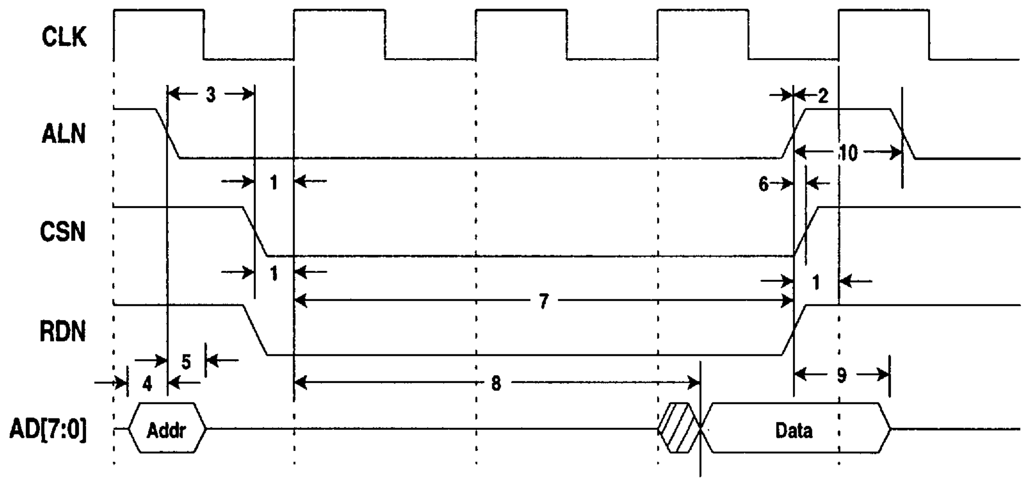


Table 5: Microprocessor Interface Timing Requirements - Read

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*	*NOTES*
1	CSN/RDN setup to CLK rising edge	10		ns	
2	ALN hold from RDN rising edge	0		ns	
3	ALN setup to RDN falling edge	10		ns	
4	Address setup to ALN falling edge	7		ns	
5	Address hold from ALN falling edge	10		ns	
6	CSN hold from RDN rising edge	0		ns	
7	RDN hold from CLK	2 Tcp+20 ns			
8	CLK to read data valid		2 Tcp+20 ns		
9	Rising edge of RDN or CSN to AD high-Z		20	ns	
10	ALN high width	30		ns	

Notes:

1) *Read cycle begins when both CSN and RDN are low and meet setup to rising edge of CLK.*
2) *CSN may be held low continuously for back to back accesses.*
3) *Neither RDN nor WRN may pulse high or low for less than one CLK period.*
4) *Tcp = clock period.*
5) *CSN must go low prior to RDN going low to begin a Read cycle.*

0255381 0002793 T93

Figure 18: Peripheral Access Timing (Write)

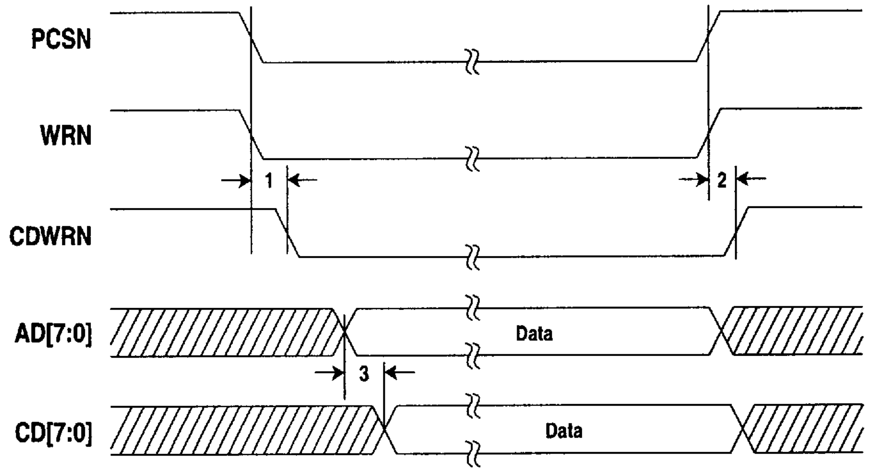


Table 6: Peripheral Access Timing Requirements - Write

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	PCSN and WRN falling edge to CDWRN falling edge	0	25	ns	
2	PCSN or WRN rising edge to CDWRN rising edge	0	25	ns	
3	AD[7:0] delay to CD[7:0]	0	25	ns	

Notes:

1) If AHA3710 is paused, CD[7:0] is only tristated when PCSN and RDN are active.

Figure 19: Peripheral Access Timing (Read)

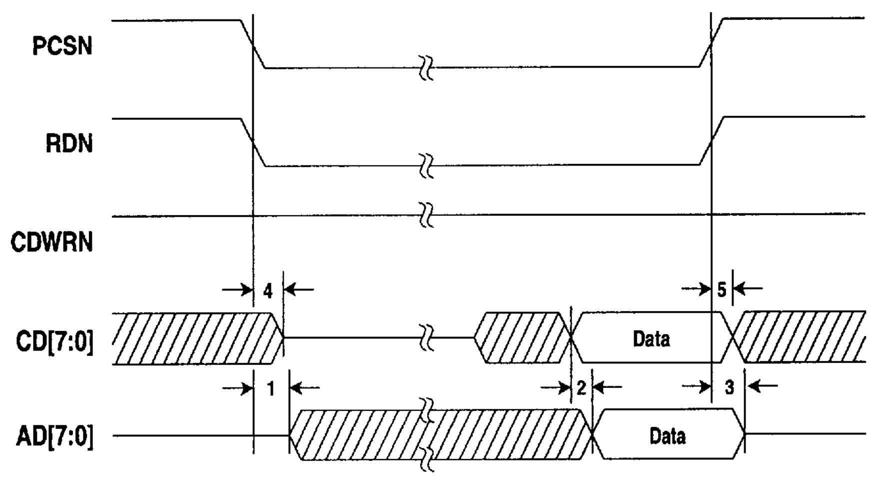


Table 7: Peripheral Access Timing Requirements - Read

NUMBER	PARAMETER	MIN	MAX	UNITS
1	PCSN and RDN falling edge to AD[7:0] driven	0	25	ns
2	CD[7:0] delay to AD[7:0]	0	25	ns
3	PCSN or RDN rising edge to AD[7:0] tristate	0	25	ns
4	PCSN and RDN falling edge to CD[7:0] tristate	0	25	ns
5	PCSN or RDN rising edge to CD[7:0] driven	0	25	

0255381 0002794 92T

Figure 20: Interrupt Timing

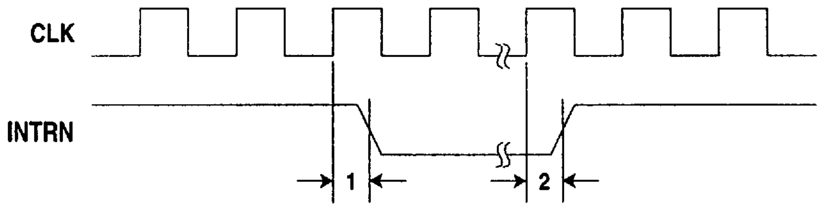


Table 8: Interrupt Timing Requirements

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*
1	INTRN delay time		20	ns
2	INTRN hold time	3		ns

Figure 21: Clock Timing

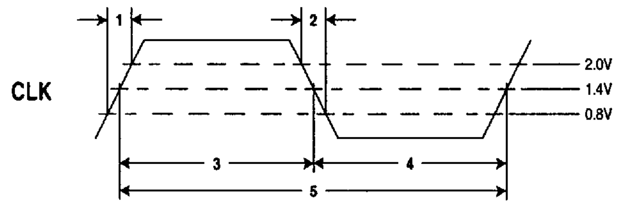


Table 9: Clock Timing Requirements

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*
1	CLK rise time		2	ns
2	CLK fall time		2	ns
3	CLK high time	12		ns
4	CLK low time	12		ns
5	CLK period (Tcp)	33		ns

Figure 22: Power On Reset Timing

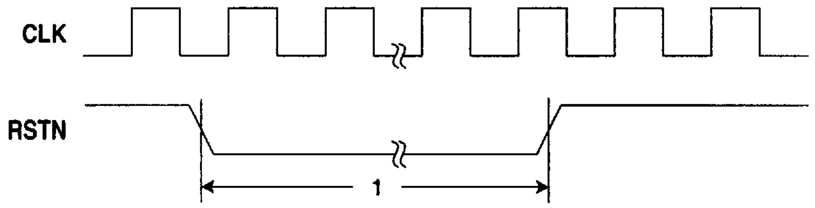


Table 10: Power On Reset Timing Requirements

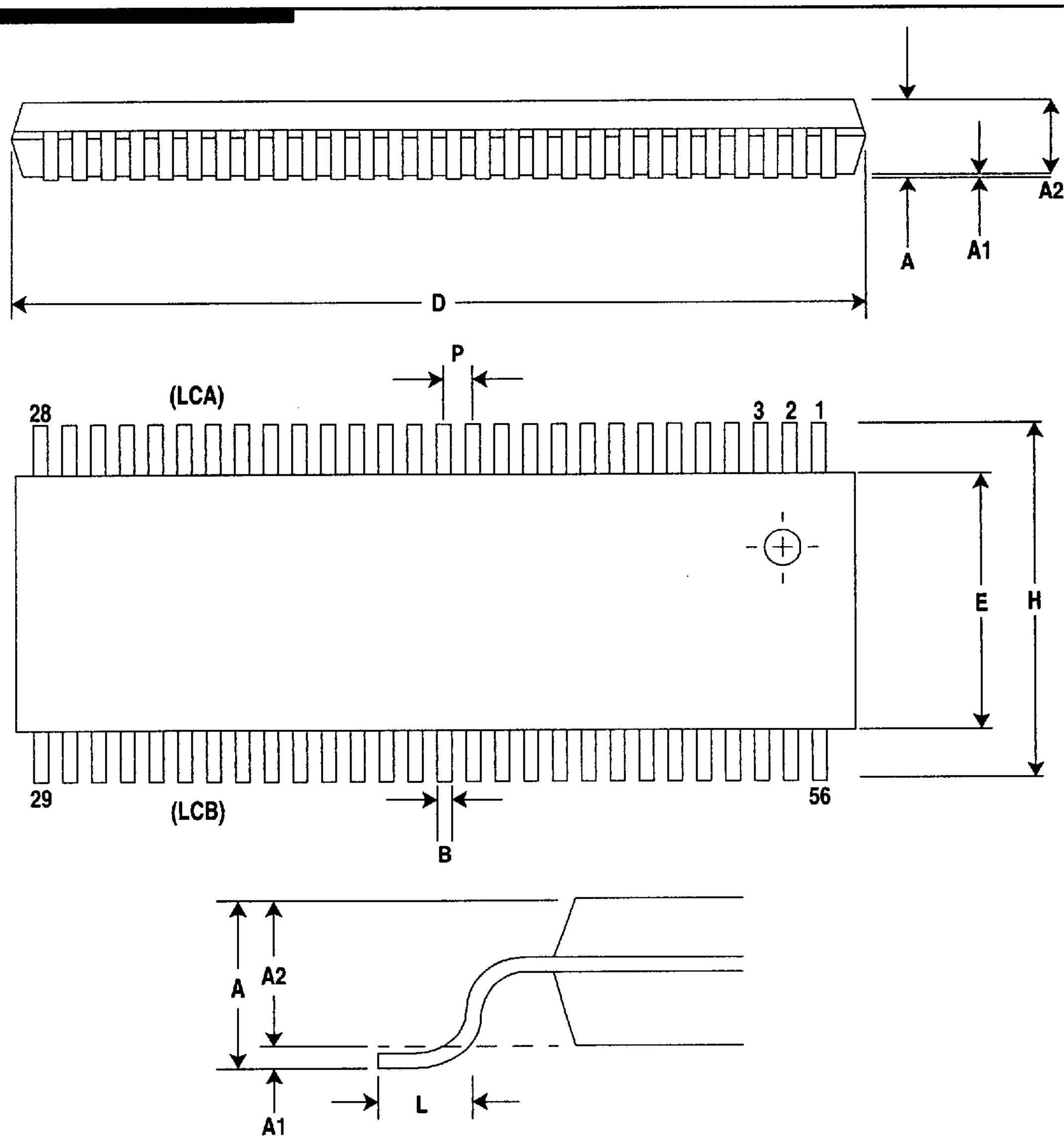
NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*
1	RSTN low pulsewidth	8		clocks

Notes:

1) RSTN signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK.

0255381 0002795 866

7.0 PACKAGE SPECIFICATIONS



PLASTIC TSSOP PACKAGE DIMENSIONS

SYMBOL	*NUMBER OF PIN AND SPECIFICATION DIMENSION*		
	56		
	MIN	NOM	MAX
(LCA)	28		
(LCB)	28		
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
D		14.00	
E	6.00	6.10	6.20
H	8.10 BSC		
L	0.50	0.60	0.75
P	0.50 BSC		
B	0.17		0.27

All dimensions in millimeters (mm)

8.0 ORDERING INFORMATION

8.1 AVAILABLE PARTS

PART NUMBER	DESCRIPTION
AHA3710A-006 PTC	6.0 MBytes/sec Compression Coprocessor

8.2 PART NUMBERING

AHA	3710	A-	006	P	T	C
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:
3710

Revision Letter:
A

Speed Designation:
006 6.0 MB/s

Package Material Codes:
P Plastic

Package Type Codes:
T TSSOP

Test Specifications:
C Commercial 0°C to +70°C

9.0 RELATED TECHNICAL PUBLICATIONS

DOCUMENT #	DESCRIPTION
PB3710	AHA Product Brief – AHA3710 6 MBytes/sec Color Image Compression IC
ANDC20	AHA Application Note – AHA3710 Designer's Guide
ANDC21	AHA Application Note – AHA3710 Compression Performance
ANDC22	AHA Application Note – Operating the AHA3710 Without a Microprocessor
CADCEVAL	CADC™ Evaluation Software (Windows®95)