

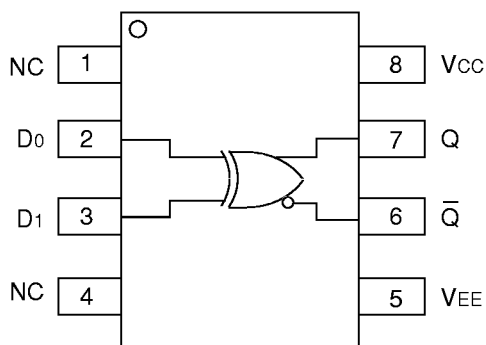
FEATURES

- 260ps propagation delay
- High bandwidth output transitions
- Internal 75K Ω input pull-down resistors
- ESD protection of 2000V
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100EL07 are 2-input XOR/XNOR gates. These devices are functionally equivalent to the E107 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E107, the EL07 is ideally suited for those applications which require the ultimate in AC performance.

PIN CONFIGURATION/BLOCK DIAGRAM



**SOIC
TOP VIEW**

PIN NAMES

Pin	Function
D0, D1	Data Inputs
Q	Data Outputs

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	14	17	11	14	17	11	14	17	11	14	17	
	100EL	—	14	17	11	14	17	11	14	17	13	16	20	
VEE	Power Supply Voltage													V
	10EL	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	
	100EL	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	
IIH	Input HIGH Current													μA
	D0	—	—	250	—	—	250	—	—	250	—	—	250	
	D1	—	—	150	—	—	150	—	—	150	—	—	150	

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
tPLH tPHL	Propagation Delay to Output D	90	250	435	140	250	385	150	260	395	170	280	415	ps
tr tf	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

PRODUCT ORDERING CODE

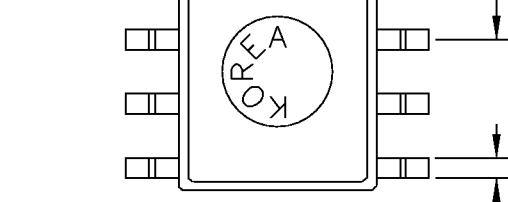
Ordering Code	Package Type	Operating Range
SY10EL07ZC	Z8-1	Commercial
SY10EL07ZCTR	Z8-1	Commercial
SY100EL07ZC	Z8-1	Commercial
SY100EL07ZCTR	Z8-1	Commercial

8 LEAD PLASTIC SOIC (Z8-1)

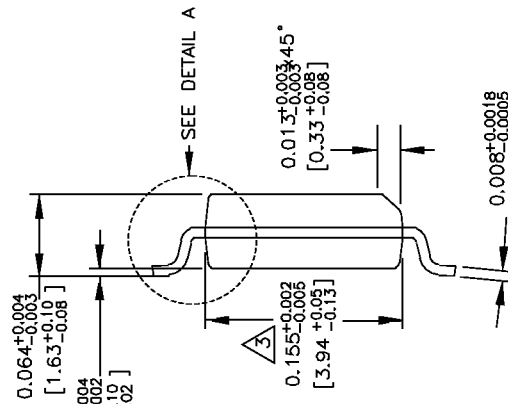
FILE/REV #: PD0032A03
PD/0032/ASCORP
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REV.	REVISION DESCRIPTION	DATE
00	NEW OUTLINE DRAWING.	01/20/94
01	CONVERT TO AUTOCAD. REFERENCE AMKOR DWG. NO. 00019 REVOS. MAKE @ SAME AS JEDEC.	12/14/96
02	ADDED LEAD WIDTH AND PITCH DIMENSIONS. CORRECTED TYPOS.	03/12/97
03	CONVERT DWG TO REL.13 AND ONE PAGE DOCUMENT.	02/20/98

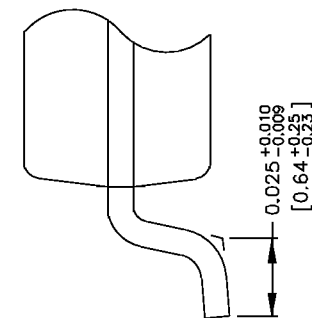
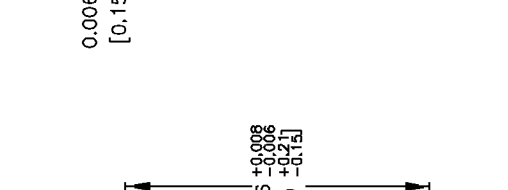
TOP VIEW



END VIEW



BOTTOM VIEW



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

SYNERGY
SEMICONDUCTOR

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APPROVALS	DATE	APPROVALS	DATE
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO	
RELEASE DATE:			

SIZE: A
PACKAGE OUTLINE: 8 LEAD PLASTIC SOIC (.150" WIDE)

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SCALE: N/A
REVISION: 03