NEC Electronics Inc.

MC-421000A8
1,048,576 x 8-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A8 is a fast-page 1,048,576-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles.

The MC-421000A8 is available with eight μPD421000 DRAMs (1M x 1) or two μPD424400 DRAMs (1M x 4) in a variety of 30-pin Single Inline Memory Modules (SIMMs™).

Features

- 1,048,576-word by 8-bit organization
- Single +5-volt power supply
- Eight 1M DRAMs or two 4M DRAMs in a 30-pin SIMM package
- Low power dissipation
- TTL-compatible inputs and outputs
- Fast-page option

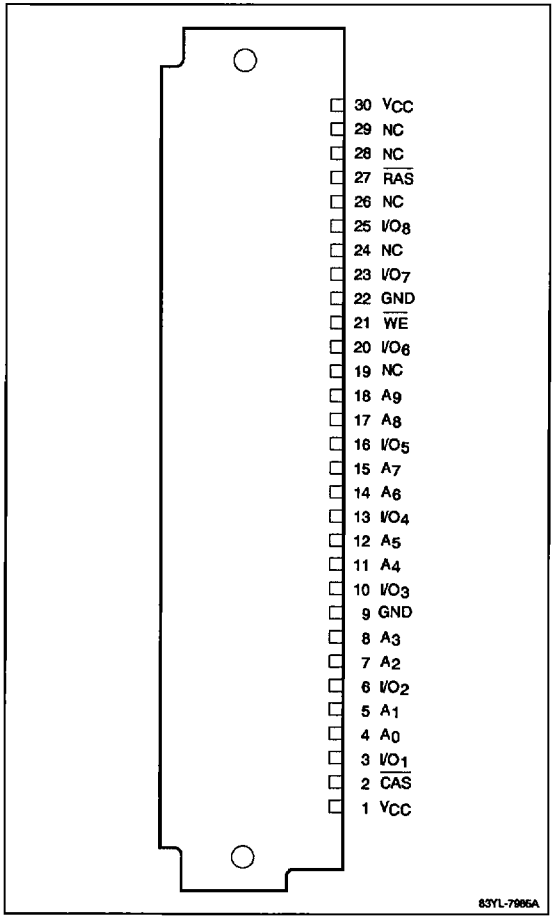
Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configurations

30-Pin Socket-Mountable SIMM (MC-421000A8: Suffix B, F, BA, FA, BB, FB)



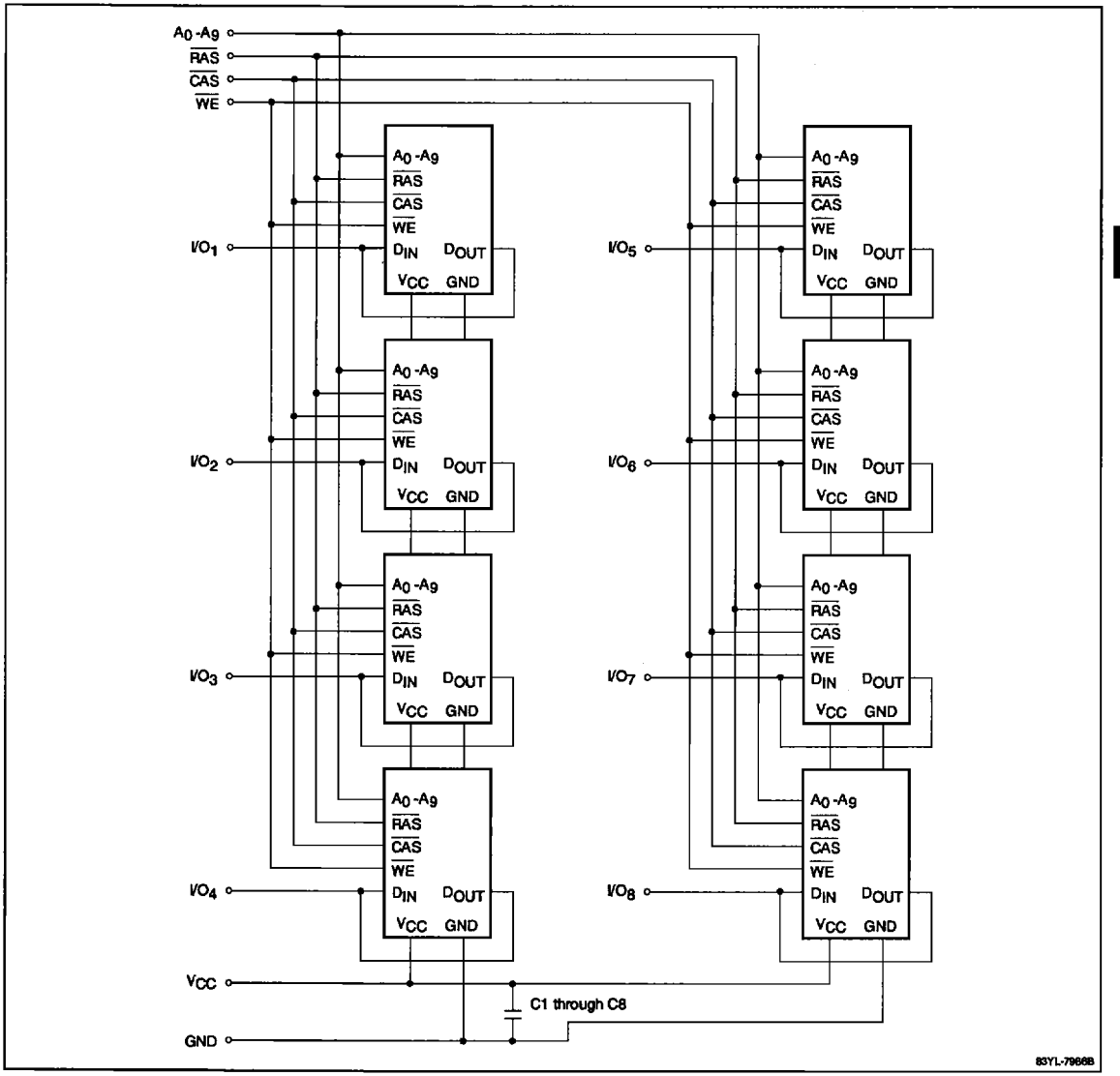
Ordering Information, Modules With Eight 1M x 1 DRAMs

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A8B-60	60 ns	30-pin socket-mountable SIMM (solder plating)	20 mm (0.787 inch)	5.28 (0.208 inch)	Eight μPD421000LA
B-70	70 ns				
B-80	80 ns				
MC-421000A8F-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				

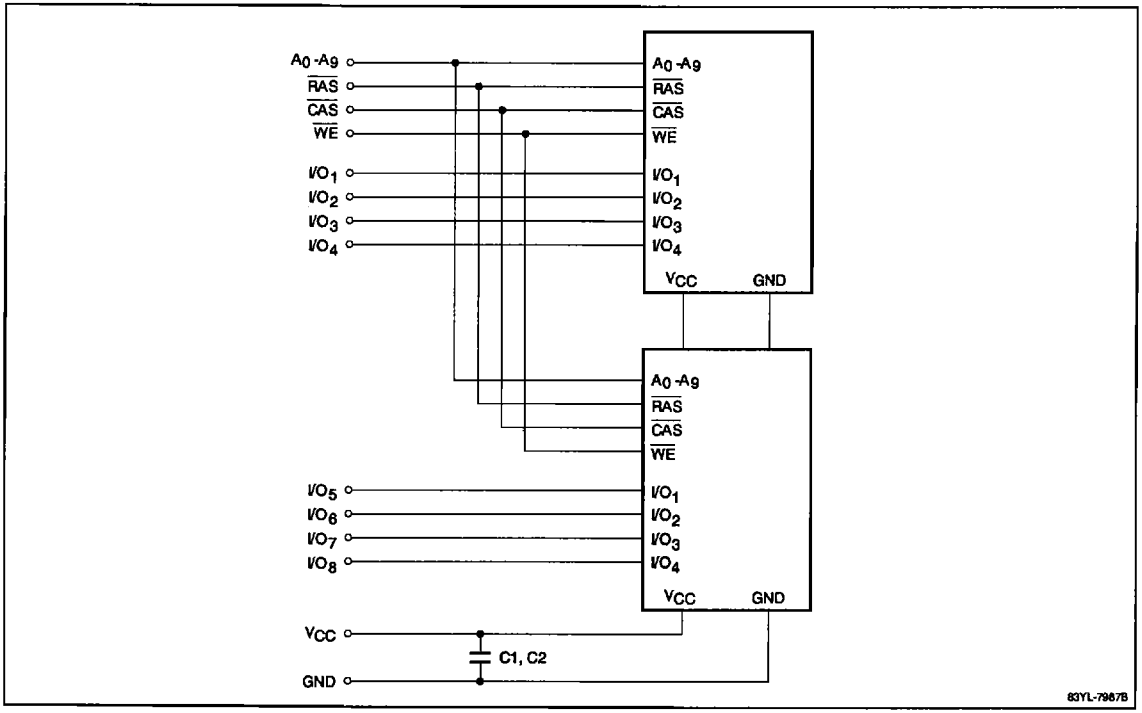
Ordering Information, Modules With Two 1M x 4 DRAMs

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A8BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)	16.67 mm (0.656 inch)	5.28 mm (0.208 inch)	Two μPD424400LA
BA-70	70 ns				
BA-80	80 ns				
MC-421000A8FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FA-70	70 ns				
FA-80	80 ns				
MC-421000A8BB-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
BB-70	70 ns				
BB-80	80 ns				
MC-421000A8FB-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FB-70	70 ns				
FB-80	80 ns				

Connection Diagram; Modules With Eight 1M x 1 DRAMs



Connection Diagram; Modules With Two 1M x 4 DRAMs



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	
Modules with eight 1M x 1 DRAMs	8.0 W
Modules with two 1M x 4 DRAMs	2.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Ambient temperature	T_A	0		70	°C	
Input leakage current						
Modules with eight 1M x 1 DRAMs	I_{IL}	−80		80	μA	For Addresses, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 V to V_{CC}; other pins = 0 V
Modules with two 1M x 4 DRAMs	I_{IL}	−20		20	μA	
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8: D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

Capacitance

T_A = 25°C; f = 1 MHz

		Modules With Eight 1M x 1 DRAMs		Modules With Two 1M x 4 DRAMs			
Parameter	Symbol	Min	Max	Min	Max	Unit	Pins Under Test
Input capacitance	C_{I1}		60		24	pF	Addresses, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	$C_{I/O}$		15		12	pF	I/O_1 - I/O_8

DC Characteristics; Modules With Eight 1M x 1 DRAMs

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		720		640		560	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Standby current	I_{CC2}		24		24		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8		8		8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Refresh operating current, average	I_{CC3}		720		640		560	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Fast-page operating current, average	I_{CC4}		640		560		480	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		720		640		560	mA	t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)

DC Characteristics; Modules With Two 1M x 4 DRAMs

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		240		200		180	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Standby current	I_{CC2}		4		4		4	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			2		2		2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Refresh operating current, average	I_{CC3}		240		200		180	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Fast-page operating current, average	I_{CC4}		180		160		140	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		240		200		180	mA	t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Access time from column address	t_{AA}		30		35		45	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		ns	(Note 19)
Column address setup time	t_{ASC}	0		0		0	20	ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	(Note 18)
Data setup time	t_{CLZ}	0		0		0		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	20	10	20	ns	(Note 11)
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	(Note 19)
Data-in hold time	t_{DH}	15		15		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		ns	(Note 19)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 12)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	50	25	60	ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period Modules with eight 1M x 1 DRAMs	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
Modules with two 1M x 4 DRAMs	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		ns	(Note 19)
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
Write command pulse width	t_{WP}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (-1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max)

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(18) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

(19) This parameter is not needed for MC-421000A8-60/-70

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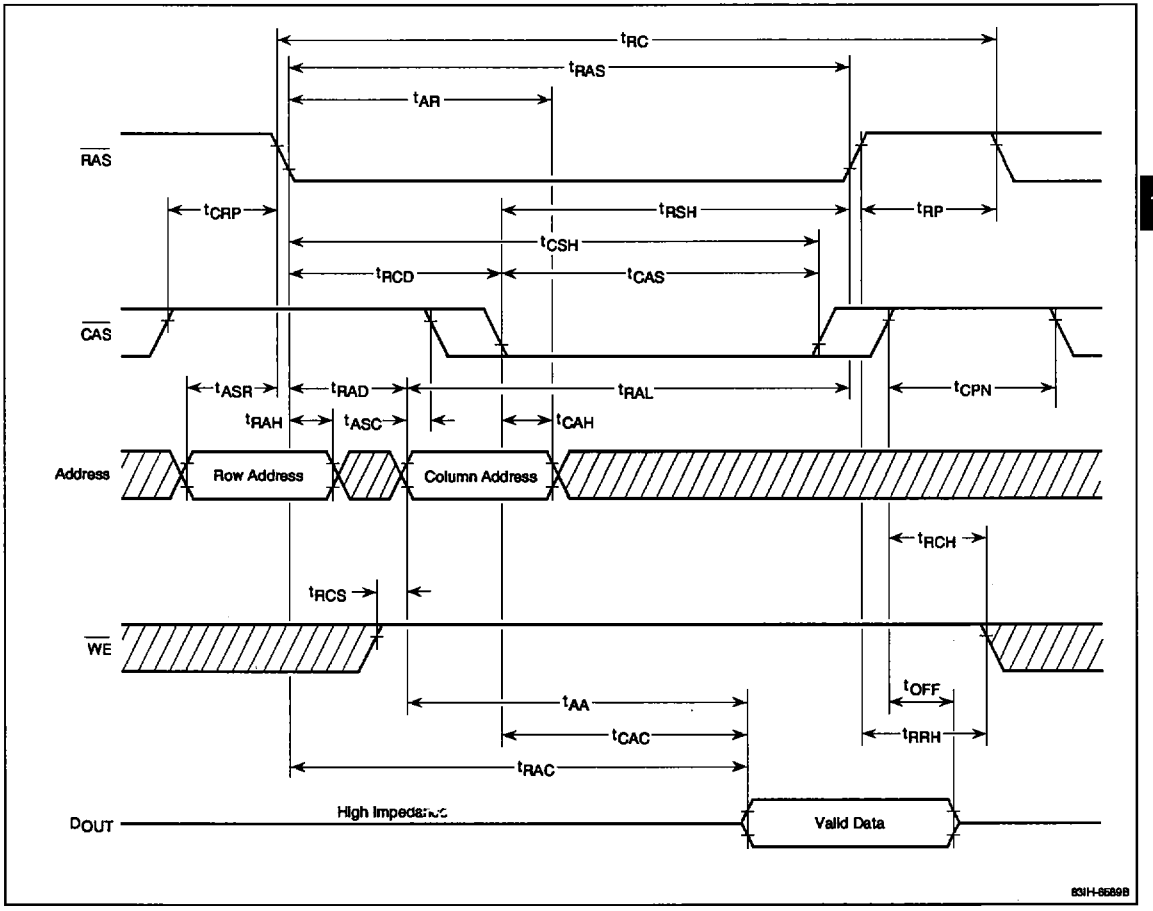
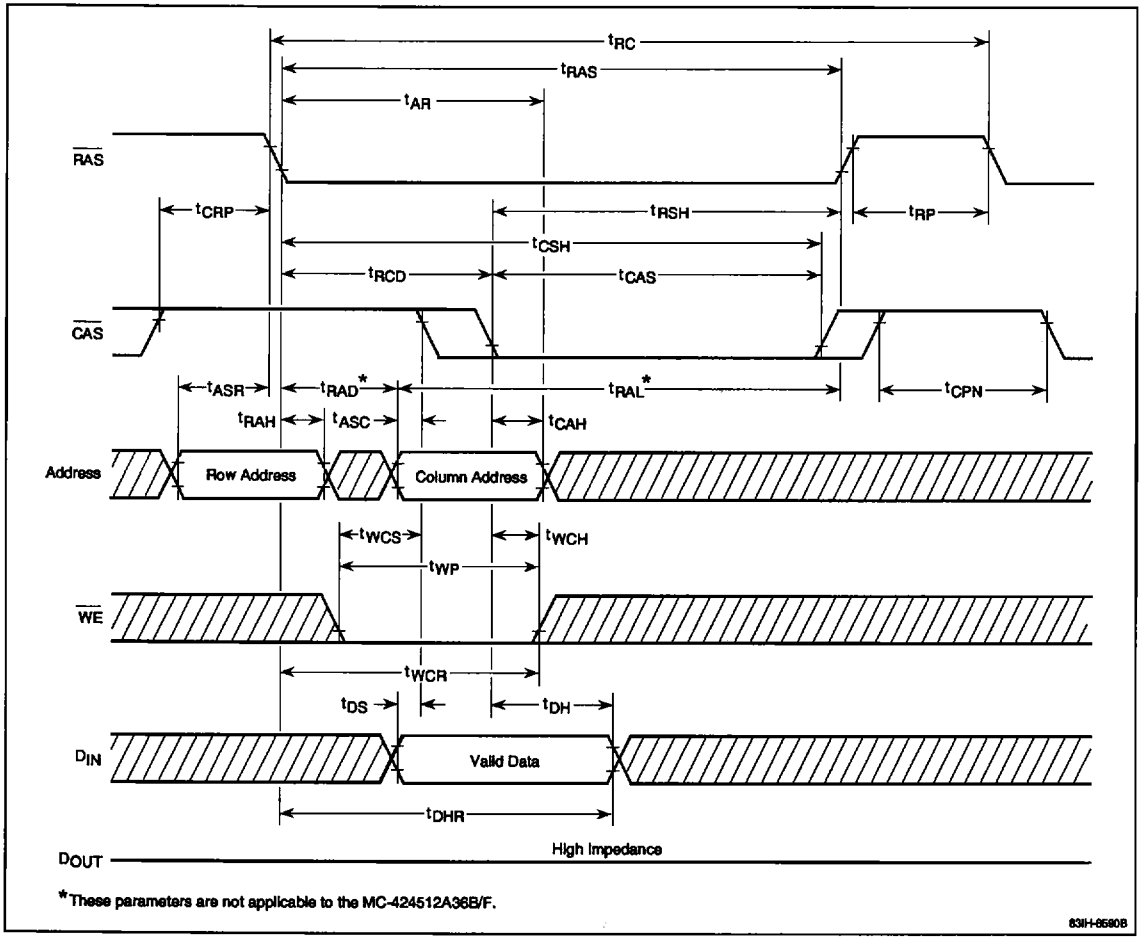
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle

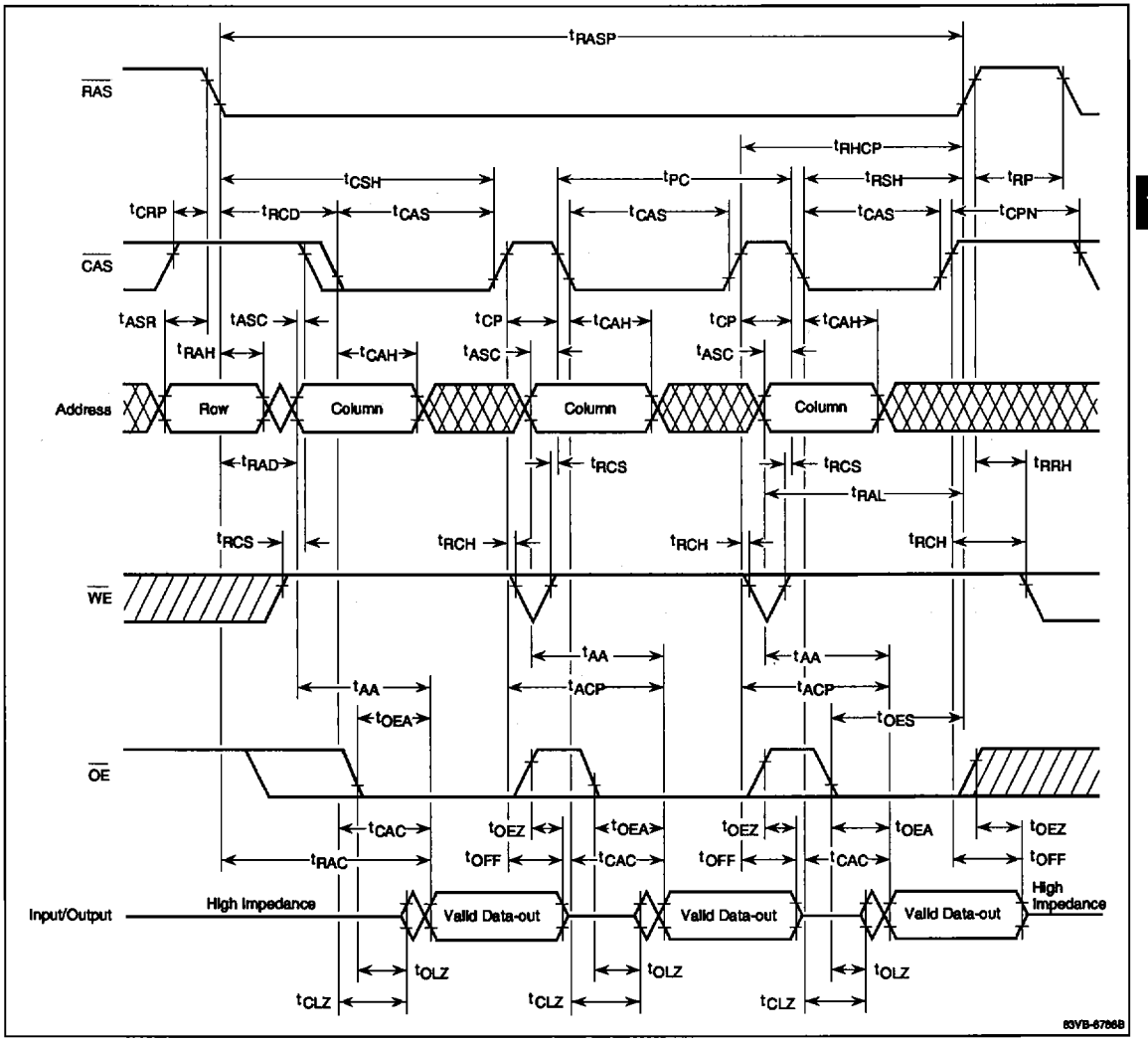


*These parameters are not applicable to the MC-424512A36B/F.

83II-8580B

Timing Waveforms (cont)

Fast-Page Read Cycle



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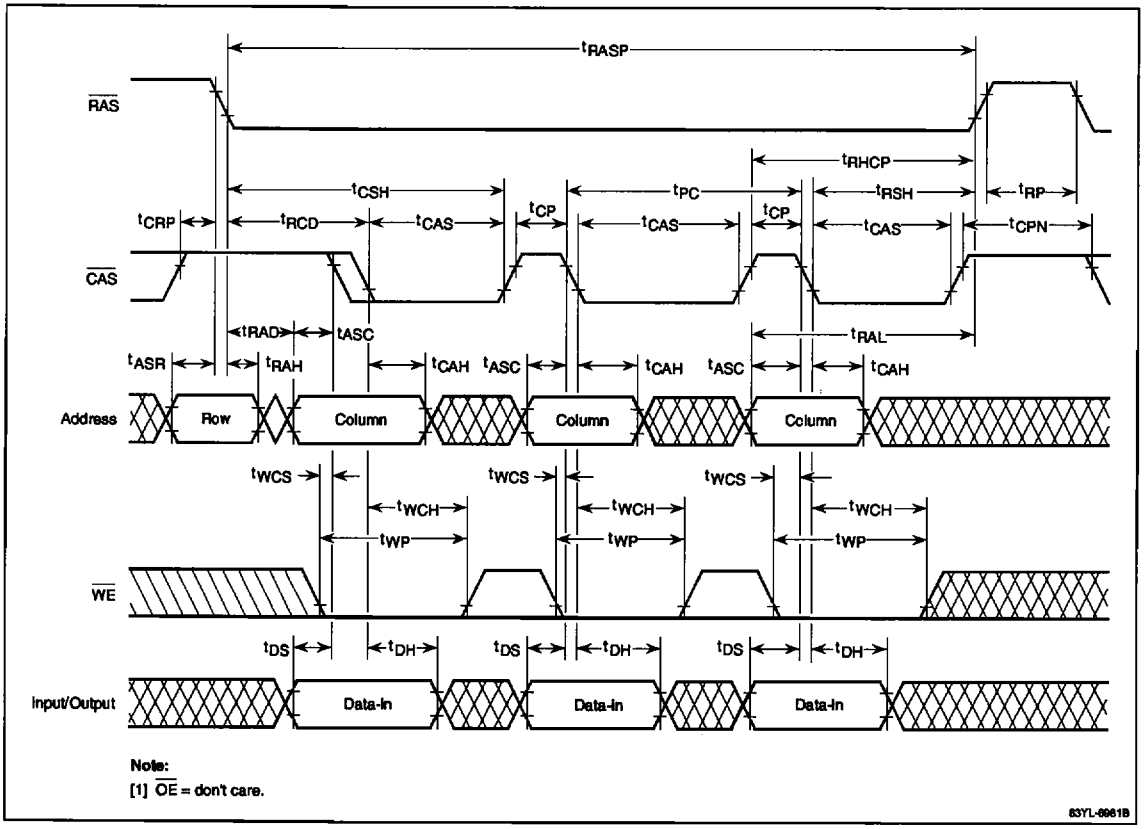
Timing Waveforms (cont)

Fast-Page Early Write Cycle

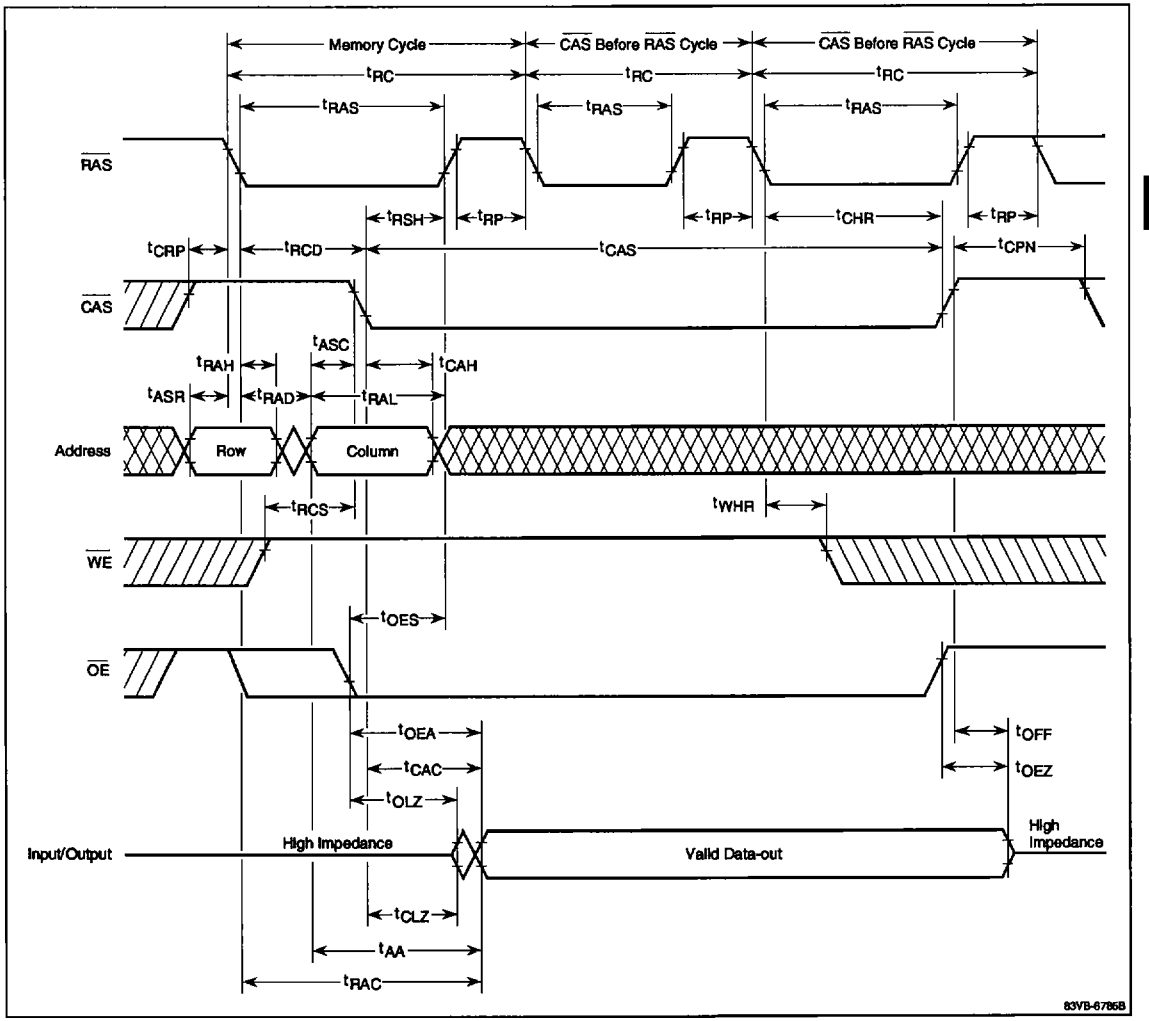


Note:
[1] $\overline{OE}$ = don't care.

83YL-6661B

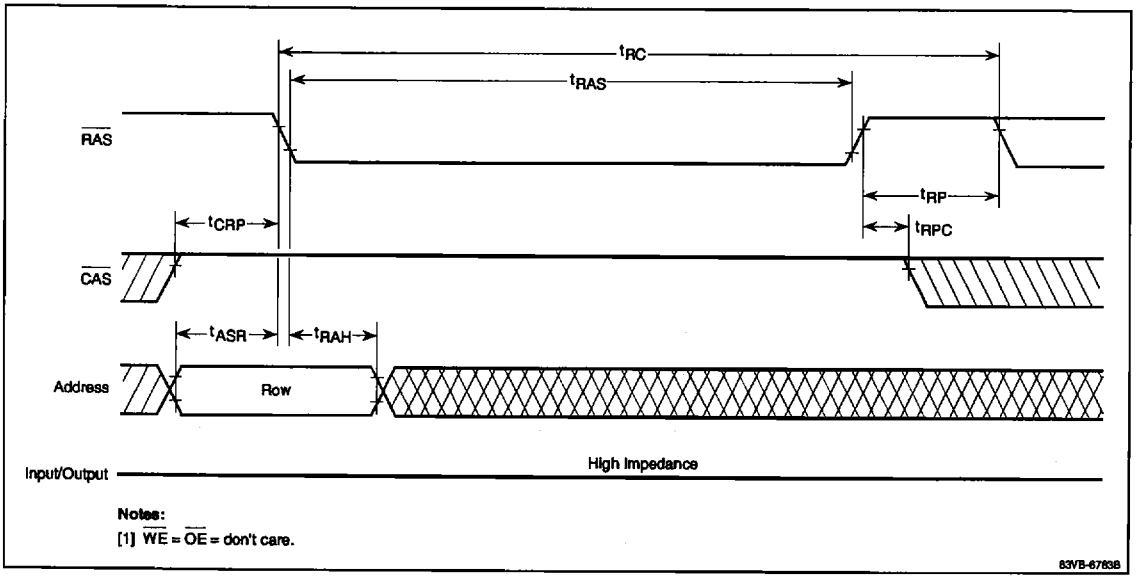
Timing Waveforms (cont)

Hidden Refresh Cycle

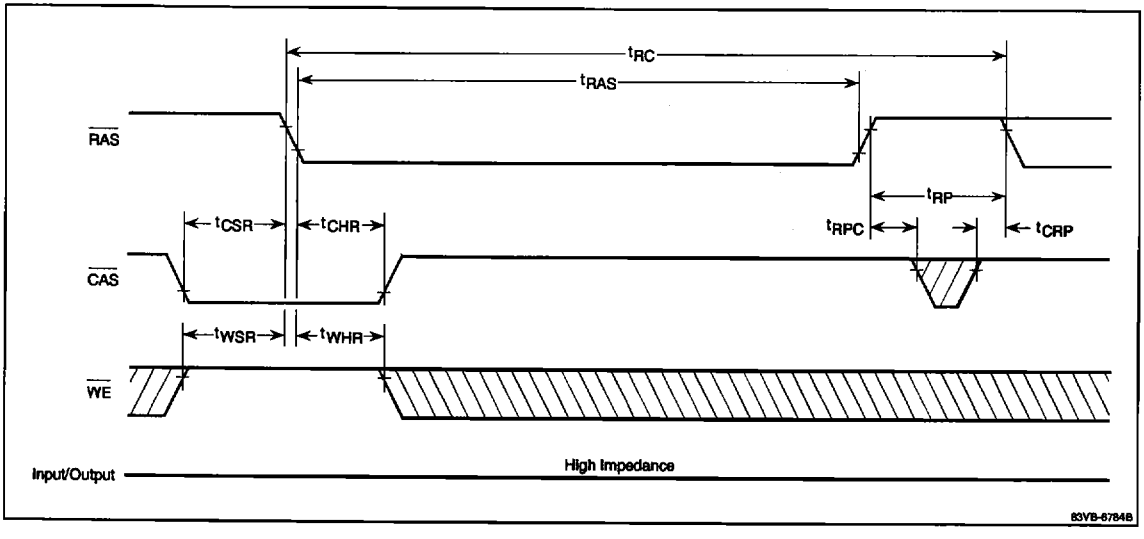


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



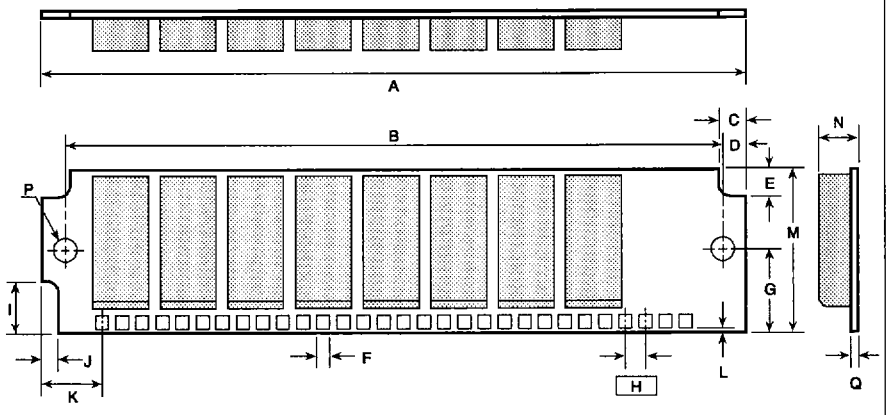
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawings

30-Pin Socket-Mountable SIMM (MC-421000A8: Suffix B, F)

Item	Millimeters	Inches
A	88.9 ± 0.5	3.500 ± .020
B	82.14	3.234
C	3.56	.140
D	3.38	.133
E	3.5	.138
F	1.77	.070
G	10.16	.400
H	2.54 (T.P.)	.100 (T.P.)
I	6.35	.250
J	2.03	.080
K	7.62	.300
L	0.2	.008
M	20.0	.787
N	5.28 max	.208 max
P	3.18 dia	.125 dia
Q	1.27 ± 0.15	.050 ± .006

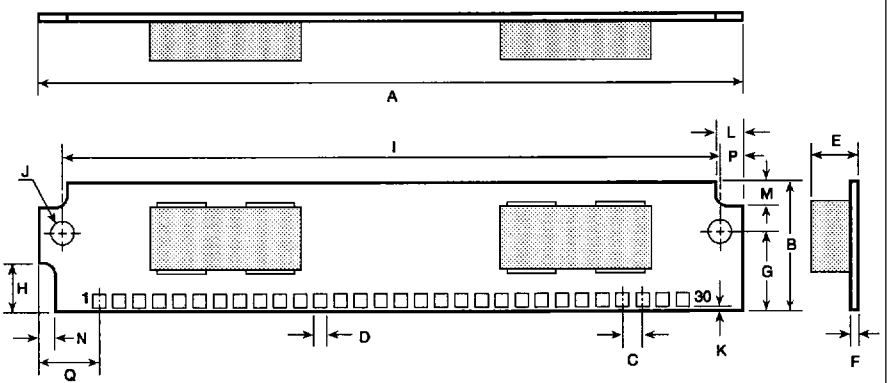


MC-421000A8: B, F

83YL-7991B (8/92)

30-Pin Socket-Mountable SIMM (MC-421000A8: Suffix BA, FA, BB, FB)

Item	Millimeters	Inches
A	88.9 ± 0.5	3.500 ± .020
B	16.67	.656
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ± 0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300



MC-421000A8: BA, FA, BB, FB

83YL-7989B (8/92)

10a