This product is not released and the specifications herein are subject to change.

AMCC®

E4/STM-1/OC-3 ATM TRANSCEIVER WITH TTL REFCLK S3030

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLLs for clock generation and clock recovery
- On-chip analog circuitry for transformer driver and equalization
- Supports 139.264 Mbit/s (E4) and 155.52 Mbit/s (OC-3) transmission rates
- Supports 139.264 Mbit/s and 155.52 Mbit/s Coded Mark Inversion (CMI) interfaces
- TTL Reference frequencies of 19.44 and 38.88 MHz (OC-3) or 17.408 and 34.816 MHz (E4)
- Interface to both PECL and TTL logic
- Lock detect on clock recovery function — monitors runlength and frequency
- Serial and 4 bit (nibble) system interfaces
- Low jitter PECL interface
- +5v operation
- Small 80 PQFP package
- Supports both electrical and optical interfaces

APPLICATIONS

- ATM over SONET/SDH
- OC-3/STM-1 or E4-based transmission systems
- OC-3/STM-1 or E4 modules
- OC-3/STM-1 or E4 test equipment
- Section repeaters
- Add drop multiplexors
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3030 transceiver chip is a fully integrated CMI encoding transmitter and CMI decoding receiver. The chip derives high speed timing and data signals for SONET/SDH or PDH-based equipment. The circuit is implemented using AMCC's proven Phase Locked Loop (PLL) technology. Figure 1a and 1b show typical network applications.

The S3030 has two independent VCOs which are synchronized to the local NRZ transmitted data and the received CMI data repectively. The chip can be used with either a 19.44 MHz or a 38.88 MHz reference clock when operated in the SONET/SDH OC-3 mode. In E4 mode the chip can be operated with a 17.408 MHz or a 34.816 MHz reference in support of existing system clocking schemes. On-chip coded-mark-inversion (CMI) encoding and decoding is provided for 139.264 Mbit/s and 155.52 Mbit/s interfaces.

The low jitter PECL interface for the serial data inputs and the PECL nibble clock interface guarantee compliance with the bit-error rate requirenemts of the Bellcore, ANSI, and ITU-T standards. The S3030 is packaged in a 0.8mm pitch 80-pin PQFP.

The S3030 provides the major active components on-chip for a coaxial cable interface, including analog transformer driver circuitry and equalization interface circuitry. Discrete controls permit separate selection of CMI or NRZ operation and analog (coaxial copper) or PECL (optical module) media interfaces. Both line loopback and diagnostic local loopback operation are supported.

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Figure 1a. Electrical Interface

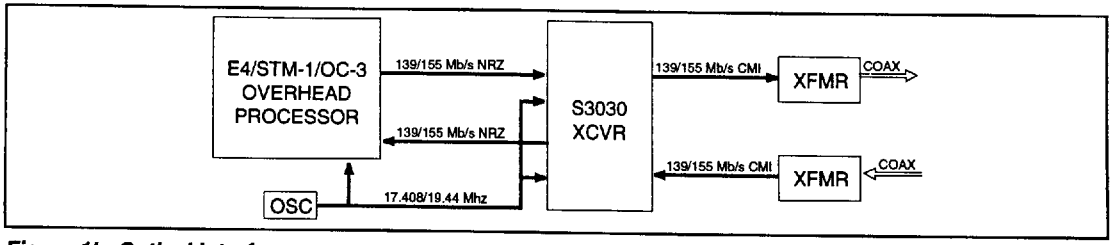
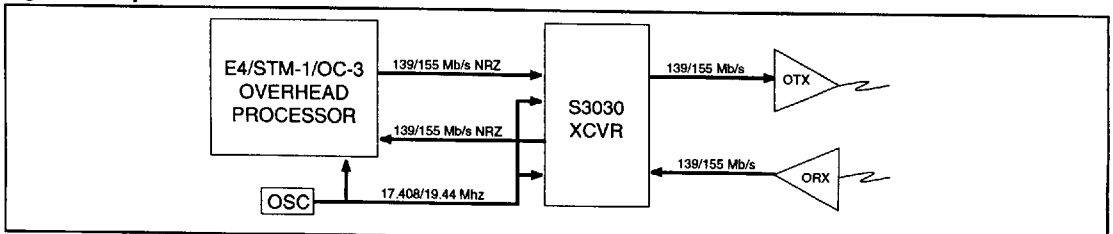


Figure 1b. Optical Interface



S3030 OVERVIEW

The S3030 transceiver can be used to implement the front end of STS-3, OC-3 or E4 equipment. The block diagram in Figure 9 shows the basic operation of the chip.

When the S3030 is operating in the Nibble parallel mode, the transmitter VCO is synchronized to the 38.88 MHz Nibble clock as both the reference clock and the data transfer clock. If the serial input is selected as the transmitter data source the VCO will be synchronized directly to the incoming data. Serial operation of the S3030 transmitter section is possible with either the 38.88 MHz or 19.44 MHz reference oscillator. In the absence of incoming serial data the transmitter section will operate as a clock synthesizer. The receiver section performs clock recovery by synchronizing its on-chip VCO directly to the incoming data stream.

The S3030 provides a PECL output for an optical interface and two transformer driver outputs for an electrical interface. One of these drivers is a monitor output. The S3030 provides a PECL input for an optical interface and an analog input for an electrical interface.

The transformer driver outputs are separately enabled. Status ouputs detect the disabled, stuck at 1, stuck at 0, and non-CMI states to qualify the transformer driver outputs.

The CMI outputs, Analog equalizer input section, and PLL sections are independently powered for isolation and for power savings when device is used in single function applications.

S3030 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

S3030 TRANSCEIVER ARCHITECTURE/ FUNCTIONAL DESIGN

Transmitter Operation

The S3030 chip's transmitter section performs the last stages of digital processing of a transmit SONET STS-3 or ITU-T E4 serial or 4-bit nibble parallel data stream.

Clock Recovery

If the serial input data has been selected, and serial data is present at the SERDATIP/N inputs, the clock is recovered from the serial data stream at 139.264 MHz or 155.52 MHz and synthesized to 278.528 MHz or 311.04 MHz to CMI encode the incoming data.

In clock recovery mode, the transmitter PLL continues to monitor the reference clock with respect to the VCO and the activity of the serial data input. The transmitter PLL will re-lock to the reference clock under the following conditions:

1. If the serial data inputs contains insufficient transition density (runlength greater than 100 to 800 bit times).

2. If the VCO drifts away from the local reference clock by more than 1000 ppm.

If either XFRMENA or XFRMENB are enabled (logic low) the density or frequency error defined above will set the appropriate status (XFMSTATA and/or XFMSTATB) to the low or fault state.

The selected drive status bits will return to the high or clear state and the PLL will again lock to the data if the serial data contains sufficient transition density (less than 100 to 800 bit times between rising edges) and the serial clock is within 250 ppm of the reference clock determined frequency.

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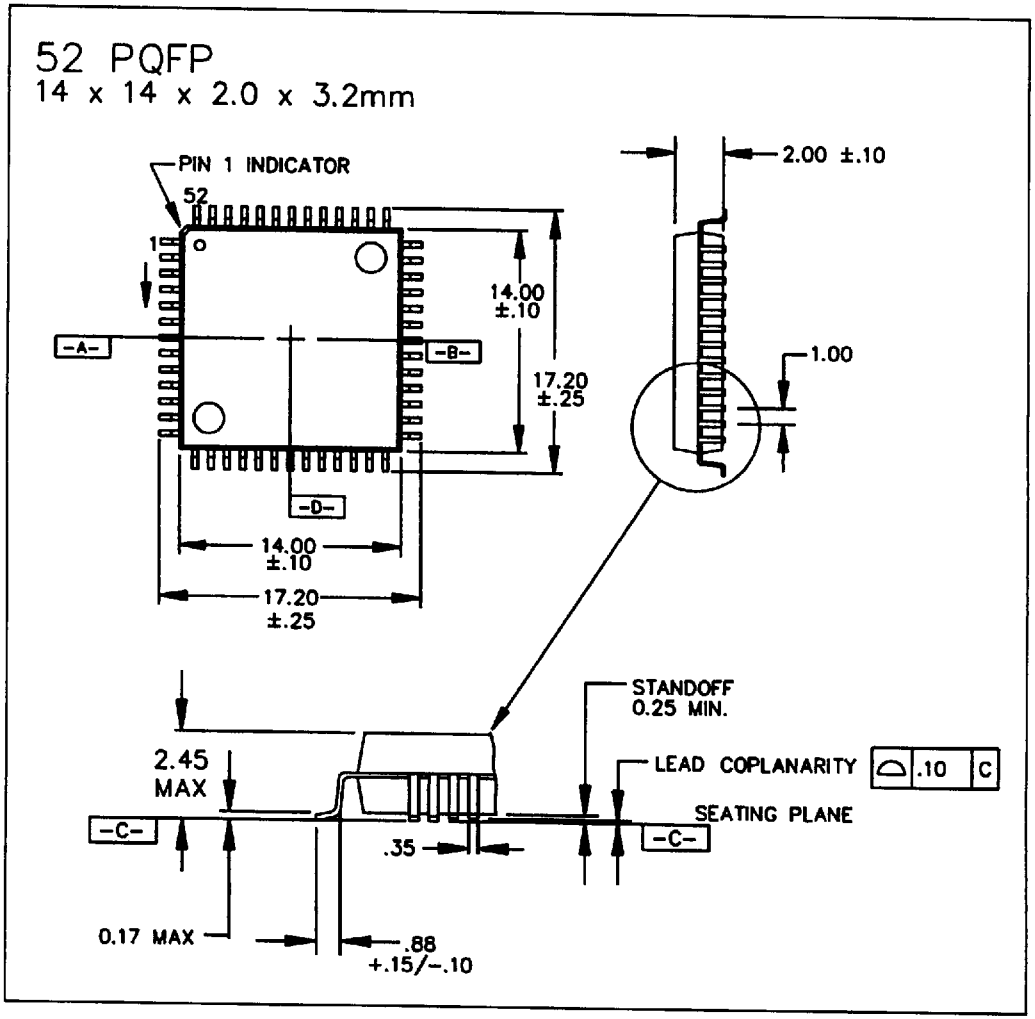
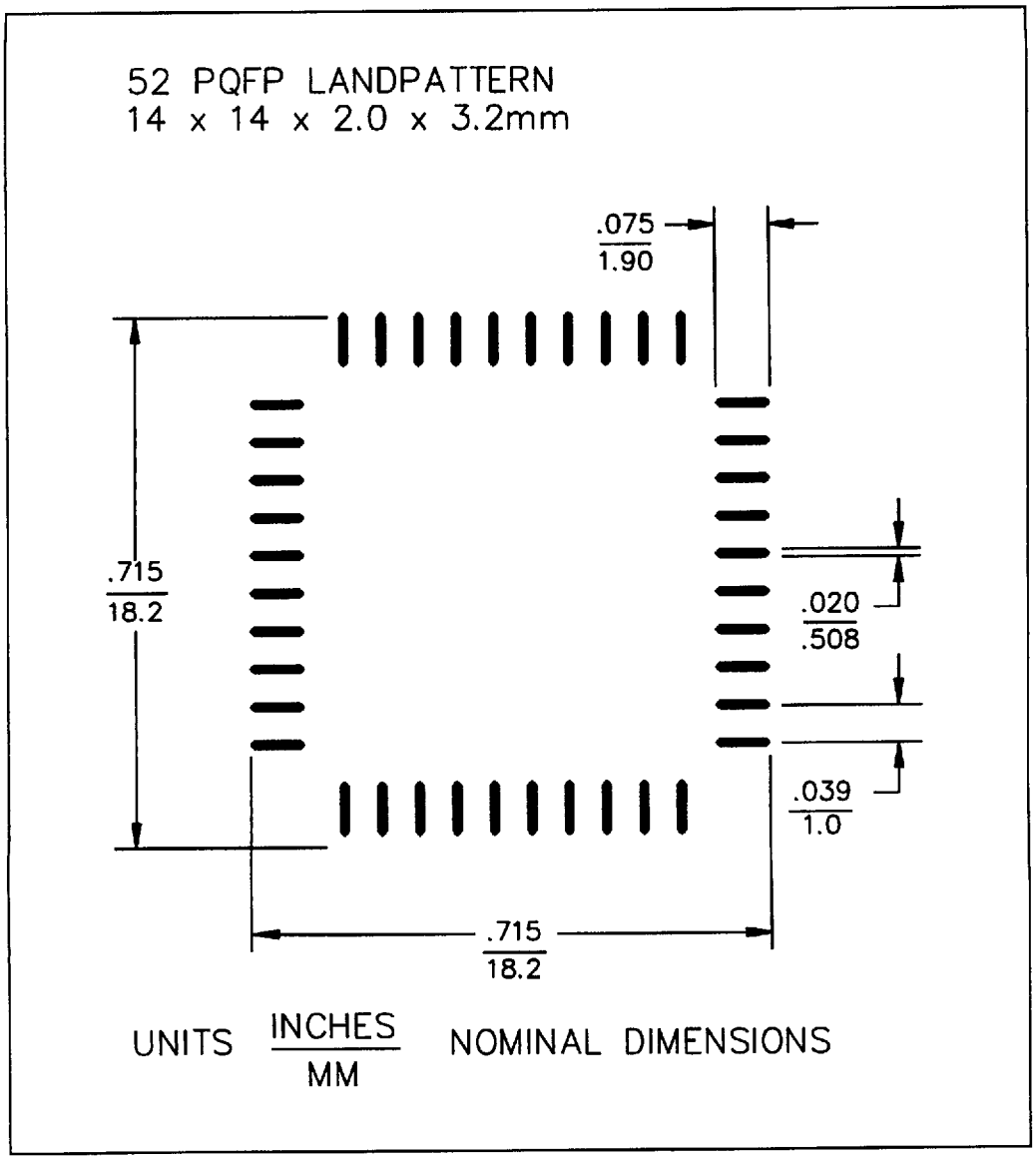

52 PQFP
14 x 14 x 2.0 x 3.2mm
PIN 1 INDICATOR
52
1
-A-
-B-
-D-
14.00 ±.10
17.20 ±.25
14.00 ±.10
17.20 ±.25
2.00 ±.10
1.00
STANDOFF 0.25 MIN.
LEAD COPLANARITY .10 C
SEATING PLANE
2.45 MAX
-C-
.35
0.17 MAX
.88 +.15/-.10

52-PIN PQFP MECHANICAL DIMENSIONS



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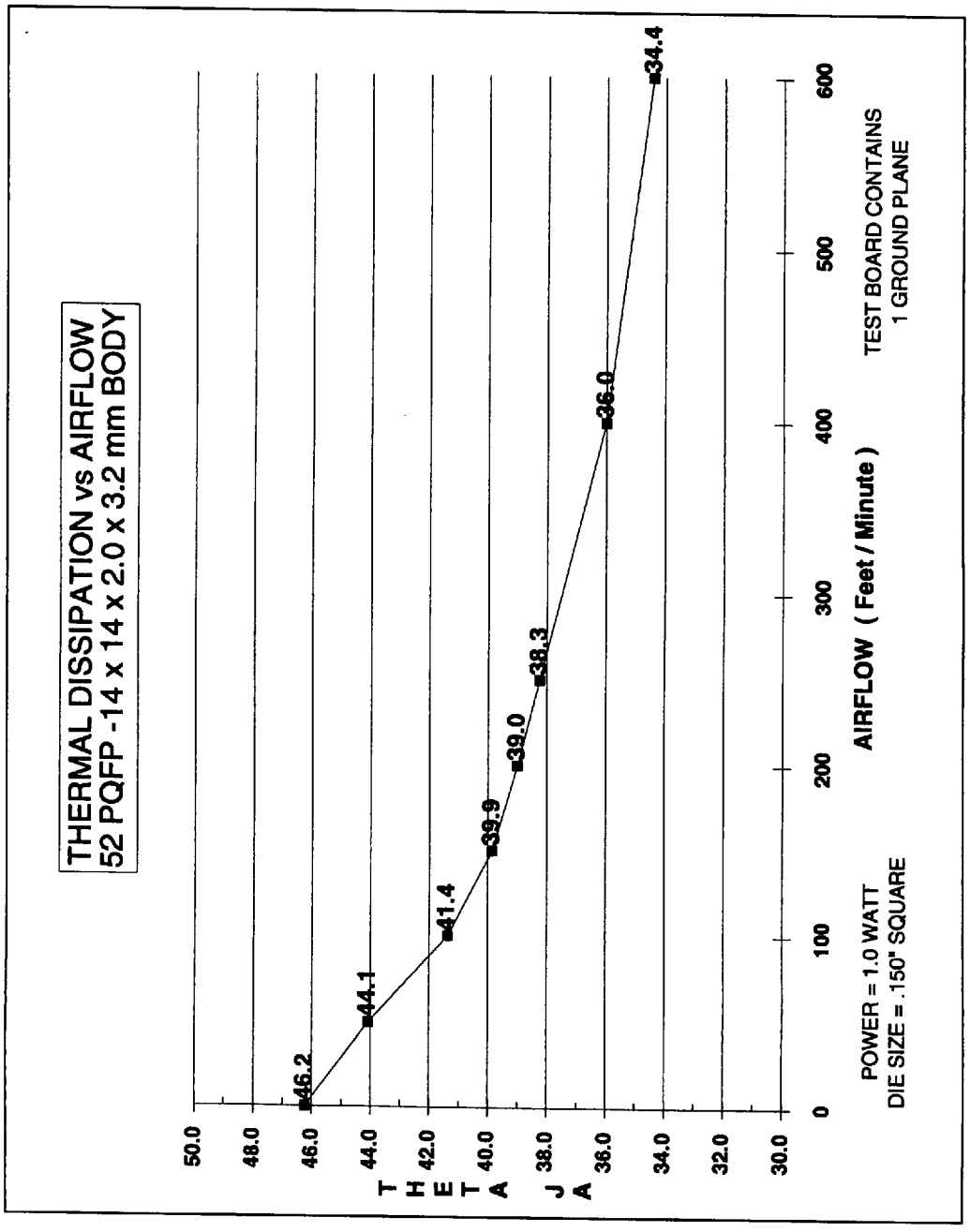
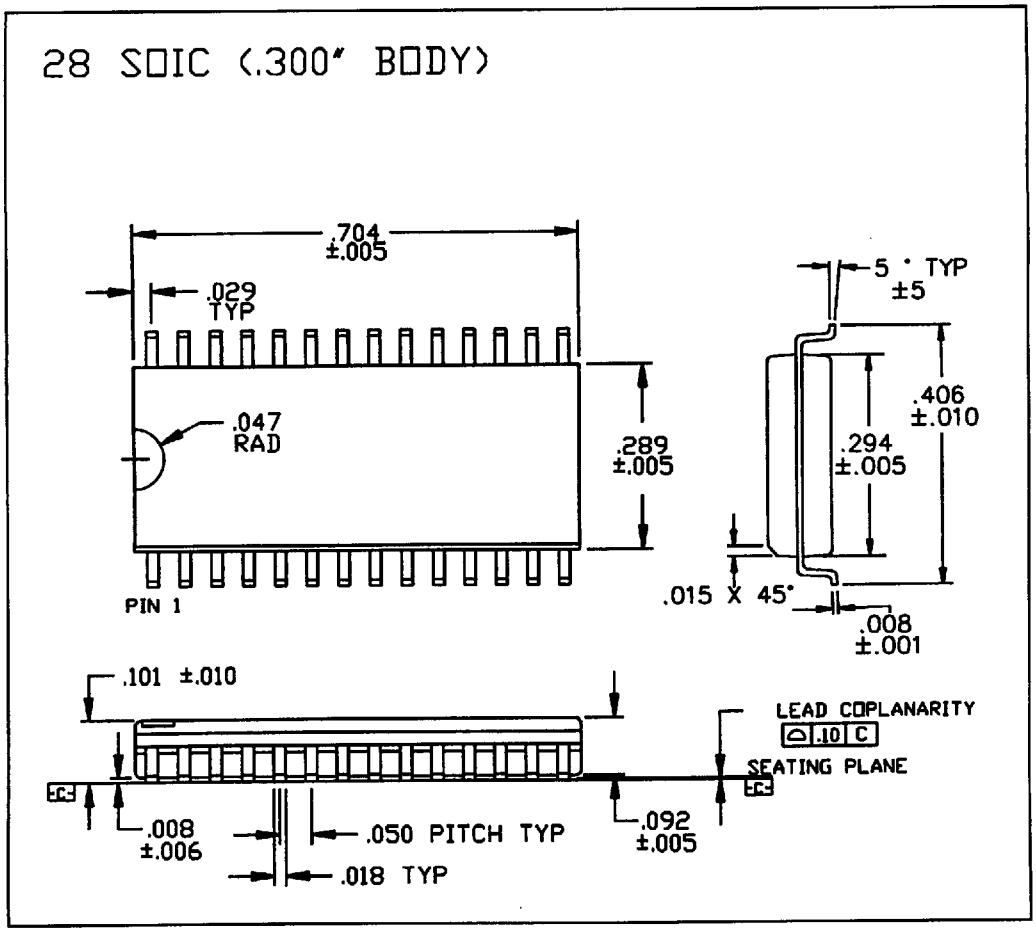

THERMAL DISSIPATION vs AIRFLOW
52 PQFP -14 x 14 x 2.0 x 3.2 mm BODY
THETA JA
50.0
48.0
46.0
44.0
42.0
40.0
38.0
36.0
34.0
32.0
30.0
46.2
44.1
41.4
39.9
39.0
38.3
36.0
34.4
0
100
200
300
400
500
600
AIRFLOW (Feet / Minute)
POWER = 1.0 WATT
DIE SIZE = .150" SQUARE
TEST BOARD CONTAINS
1 GROUND PLANE

10

28-PIN SOIC MECHANICAL DIMENSIONS



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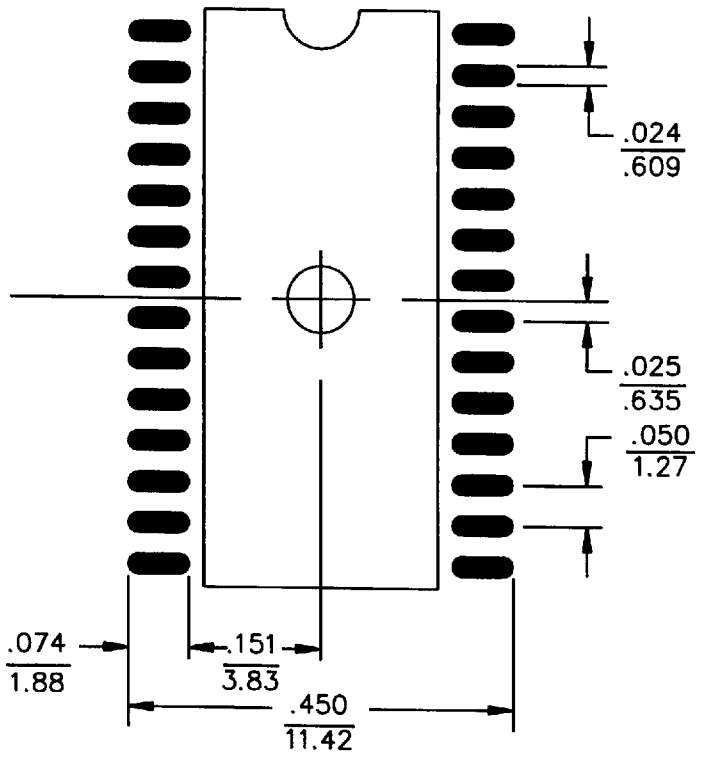
28 SOIC (.300" BODY) LANDPATTERN



UNITS $\frac{\text{INCHES}}{\text{MM}}$ NOMINAL DIMENSIONS

28-PIN SOIC MECHANICAL DIMENSIONS