Am6108 • Am6148

Microprocessor Compatible 8-Bit A/D Converter

DISTINCTIVE CHARACTERISTICS

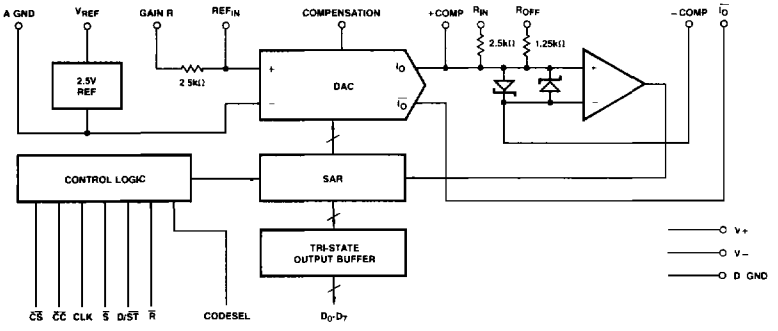
- 1 μs conversion time
- Trimmed internal voltage reference
- 0.1% nonlinearity
- Ratiometric operation
- Low operating voltages
- Internal matched gain, reference and offset resistors
- Microprocessor compatible
- 3-state outputs
- Pin-programmable unipolar or bipolar two's complement conversion
- Conversion complete available as interrupt or as multiplexed output on data bus
- Available in slim, 24-pin, 0.3" and standard, 28-pin, 0.6" packages

FUNCTIONAL DESCRIPTION

The Am6108 and Am6148 are microprocessor-compatible, 8-bit, high-speed, analog-to-digital converters. They include a precision reference, DAC, comparator, SAR, scale resistors, 3-state output buffers and control logic. The Am6108 is available in a standard .600-inch-wide, 28-pin package, and the Am6148 is offered in a space-saving, .300-inch-wide, 24-pin package. The Am6108/Am6148 are capable of completing an 8-bit conversion in under one microsecond and can handle input voltage ranges of 0 to +10V, 0 to +5V, and ±5V without external components. With appropriate external resistors, the user can program the device to operate on other input signal ranges (2 or 3 precision resistors are required). Full 8-bit monotonic performance with no missing codes is guaranteed over temperature. Both devices have 3-state outputs for bus compatibility and a status output.

The Am6108/Am6148 are useful in microprocessor-based systems or can be used in a stand-alone mode. The conversion time is short enough to allow most microprocessors to accept data immediately after requesting a conversion. Applications include Analog I/O subsystems, process control and servo-control.

Am6108 EQUIVALENT CIRCUIT



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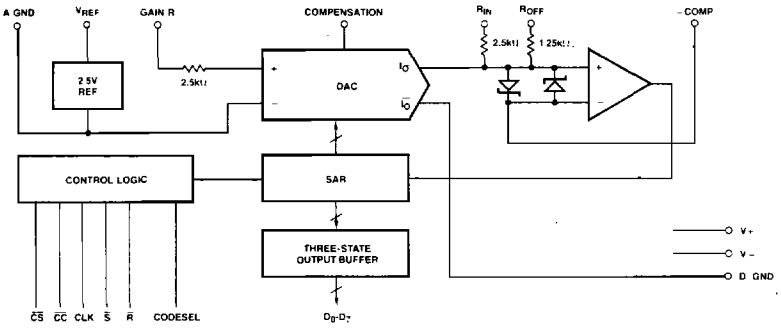
Am6148 EQUIVALENT CIRCUIT



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THEORY OF OPERATION

A conversion cycle in the Am6108/Am6148 begins by taking the $\overline{S}$ input low simultaneously with $\overline{CS}$ low and the CLK input low, this resets the Successive Approximation Register (SAR). When $\overline{S}$ is returned high, all bits of the SAR are ones with the exception of the MSB, which is set to a zero. The output of the SAR is fed to a DAC that converts it to a current. The current from the DAC output is then compared with the current generated by the analog input voltage. Based on this comparison, the SAR either keeps the MSB as a zero or resets it to a one before beginning the next approximation. This process of successive removal and testing continues until all bits have been tested. At that time the conversion complete, $\overline{CC}$, output goes low, and the Am6108/Am6148 is ready to output the data byte or begin a new conversion.

Read operations in the Am6108/Am6148 are initiated by taking $\overline{CS}$ and $\overline{R}$ both low to enable the 3-state data outputs. On the Am6108 only, if D/$\overline{ST}$ is held low, then $\overline{CC}$ is output at D_7 and $D_6 - D_0$ are held disabled. This allows the processor to check the status of the converter to determine if the conversion is complete. When $\overline{CS}$ and $\overline{R}$ are both held low with D/$\overline{ST}$ high, the 3-state outputs will not be enabled until $\overline{CC}$ goes low. When the 3-state outputs are enabled there are two formats for reading data out of the Am6108/Am6148: two's complement format is selected by holding CODESEL low during the read, and binary offset is selected by holding CODESEL high. Figure 1 shows the complete decoding of the Am6108/Am6148 control lines.

The full-scale output current of the DAC is determined by the reference current supplied to the GAIN R and/or REF_{IN} inputs of the Am6108/Am6148. The DAC full-scale output current is four times the reference current. The GAIN R input is a 2.5KΩ series resistor that will convert the 2.5V internal reference voltage into a 1mA reference current. The REF_{IN} input, on the Am6108 only, allows the user to provide his own scaling resistor for determining the reference current.

Once the DAC reference current is set up, the Am6108/Am6148 can be operated with either a unipolar or bipolar input signal. Two inputs are provided for unipolar operation, the R_{IN} input has a 2.5KΩ resistor connected between it and the comparator summing node. The R_{OFF} input is identical to R_{IN}, except the value of the resistor is 1.25KΩ. The R_{IN} input is used alone for a unipolar input of 0 to +10V and the R_{OFF} input is used alone for 0 to +5V signals. The bipolar operation of the Am6108/Am6148 requires a half-scale offset current to be supplied to the comparator summing node. This can be accomplished by connecting the R_{OFF} input to the V_{REF} output, which produces a 2mA offset current to the comparator summing node. A −5 to +5V input signal can be applied at R_{IN}. A third input, +COMP, is connected directly to the comparator summing node. This allows the user to provide any external scaling networks desired for the Am6108 operation. This +COMP is not available on the Am6148.

Figure 1. Am6108/ Am6148 Control Signal Decoding

Signals							
CLK	$\overline{CS}$	$\overline{S}$	$\overline{R}$	D/$\overline{ST}$*	CODESEL	$\overline{CC}$	Function
X	1	X	X	X	X	X	Outputs Three-stated
0	0	0	X	X	X	X	Reset SAR
X	0	1	0	0	X	X	Read Status (Am6108 Only)
X	0	1	0	1	X	1	Outputs Three-stated
X	0	1	0	1	0	0	Read Data (Two's Complement Code)
X	0	1	0	1	1	0	Read Data (Binary Offset Code)

*Function available on the Am6108 only. X = Don't Care

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as the number of output bits, or 1 part in 2^n where n is the number of bits.

Monotonicity (Missing Codes): Monotonicity is a property of the D/A within a successive approximation (S/A) A/D. Each increment in the digital code to the D/A is accompanied by an analog output that is greater than, or equal to, that of the preceding code. Monotonicity of the D/A is a necessary requirement for a S/A A/D to have no missing codes.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input value which produces a given digital output code. An ideal value of a code width is equivalent to $FSR/2^n$, where n is the number of bits.

Linearity: The deviation of each individual code from an ideal straight line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an *inherent* ±1/2LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2LSB.

Unipolar Offset Error: Difference between the ideal (+½LSB) and the actual analog input level required to produce the first digital code transition (00 . . . . 00 to 00 . . . . 01) over the complete temperature range.

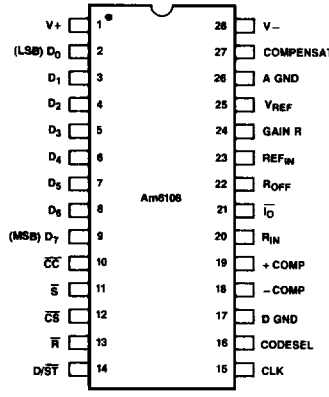
Bipolar Offset Error: Difference between the ideal (1/2FSR - 1/2LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 . . . . 11 to 10 . . . . 00).

Power Supply Sensitivity: A measure of the change in gain and offset of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: The measure of how long it takes for the A/D to arrive at the correct digital output code. It is the time between the clock edge that starts a conversion after receiving a start command and the edge of the status line ($\overline{CC}$) which signifies that the conversion is completed.

CONNECTION DIAGRAMS
Top Views

D-28-1



Standard, 0.6" Package

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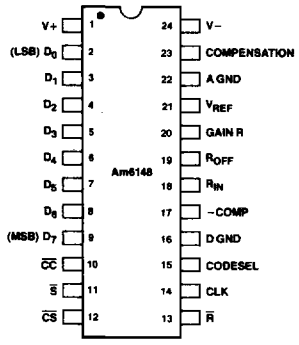
D-24-SLIM



Slim, 0.3" Package

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FUNCTIONAL PIN DESCRIPTION

Symbol	Function
V_{REF}	Reference Voltage Output – The output of the internal, precision 2.5 volt reference.
GAIN R	Reference Input Gain Resistor – A 2.5KΩ resistor in series with the positive input of the DAC reference amplifier. When 2.5 volts is applied to this pin, a 1.0mA reference current flows to the DAC. This produces a DAC full scale current of 4mA.
REF_{IN} (Am6108 Only)	Current Reference Input – This pin is directly connected to the positive input of the DAC reference amplifier. The DAC full scale output current is four times the reference current applied to this input.
R_{IN}	Analog Input Resistor – A 2.5KΩ resistor in series with the summing node at the noninverting input to the comparator. It converts the analog input voltage to a current for comparison with the current at the DAC I_O output. When the DAC has a reference current of 1.0mA, this input can be used alone for a 0 to +10 volt input range, or in conjunction with the R_{OFF} input for a −5 to +5 volt range.
R_{OFF}	Input Offset Resistor – A 1.25KΩ resistor in series with the summing node at the noninverting input of the comparator. When this input is connected to the 2.5 volt reference, a half scale offset current enters the summing node. This allows a bipolar input range of −5 to +5 volts at the R_{IN} input. The R_{OFF} pin may also be used as an analog voltage input for a 0 to +5 volt range. When R_{OFF} is not used, this pin should be connected to A GND.
$\overline{I_O}$ (Am6108 Only)	DAC Complementary Current Output – This output should be tied to the digital ground. On the Am6148, $\overline{I_O}$ is internally connected to digital ground.
−COMP	Comparator Inverting Input – Allows the user to add an offset voltage to null the system or as a zero reference. It may also be used as a high-impedance input, normally it is connected to analog ground.
+COMP (Am6108 Only)	Comparator Noninverting Input – This input allows the user to add his own external scaling network to the summing node at the noninverting input of the comparator.
COMPENSATION	Reference Amplifier Compensation – An external capacitor is connected between this pin and V− to provide frequency compensation for the DAC reference amplifier.
$\overline{CS}$	Chip Select – Enables the Am6108/Am6148 for read and start conversion operations.
$\overline{S}$	Start Conversion – An active low input which resets the successive approximation register. When $\overline{S}$ is taken back high, the Am6108/Am6148 begins a conversion.
$\overline{R}$	Read – An active low input which enables the 3-state outputs and allows data to be transferred from the Am6108/Am6148 to the processor.
D/$\overline{ST}$ (Am6108 Only)	Data/Status Control – This input determines whether the Am6108 outputs data, D/$\overline{ST}$ = logic 1, or a status bit, D/$\overline{ST}$ = logic 0, during a read operation. The status bit which appears at output D_7 is the same as the $\overline{CC}$ output. During a status read operation, data outputs D_0-D_6 remain 3-stated. Status output at D_7 is not available on the Am6148.
CODESEL	Code Select – A logic 1 on this input enables the Am6108/Am6148 to output data in binary offset format, a logic 0 results in two's complement format.
CLK	Clock – A TTL level clock is used at this input to produce the internal timing of the Am6108/Am6148 during a conversion.
$\overline{CC}$	Conversion Complete – This active low output indicates the end of a conversion.
D_0-D_7	Data Outputs – Eight 3-state outputs which are used to transfer data from the Am6108/Am6148 to the processor.

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.3 to +7.0V	Voltage at GAIN R, REF_{IN}	V− to V+
V− to D GND	+0.3 to −7.0V	Voltage at R_{IN}, R_{OFF}	±12V
Max Differential V+ to V−	±12V	DAC Compliance Voltage	−2 to +12V
Digital Inputs to D GND	−0.5 to +6.0V	Operating Temperature	0 to +70°C
A GND to D GND	±1V	Storage Temperature	−65 to +150°C
V_{REF} Max Output Current	15mA	Lead Temperature (Soldering 60 sec)	300°C
Max Input Current at REF_{IN}	2mA	Minimum Operating Voltage	9.7V

ELECTRICAL CHARACTERISTICS (These specifications apply for $V^+ = +5V \pm 5\%$, $V^- = -5.2V \pm 5\%$, V_{REF} connected to GAIN R, $0°C \leq T_A \leq 70°C$ and $f_{CLOCK} = 500KHz$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristics						
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Differential Nonlinearity			±1/4	±1/2	LSB
	Linearity			±1/4	±1/2	LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error	V_{IN} = 0 to +5V		±1½	±4	LSB
		V_{IN} a= 0 to +10V		±1	±2	
	Unipolar Offset Error			±1/2	±1	LSB
	Bipolar Gain Error	$V_{IN} = -5V$ to +5V		±1	±2	LSB
	Bipolar Offset Error			±3/4	±1½	LSB
	Positive Power Supply Sensitivity	$V^+ = +5V \pm 5\%$		0.02	0.2	%FS
	Negative Power Supply Sensitivity	$V^- = -5.2V \pm 5\%$		0.02	0.2	%FS
Internal Reference						
V_{REF}	Reference Voltage	I_{REF} = 1mA	2.485	2.5	2.515	Volts
V_{REF}/T_A	Reference Voltage Tempco			20		ppm/°C
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		0.05	0.2	$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	$V^+ = +5V \pm 5\%$		0.05	0.2	$\%V_{REF}$
	Noise, f_n = 10KHz to 1MHz			20		μV_{rms}
Analog Inputs						
	Input Resistance					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
	0 to 5V			1.25		KΩ
	Input Capacitance					
	R_{IN}, R_{OFF}, REF_{IN}*, GAIN R			2		pF
	$\overline{I_O}$*			20		pF
	+COMP*			20		pF
	−COMP			2		pF
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				0.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1	V_{IN} = 2.7V			40	μA
I_{IL}	Logic 0	V_{IN} = 0.4V			10	μA

*Function available on the Am6108 only.

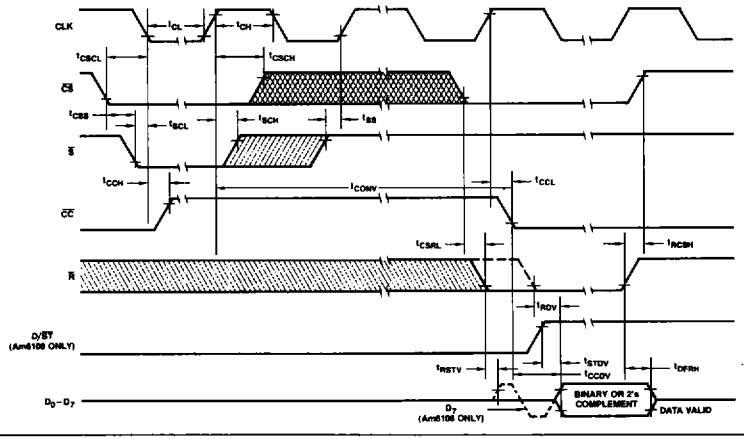
ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			0.5	Volts
I_{SC}	Output Short Circuit Current			−40		mA
I_{OZ}	**Off-State Output Current**					
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Power Requirements						
I^+	Positive Supply Current			44	60	mA
I−	Negative Supply Current			−65	−85	mA
	Power Dissipation			600	800	mW

SYSTEM TIMING

Parameters	Description	Min	Typ	Max	Units
t_{CONV}	Conversion Time		1	2	μs
t_{CSS}	$\overline{CS}$ Low to $\overline{S}$ Low	0			ns
t_{CSCL}	$\overline{CS}$ Low to CLK Low	0			ns
t_{SCL}	$\overline{S}$ Low to CLK Low	0			ns
t_{CCH}	$\overline{CC}$ High from CLK Low		35	40	ns
t_{SCH}	$\overline{S}$ High from CLK High	0			ns
t_{SS}	$\overline{S}$ High before CLK High	10			ns
t_{CSCH}	$\overline{CS}$ High from CLK High	0			ns
t_{CCL}	$\overline{CC}$ Low from CLK High	20	30	40	ns
t_{CSRL}	$\overline{CS}$ Low to $\overline{R}$ Low	0			ns
t_{RSTV}	$\overline{R}$ Low to Status Valid on D_7 (Am6108 Only)	15	30	40	ns
t_{STDV}	Status to Data Valid on D_7 (Am6108 Only)	15	30	40	ns
t_{CCDV}	$\overline{CC}$ Low to Data Valid	15	30	40	ns
t_{RDV}	$\overline{R}$ Low to Data Valid	15	30	40	ns
t_{DFRH}	Data Float from $\overline{R}$ High	20	30	40	ns
t_{RCSH}	$\overline{R}$ High to $\overline{CS}$ High	0			ns
t_{CL}	CLK Low	50			ns
t_{CH}	CLK High	50			ns

System Timing



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*Function available on the Am6108 only.

APPLICATIONS INFORMATION

The Am6108/6148 contains all the active components required to perform a complete A/D conversion. The device is specified over the complete temperature range and includes the effects of the on-chip voltage reference.

Figures 2 and 3 show the Am6108/6148 used in unipolar and bipolar configurations. Gain and offset errors may be trimmed for optimum performance using external components (discussed later). The maximum offset error, unipolar and bipolar are specified as ±1LSB and ±2LSB respectively over the complete temperature range and in many applications would not require any trimming.

Both Figures 2 and 3 show the Am6108/6148 configured as an I/O port. A conversion is started by performing a write operation to the port address. The $\overline{IOW}$ line strobes the $\overline{S}$ input to start the conversion. Operating with a 10MHz clock, the Am6108/6148 will complete a conversion within 1μsec; therefore with many CPUs, a READ operation could occur immediately after starting the conversion and receive valid data. The Am6108/6148 requires a minimum of nine clock cycles to complete a conversion, which most microprocessors can meet fairly easily. However, if the Am6108/6148 is used with a slower clock, then a circuit similar to Figure 4 may be used to hold the processor in wait states during the read operation until the $\overline{CC}$ output goes low.

The status of the A/D (Am6108 only) can be interrogated via output D_7 when $D/\overline{ST}$ = logic 0 during a read operation. During a status read operation data outputs D_0-D_6 remain three-stated. The status output at D_7 is not available on the Am6148.

The data from the A/D converter can be read out using a normal I/O read operation to the port address. The output code may be offset binary or two's complement depending upon the logical state of CODESEL (logic 1 – offset binary, logic 0 – two's complement).

The Am6108/6148 may also be interfaced with a DMA controller for burst mode operation. Figure 5 shows the Am6108/6148 interfaced with the Am9517A DMA Controller. The DMA mode of operation begins with a software request for block transfer by the Am9517A. The Am6108/6148 begins a conversion each time it receives a request and holds the DMA controller in wait states until each conversion is complete. This cycle is repeated until a complete block of data has been transferred to memory.

Unipolar Configuration (Figure 2)

The Am6108/6148 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of the code. If no trims are used, the Am6108/6148 is guaranteed to have ±1LSB max zero offset error and ±2LSB max gain error (0 to +10V full scale). If the offset trim is not required R_{OFF} (pin 22 – Am6108, pin 19 – Am6148) should be connected to analog ground. The two resistors R_1 and R_2 and potentiometer R_3 are then not needed. If the gain error (full scale) trim is not required, then resistor R_5 should be removed and the analog input connected to R_{IN} directly. The 100Ω full scale adjust potentiometer R_4 is not needed and V_{REF} out is connected directly to GAIN R. When a 0 to +5V input range is required the analog input is connected to R_{OFF} instead of R_{IN}. R_{IN} should be connected to analog ground in this application.

Unipolar Calibration

Connecting R_{OFF} to R_1 and R_2 the initial offset error can be trimmed by R_3. The first A/D transition (0000 0000 to 0000 0001) should occur for an input level of +1/2LSB (19.5mV).

The gain error (full scale) trim is done by applying a signal 1 1/2LSBs below the nominal full scale (9.94 for a 10V input range). R_4 is trimmed to give the last transitions (1111 1110 to 1111 1111).

Bipolar Configuration (Figure 3)

If the offset and gain errors are acceptable, one or both of the trimmers can be removed plus the 50Ω resistor R_3. The analog input is applied directly to R_{IN} and V_{REF} out is connected to GAIN R and R_{OFF} directly.

Bipolar Calibration

Bipolar calibration is similar to unipolar calibration. First, a signal +1/2LSB above negative full scale (−4.9805V) for the ±5V input range) is applied to R_3 and potentiometer R_1 is trimmed to give the first transition (0000 0000 to 0000 0001). Then a signal 1 1/2LSB below positive full scale (+4.9941V) is applied and potentiometer R_2 trimmed to give the last transition (1111 1110 to 1111 1111).

Offset and gain calibration can be more accurately trimmed by summing a small triangular wave voltage to the analog input signal, and the digital outputs monitored to determine the center point of the code transition.

Driving the Am6108/6148

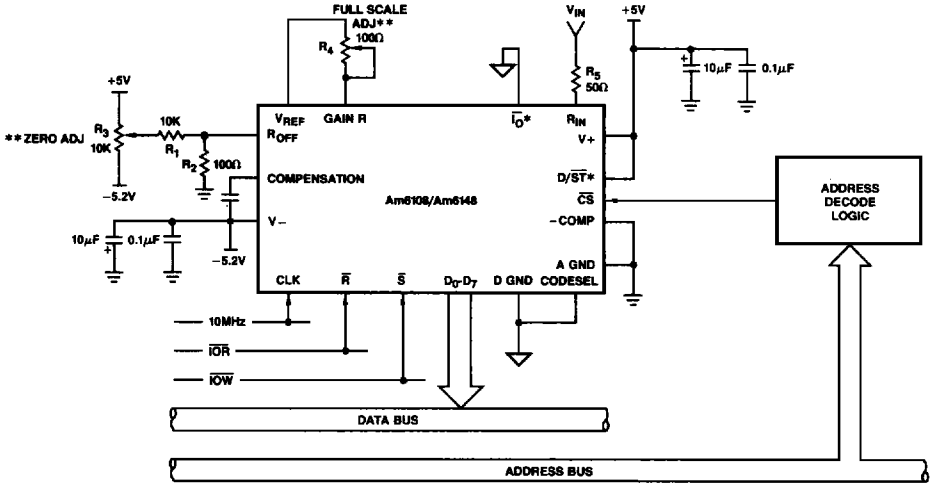
TheAm6108/6148 is a successive approximation type analog-to-digital converter. During the conversion cycle, the A/D input current is modulated by the DC test current at the A/D clock frequency. Thus, it is important to recognize that the signal source driving the Am6108/6148 must be capable of holding a constant output voltage under dynamically-changing load currents. Many operational amplifiers have closed-loop output impedance equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. At high frequencies, where the loop gain is low, the amplifier output impedance rises to its open-loop value. The output of the amplifier may return to its nominal voltage before the converter makes a comparison, so that little or no error is introduced. However, many precision amplifiers have limited bandwidth, which recover very slowly from output transients. The use of wide-band amplifiers is recommended plus a unity-gain buffer included inside the amplifier's feedback loop.

Supplying Decoupling and Layout Considerations

The Am6108/6148 is built using a very high frequency bipolar process, it is very important that the power supplies be filtered, well regulated and free from high frequency noise. Switching power supplies are not recommended because of the switching spikes present. Decoupling of the supplies with 10μF tantalum in parallel with 0.1μF disc ceramic type capacitors is recommended. If the supplies are still noisy then further filtering can be achieved by inserting low value series resistors (metal film) between the supplies and the decoupling capacitors.

Circuit layout should attempt to keep analog circuitry of the Am6108/6148 and associated components as far away from logic interconnections as possible. The analog ground (A GND) is the ground point for the internal reference, D/A converter and comparator and should be a "high quality" ground. In most cases, the A. GND and D. GND can be connected together at the package, but in some situations, the D. GND can be connected to the most convenient ground, and the A. GND to the analog power return.

Figure 2. Am6108/Am6148 Unipolar Configuration



*Function available on the Am6108 only. **See application information.

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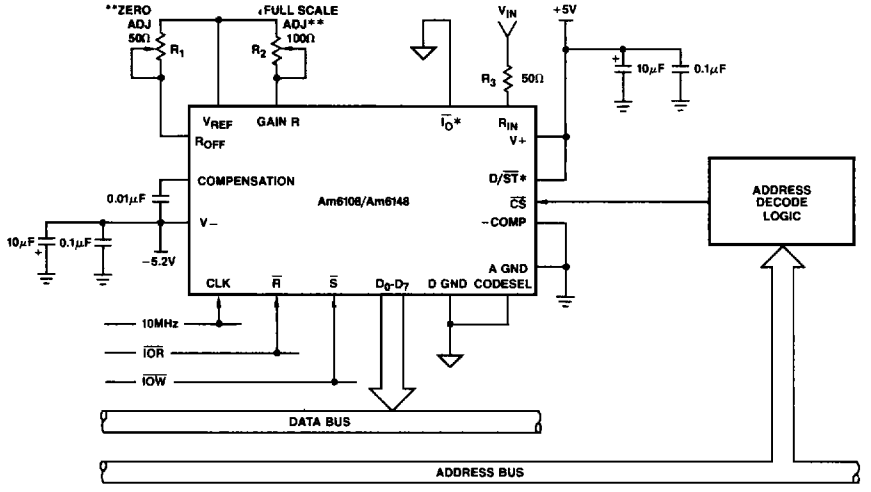
Figure 3. Am6108/Am6148 Bipolar Configuration



*Function available on the Am6108 only. **See application information.

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Figure 4. Am6108/Am6148 $\overline{CC}$ to Microprocessor RDY Interface

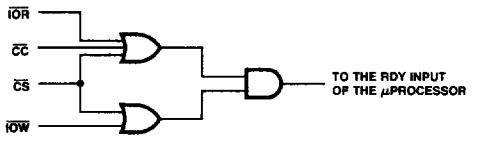

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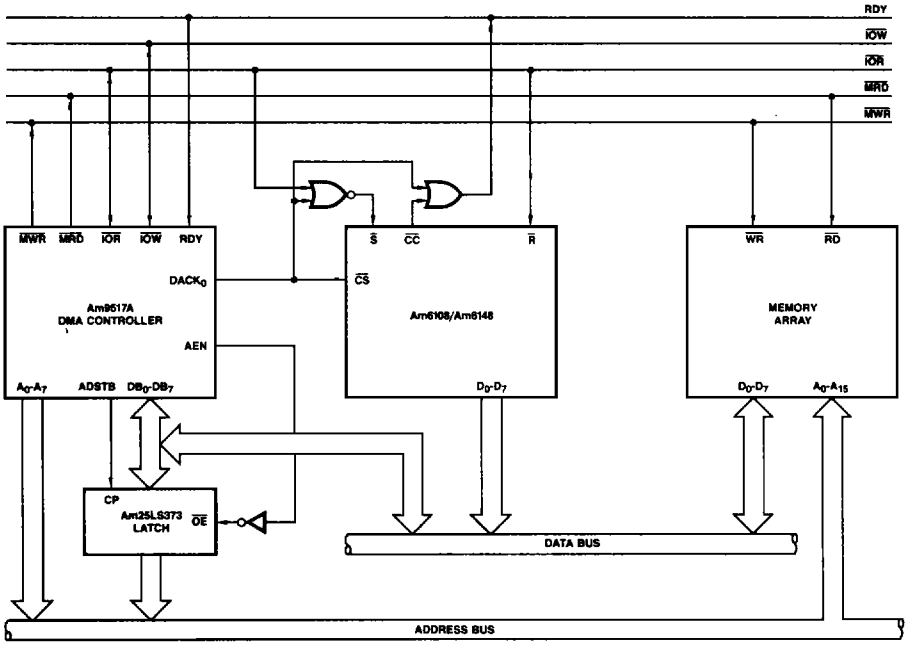
Figure 5. Am6108/Am6148 DMA Configuration



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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
Am6108DC	D-28-1	C	C-1
Am6148DC	D-24-SLIM	C	C-1

Notes: 1. D = Hermetic DIP. Number following letter is number of leads.
2. C = 0 to +70°C.
3. Level C-1 conforms to MIL-STD-883, Class C.