LSI/CSI
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LS7030

Revised October 1990

EIGHT DECADE MULTIPLEXED MOS UP COUNTER

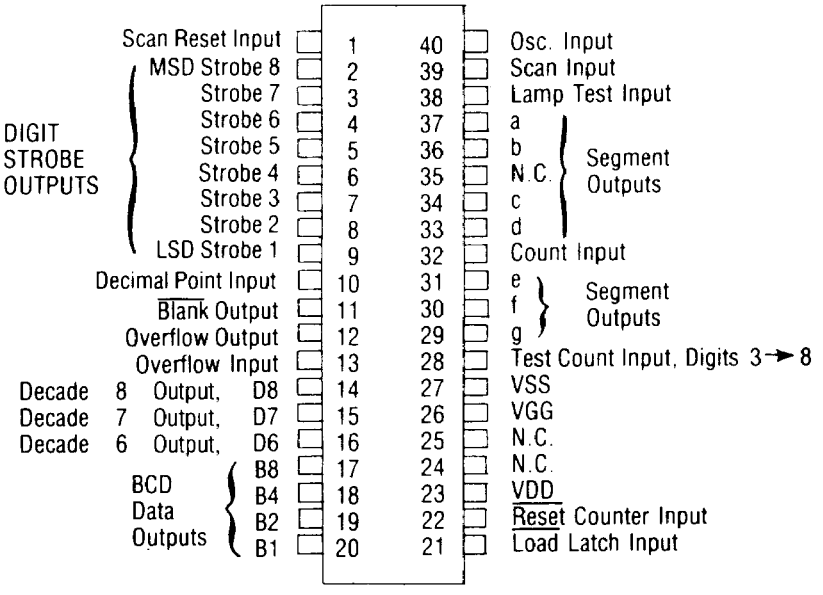
FEATURES:

- DC to 7.5MHz Count Frequency
- Multiplexed BCD and 7 Segment Outputs
- DC to 500 KHz Scan Frequency
- Single Power Supply Operation, +4.75VDC to +15VDC
- Compatible with CMOS Logic
- High Input Noise Immunity
- Counter Output Latches
- Leading Zero Blanking
- Low Power Dissipation
- All Inputs Protected

DESCRIPTION:

The LS7030 is a monolithic, ion implanted, 8 decade up counter. The circuit includes latches, multiplexer, leading zero blanking, BCD and 7 segment data outputs.

CONNECTION DIAGRAM:



OPERATING DESCRIPTION:

8 DECADE UP COUNTER

The eight decade ripple through counter increments on the negative edge of the input count pulse. Maximum ripple time is 12 μs (99999999 to 00000000). Maximum count frequency is 7.5MHz.

RESET

All decades are reset to zero when $\overline{\text{Reset}}$ input is brought low for minimum of 4 μs. The Overflow flip flop is reset at the same time. $\overline{\text{Reset}}$ must be high for a minimum of 1 μs before next valid count can be recorded.

LATCHES

Contents of counter are transferred to latches when $\overline{\text{Load}}$ signal is brought low for a minimum of 4 μs and kept low until a minimum of 12 μs has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when $\overline{\text{Load}}$ signal is high for a minimum of 1 μs before next negative edge of count pulse or reset. Data is transferred from Overflow flip-flop to Overflow latch at the same time.

NOTE

The LS7030-1 is a selected higher count frequency version of the LS7030. The specification differences occur under DYNAMIC ELECTRICAL CHARACTERISTICS as follows:

PARAMETER	SYMBOL	MIN	MAX	UNITS
Count and Test Count Frequency				
(VSS = + 5V ± 5%)	Fc, Fac	DC	10	MHz
(VSS = + 10V)	Fc, Fac	DC	7.5	MHz
(VSS = + 15V)	Fc, Fac	DC	6	MHz
Count Pulse Width				
(VSS = + 5V ± 5%)	Tcpw	50		ns
(VSS = + 10V)	Tcpw	62		ns
(VSS = + 15V)	Tcpw	83		ns

Other specifications are unchanged.

SCAN OSCILLATOR AND COUNTER

The scan counter is driven by an internal oscillator whose frequency is determined by a capacitor connected between Oscillator input and Scan input. An external scan clock applied to Scan input can also drive the scan counter. Scan counter advances on negative edge of scan clock.
The counter scans from **MSD** to LSD. When Scan Reset input is brought high the scan counter is forced to MSD state. Internal synchronization guarantees proper scanning no matter when Scan Reset is brought low relative to scan clock. Maximum scan frequency is 500 KHz.

DIGIT STROBES

Timing of Digit Strobes is arranged such that both edges of strobe are guardbanded by a minimum 400 ns within valid BCD data when scan frequency is 100 KHz or less. The guardband is a minimum of 200 ns at 250 KHz scan frequency. At 500 KHz only negative edge of Strobe is guaranteed to be within valid BCD data by a minimum 200 ns.

DECIMAL POINT

A high at the Decimal Point input resets the Blanking Flip Flop causing the display to unblank. Decimal Point should be brought high at start of digit time which has active Decimal Point.

OVERFLOW

The Overflow flip flop sets on the first negative transition of the Overflow Input and remains set until Reset is brought low. Data is transferred from Overflow flip flop to Overflow Latch when Load is brought low. A high at the Overflow Latch causes display to unblank. Overflow Output is output of Overflow Latch. MSB outputs of Decades 6, 7, 8 are available for use as Overflow Input.

BLANKING

Leading zero blanking is employed. At start of each MSD to LSD scan, display is blanked until a nonzero digit or active decimal point is encountered. Display unblanks during LSD time and for a whole scan when Overflow output is high. When Scan Reset is applied, display blanks to prevent display damage.

Blanking information is available at Blank output and is incorporated into 7 segment information.

BCD AND 7 SEGMENT DATA

Data is available in BCD and 7 segment format. BCD data can readily be demultiplexed using Digit Strobes as latch enable signals.

POWER SUPPLIES

+4.75 volts to +15 volts single power supply operation is obtained when VGG and VDD are tied together. Inputs and outputs are CMOS compatible and Minimum Input Noise Immunity of 25% of power supply is guaranteed except for Test Count Input. (Inputs are TTL compatible at +4.75 volt to +5.25 operation.)

With VGG at −12V, VDD at OV and VSS at +5V all inputs are TTL and CMOS compatible. All outputs are CMOS compatible and BCD and BLANK outputs also provide standard TTL compatibility. In addition. Overflow Output is low power TTL compatible.
In either mode outputs swing between VDD and VSS.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	Tstg	−65 to +150	°C
Operating Temperature	Ta	−25 to +70	°C
Voltage (any pin to VSS)	Vmax	−30 to +0.5	V

DC ELECTRICAL CHARACTERISTICS:

(VDD = VGG = OV, VSS = +4.75 to +15V, −25°C ≤ Ta ≤ +70°C unless otherwise specified.)

	PARAMETER	SYMBOL	MIN	MAX	UNITS
	Operating Supply Current (@ FC =7.5MHz)	Idds		15	mA
	Input Noise Immunity Low and High	Vni	25% (VSS-VDD)		V
	Test Count Input	Vil	VSS-20	VSS-3.95	V
		Vih	VSS-1.0	VSS	V
D6, D7, D8 OF, BCD, Blank (See Note 1)	Output Voltage "0"	Vol		+0.2	V
	Output Voltage "1"	Voh	VSS-1.0		V
Segment and Strobe Outputs (See Note 2)	Output Voltage "0" (sinking 10 uA)	Vol		+0.5	V
	Output Current "1"				
	VSS=+4.75 (Voh=VSS−0.5V)		0.05		mA
	(Voh=VSS−1V)		0.25		mA
	(Voh=VSS−4V)		0.90		mA
	VSS=+10V (Voh=VSS−2V)		2.0		mA
	(Voh=VSS−3V)		3.0		mA
	VSS=+15V (Voh=VSS−2V)		3.0		mA
	(Voh=VSS−3V)		4.5		mA

Note 1: Current Sink = Same as segment and strobe outputs.
Current Source = N/A at Voh = VSS−.5V for VSS =+4.75V
35μA at Voh = VSS−1V for VSS = +4.75V
40% of segment and strobe outputs at all other specified operating points.

Note 2: Limit segment current to 4.5mA maximum.
Limit strobe current to 6mA maximum.

Note: The following inputs have internal pull down resistors to VDD with maximum sink current of 5 μA at VSS input.

Scan Reset	Test Count
Decimal Point	Count
Overflow	Lamp Test

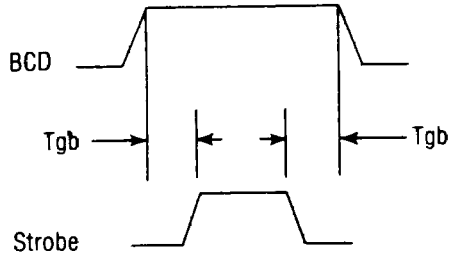
DYNAMIC ELECTRICAL CHARACTERISTICS:

(VDD = VGG = 0V, VSS = +4.75 to+15V. −25°C ≤ Ta ≤ +70°C unless otherwise specified.)

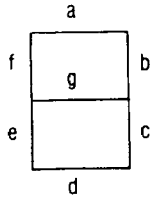
PARAMETER	SYMBOL	MIN	MAX	UNITS
Count and Test Count Frequency				
(VSS = + 5V ± 5%)	Fc, Ftc	DC	7.5	MHz
(VSS = + 10V)	Fc, Ftc	DC	6	MHz
(VSS = + 15V)	Fc, Ftc	DC	5	MHZ
Scan Frequency	Fsc	DC	500	KHz
Count Pulse Width				
(VSS = + 5V ± 5%	Tcpw	66		ns
(VSS = + 10V)	Tcpw	83		ns
(VSS = + 15V)	Tcpw	100		ns
Count Ripple Time	Tcr		12	μs
$\overline{\text{Load}}$ Pulse Width	Tlpw	4		μs
$\overline{\text{Load}}$ Removal Time	Tlr		1	μs
$\overline{\text{Reset}}$ Pulse Width	Trpw	4		μs
$\overline{\text{Reset}}$ Removal Time	Trr		1	μs
Rise and Fall Time				
Count Pulse	Trfc		4	μs
Reset Pulse	Trfr		4	μs
Test Count Pulse	Trftc		80	μs
*Strobe Guard Band Time (Fsc ≤100 kHz)	Tgb	400		ns
*Strobe Guard Band Time (100 kHz ≤Fsc ≤250 kHz)	Tgb	200		ns
*Strobe Guard Band Time (250 kHz ≤Fsc ≤ 500 kHz) negative edge only	Tgb	200		ns

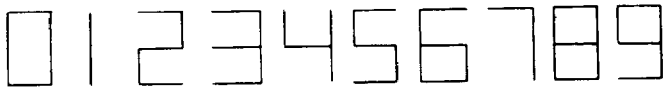
*Defines the minimum time from strobe edges to switching BCD data.

Guardbanded Strobe



Seven Segment Font





SCAN OSCILLATOR:

CAPACITANCE	TYPICAL OSCILLATOR FREQUENC		
	4.75V	10V.	15V
50pf	40.0 KHz	24.2 KHz	22.2 KHz
100pf	22.2 KHz	14.8 KHz	13.8 KHz
470pf	5.0 KHz	3.6 KHz	3.5 KHz
750pf	3.3 KHz	2.4 KHz	2.2 KHz
2000pf	1.3 KHz	.91 KHz	.85 KHz

TTL COMPATIBLE OUTPUTS:

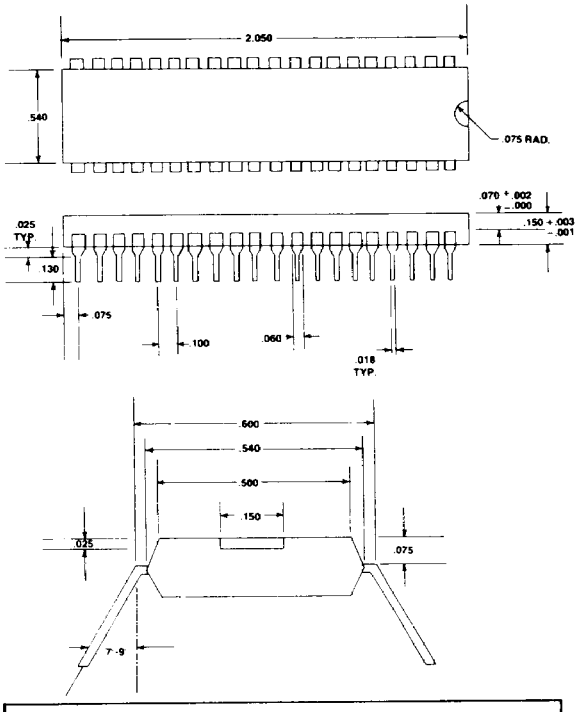
Power Supplies: VSS = +5V ±5%
VDD = 0V
VGG = −12V ±5%

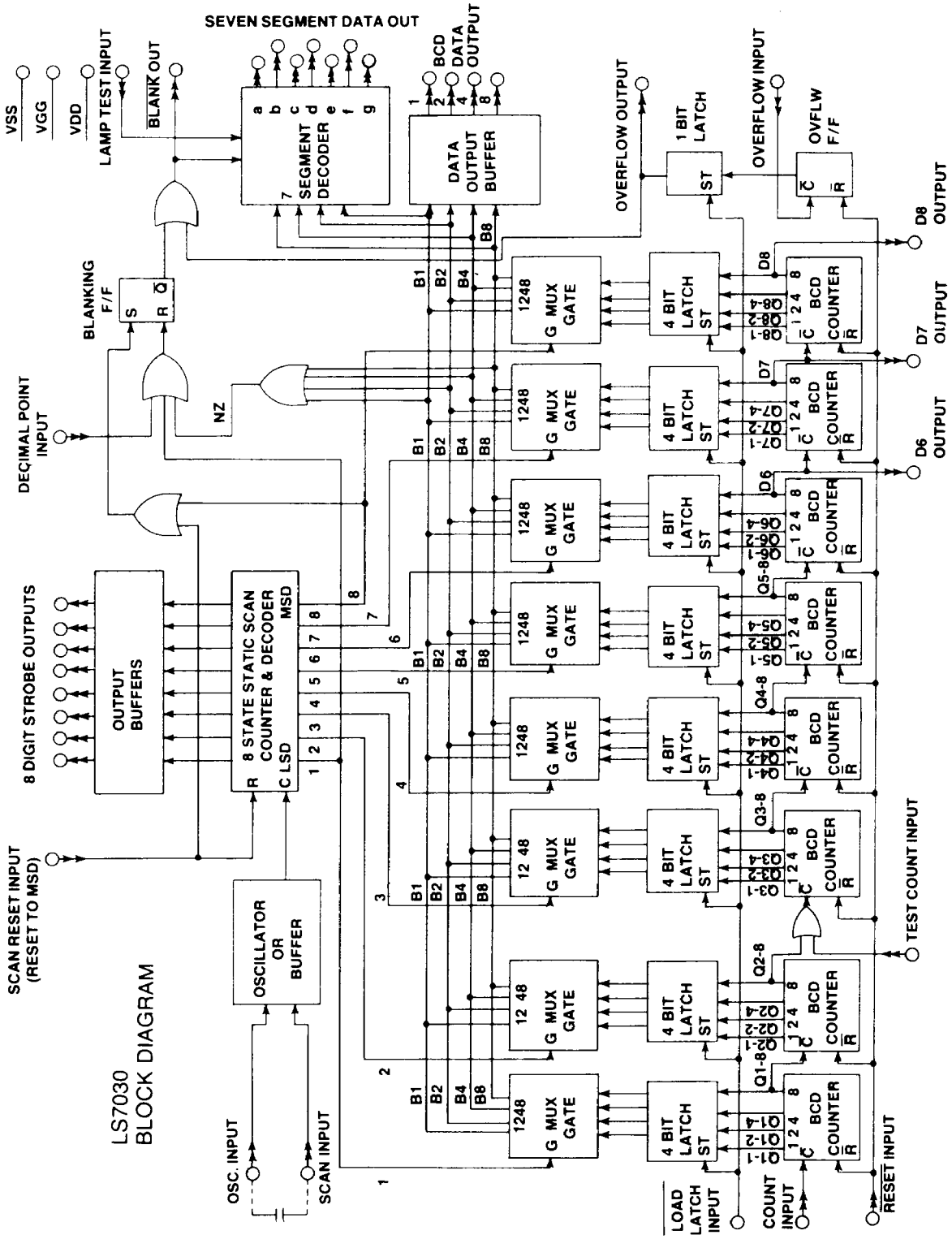
Output Levels:
"1" level ≥ VSS − 5V (sourcing 100 μA)
"0" level ≤ 0.4V (sinking 1.6mA)
} $\overline{\text{BLANK}}$ AND BCD DATA OUTPUTS

"1" level ≥ VSS − 5V (sourcing 40μA)
"0" level ≤ 0.4V (sinking .18mA)
} OVERFLOW OUTPUT

All other outputs as specified for single power supply, VSS = +15V, operation. Inputs as specified for single power supply, VSS = +5V ±5% operation.

PACKAGE DIAGRAM:




SEVEN SEGMENT DATA OUT
VSS
VGG
VDD
LAMP TEST INPUT
BLANK OUT
BCD DATA OUTPUT
SEGMENT DECODER
DATA OUTPUT BUFFER
OVERFLOW OUTPUT
1 BIT LATCH
OVERFLOW INPUT
OVFLW F/F
BLANKING F/F
DECIMAL POINT INPUT
NZ
G MUX GATE
4 BIT LATCH
BCD COUNTER
D8 OUTPUT
D7 OUTPUT
D6 OUTPUT
8 DIGIT STROBE OUTPUTS
OUTPUT BUFFERS
8 STATE STATIC SCAN COUNTER & DECODER
MSD
LSD
SCAN RESET INPUT (RESET TO MSD)
OSCILLATOR OR BUFFER
TEST COUNT INPUT
OSC. INPUT
SCAN INPUT
LOAD LATCH INPUT
COUNT INPUT
RESET INPUT
LS7030
BLOCK DIAGRAM