iSM001DR09P (9-CHIP)
1M x 9 (1,048,576 x 9) DYNAMIC RAM MEMORY MODULE WITH FAST PAGE MODE

(Formerly Known as 21019)

■ Performance Range

Symbol	Parameter	iSM001DR09P		Units
		-70	-80	
t_{RAC}	Access Time from $\overline{RAS}$	70	80	ns
t_{CAC}	Access Time from $\overline{CAS}$	20	25	ns
t_{RC}	Read Cycle Time	130	160	ns

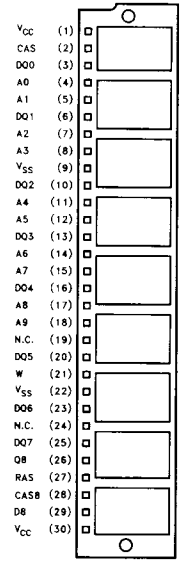
- **9-Chip Version**
- **1,048,576 x 9-Bit Organization**
- **Fast Page Mode Operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **JEDEC Standard Pin-Out in a 30-Pin Single In-Line Memory Module (SIMM)**
- **Single +5V (±10%) Power Supply**
- **512 Refresh Cycles every 8 ms**
- **Separate $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ ($\overline{CAS8}$) Control for One Separate Pair of Data-In and Data-Out Lines**
- **TTL Compatible Inputs and Outputs**

Intel's iSM001DR09P is a 1,048,576 words by 9-bit memory module consisting of nine industry standard 1M x 1 dynamic RAMs in SOJ packages.

The 20 address bits are entered 10 bits at a time using $\overline{RAS}$ to latch the first 10 bits and $\overline{CAS}$ to control the latter 10 bits. The ninth data input/output bit D8, Q8 is generally used for parity and is controlled by $\overline{CAS8}$.

The common I/O feature requires the use of an early write cycle to prevent data contention on DQ lines.

1M x 9 (9-Chip) SIMM



240721-1

Figure 1. Pin Configuration

Pin Names

A0–A9	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
D8	Data Input
Q8	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{CAS8}$	Column Address Strobe
$\overline{W}$	R/W Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

August 1991
Order Number: 240721-005

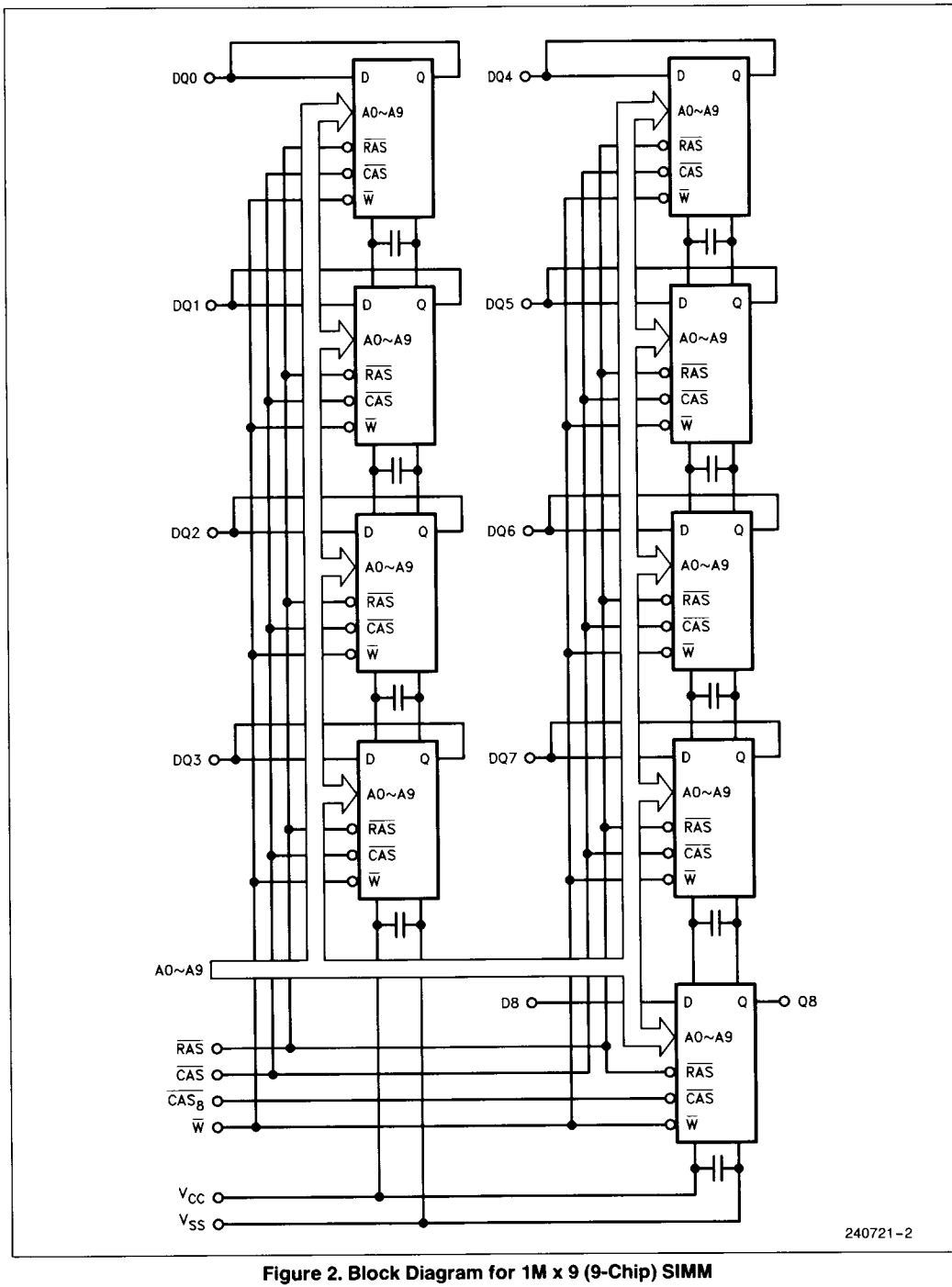


Figure 2. Block Diagram for 1M x 9 (9-Chip) SIMM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V
Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V
Storage Temperature (T_{STG}) .... −55°C to +125°C
Soldering Temperature • Time (T_{solder}) ..... 260°C • 10 Sec
Power Dissipation (P_d) 9W
Short Circuit Output Current (I_{OUT}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage Referenced to V_{SS}. T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_I (A)	Input Capacitance (A0–A9)		75	pF
C_{DQ}	I/O Capacitance		20	pF
C_I ($\overline{W}$)	Input Capacitance, Write Control Input		75	pF
C_I ($\overline{RAS}$)	Input Capacitance, $\overline{RAS}$ Input		75	pF
C_I ($\overline{CAS}$)	Input Capacitance, $\overline{CAS}$ Input		75	pF
C_I ($\overline{CAS8}$)	Input Capacitance, $\overline{CAS8}$ Input		20	pF
C_I (DP)	Input Capacitance		15	pF
C_O (QP)	Output Capacitance		15	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Symbol	Parameter		Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−70 −80		720 630	mA
I_{CC2}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}			18	mA
		$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} −0.2V			9	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = Min)		−70 −80		720 630	mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ t_{PC} = Min)		−70 −80		630 450	mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−70 −80		720 630	mA
I_{IL}	Input Current (Any Input 0 ≤ V_{IN} ≤ 6.5V All Other Pins = 0V)			−90	90	μA
I_{OZ}	Off State Output Current (Data Out is Disabled and 0 ≤ V_{OUT} ≤ 5.5V)			−20	20	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)			2.4	V_{CC}	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)			0	0.4	V

NOTE:

I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

AC CHARACTERISTICS[1, 2, 3] (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	iSM001DR09P				Units	Notes
		-70		-80			
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$		70		80	ns	4, 7
t_{CAC}	Access Time from $\overline{CAS}$		20		25	ns	5, 7
t_{CAA}	Access Time from Column Address		35		40	ns	6, 7
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40	ns	7, 14
t_{CLZ}	Output Low Impedance Time from $\overline{CAS}$ Low	0		0		ns	7
t_{OFF}	Output Disable Time after $\overline{CAS}$ High	0	20	0	20	ns	8
t_{REF}	Refresh Cycle Time		8		8	ms	
t_T	Transition Time	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ High Pulse Width	50		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	55	ns	9, 10
t_{CPN}	$\overline{CAS}$ High Pulse Width	35		35		ns	
t_{RAD}	Column Address Delay Time from $\overline{RAS}$ Low	17	35	20	40	ns	11
t_{ASR}	Row Address Setup Time before $\overline{RAS}$ Low	0		0		ns	
t_{ASC}	Column Address Time before $\overline{CAS}$ Low	0		0		ns	
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ LOW	10		15		ns	
t_{CAH}	Column Address Hold Time after $\overline{CAS}$ Low or $\overline{W}$ Low	15		20		ns	
t_{AR}	Column Address Hold Referenced to $\overline{RAS}$	55		65		ns	
t_{DHR}	Data In Hold Referenced to $\overline{RAS}$	55		65		ns	
t_{RC}	Read Cycle Time	130		160		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	70	10K	80	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	70		80		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		25		ns	
t_{RCS}	Read Setup Time before $\overline{CAS}$ Low	0		0		ns	
t_{RCH}	Read Hold Time after $\overline{CAS}$ High	0		0		ns	12
t_{RRH}	Read Hold Time after $\overline{RAS}$ High	10		10		ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Setup Time	35		40		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		ns	

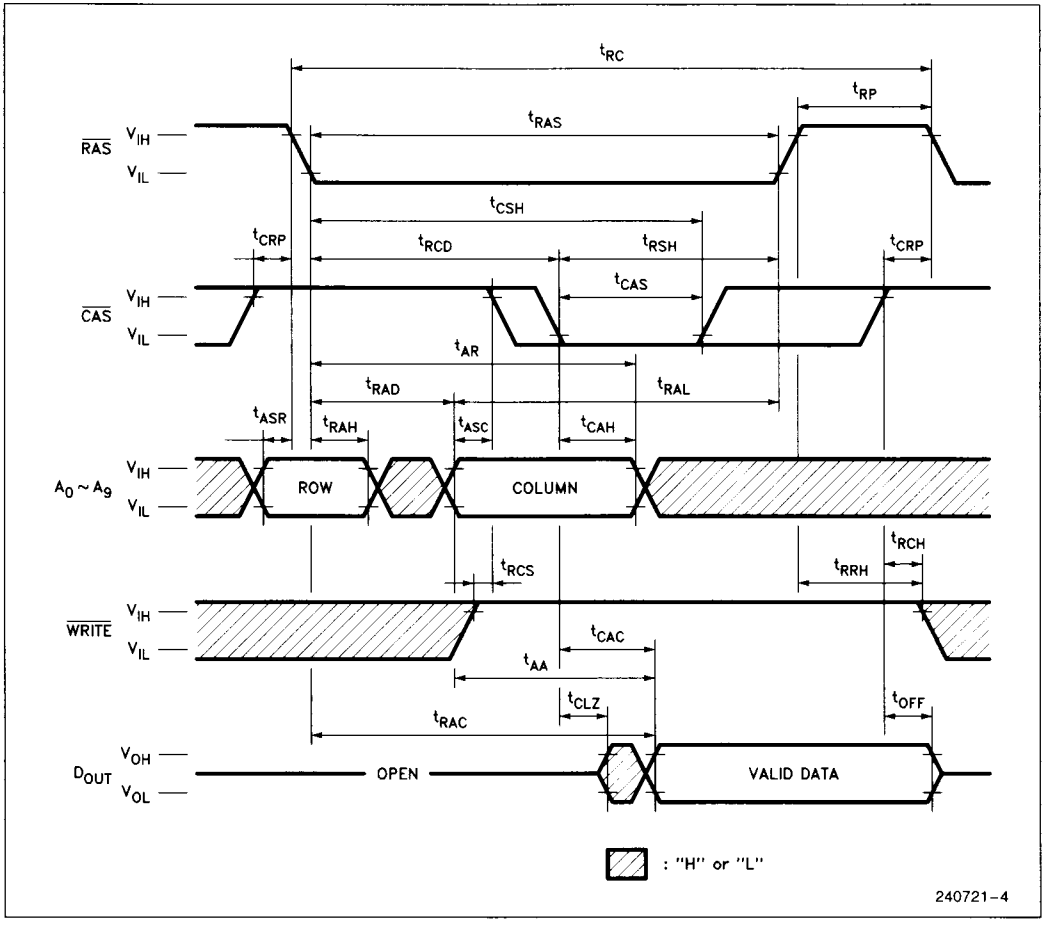
AC CHARACTERISTICS[1, 2, 3] (T_A = 0°C to 70°C, V_{CC} = 5V ±10%) (Continued)

Symbol	Parameter	iSM001DR09P				Units	Notes
		-70		-80			
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	20		25		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	40		40		ns	
t_{DS}	Data Setup Time	0		0		ns	
t_{DH}	Data Hold Time after $\overline{CAS}$ Low	15		20		ns	
t_{WCS}	Write Setup Time before $\overline{CAS}$ Low	0		0		ns	13
t_{WCH}	Write Hold Time after $\overline{CAS}$ Low	15		20		ns	
t_{WP}	Write Pulse Width	15		15		ns	
t_{WCR}	Write Command Hold Referenced to $\overline{RAS}$	55		60		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100K	80	100K	ns	
t_{PC}	Fast Page Mode Cycle Time	50		55		ns	
t_{CP}	$\overline{CAS}$ High Pulse Width	10		10		ns	

NOTES:
1. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. Characteristics assume t_T = 5 ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}(max)$, $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}(max)$, $t_{RAD} \geq t_{RAD}(max)$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}(max)$ and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. $t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H").

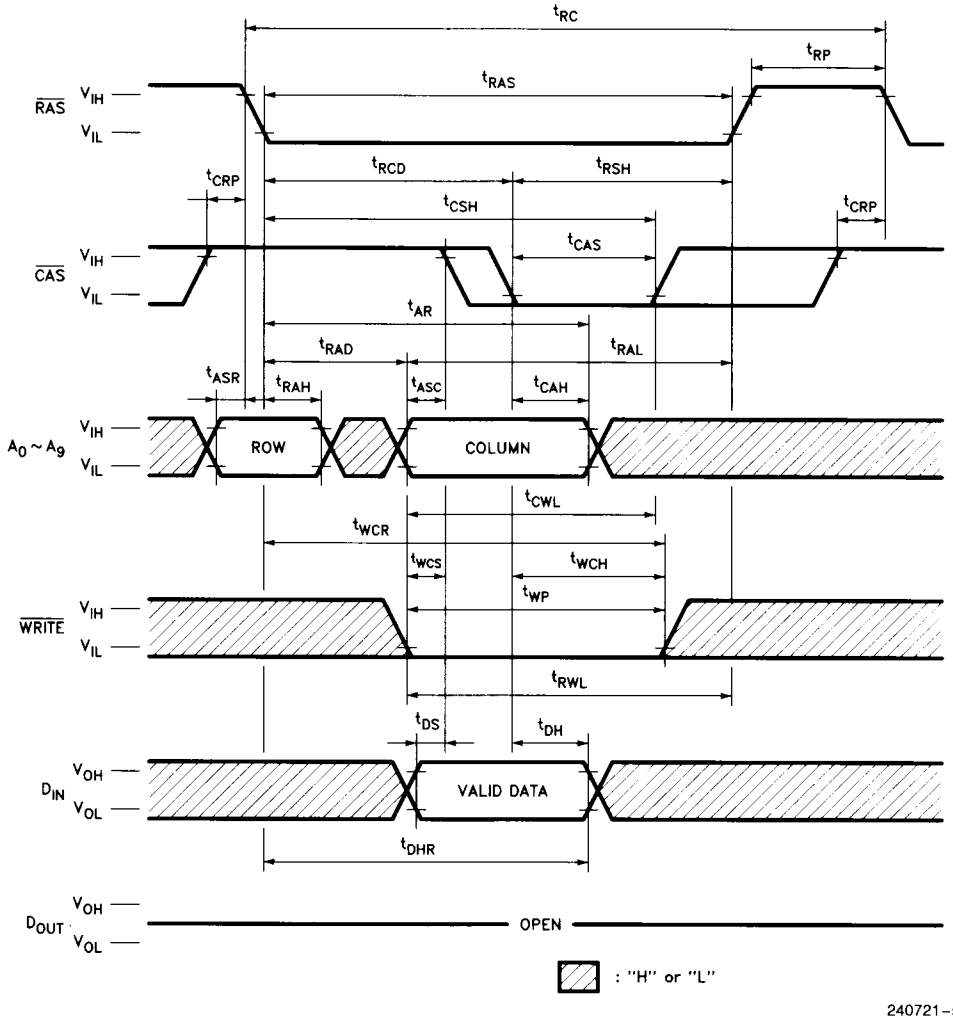
TIMING DIAGRAMS

READ CYCLE



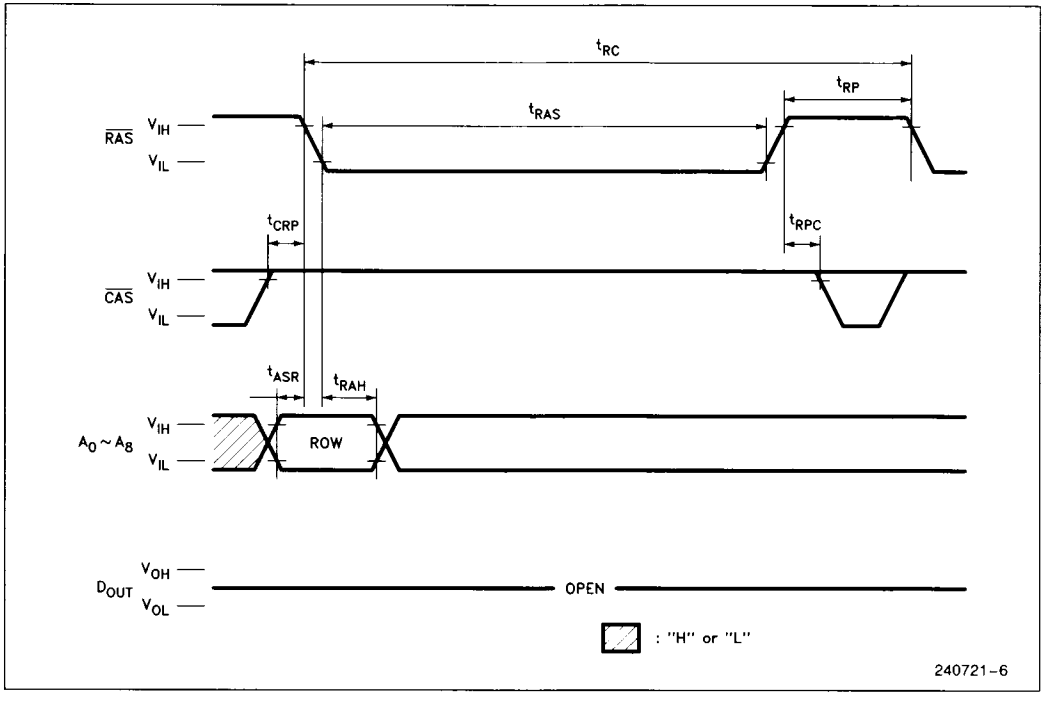
TIMING DIAGRAMS (Continued)

EARLY WRITE CYCLE

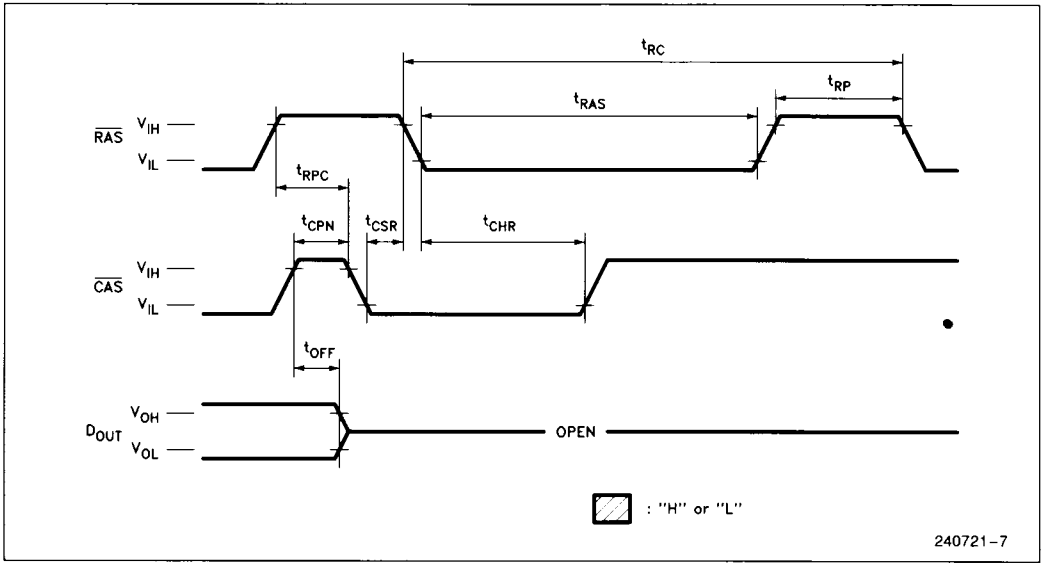


TIMING DIAGRAMS (Continued)

$\overline{RAS}$ ONLY REFRESH CYCLE

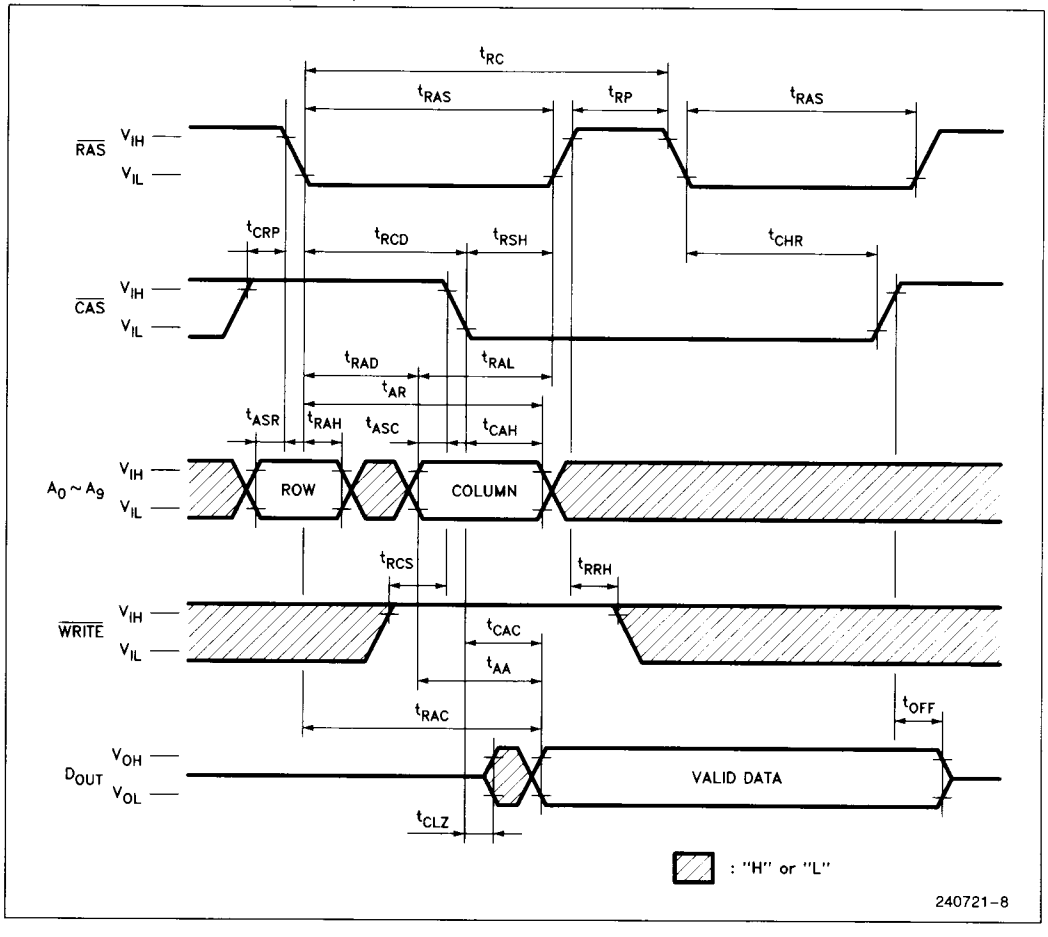


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



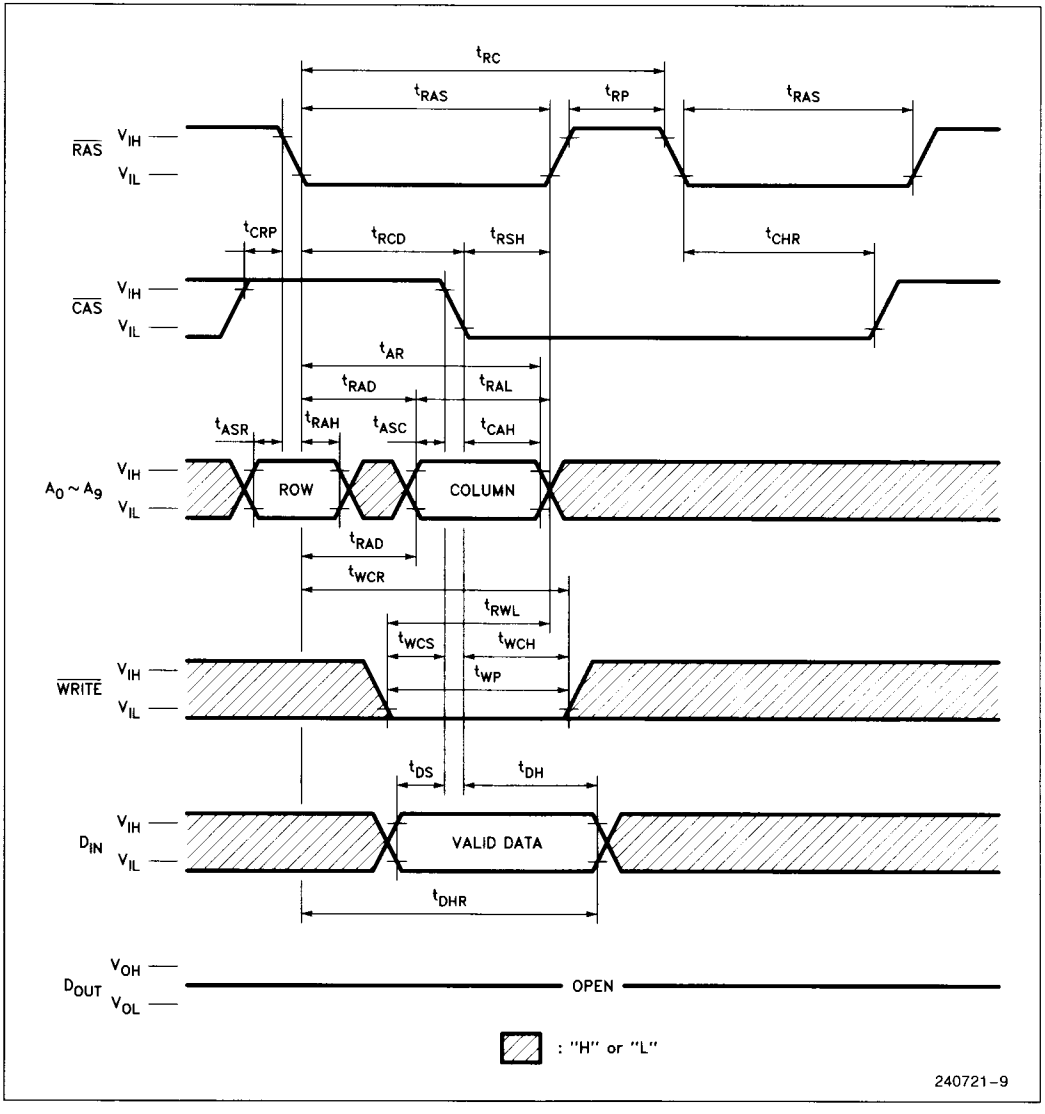
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



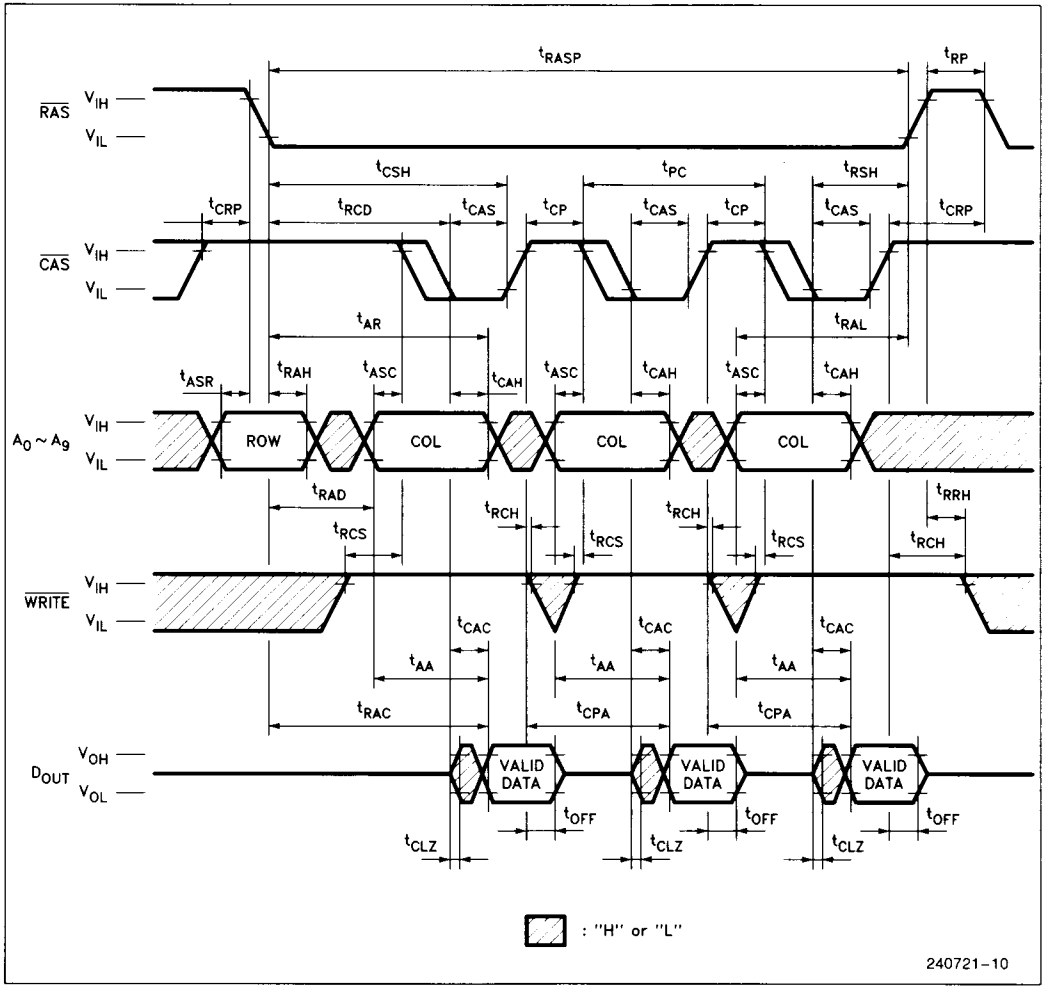
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (WRITE)



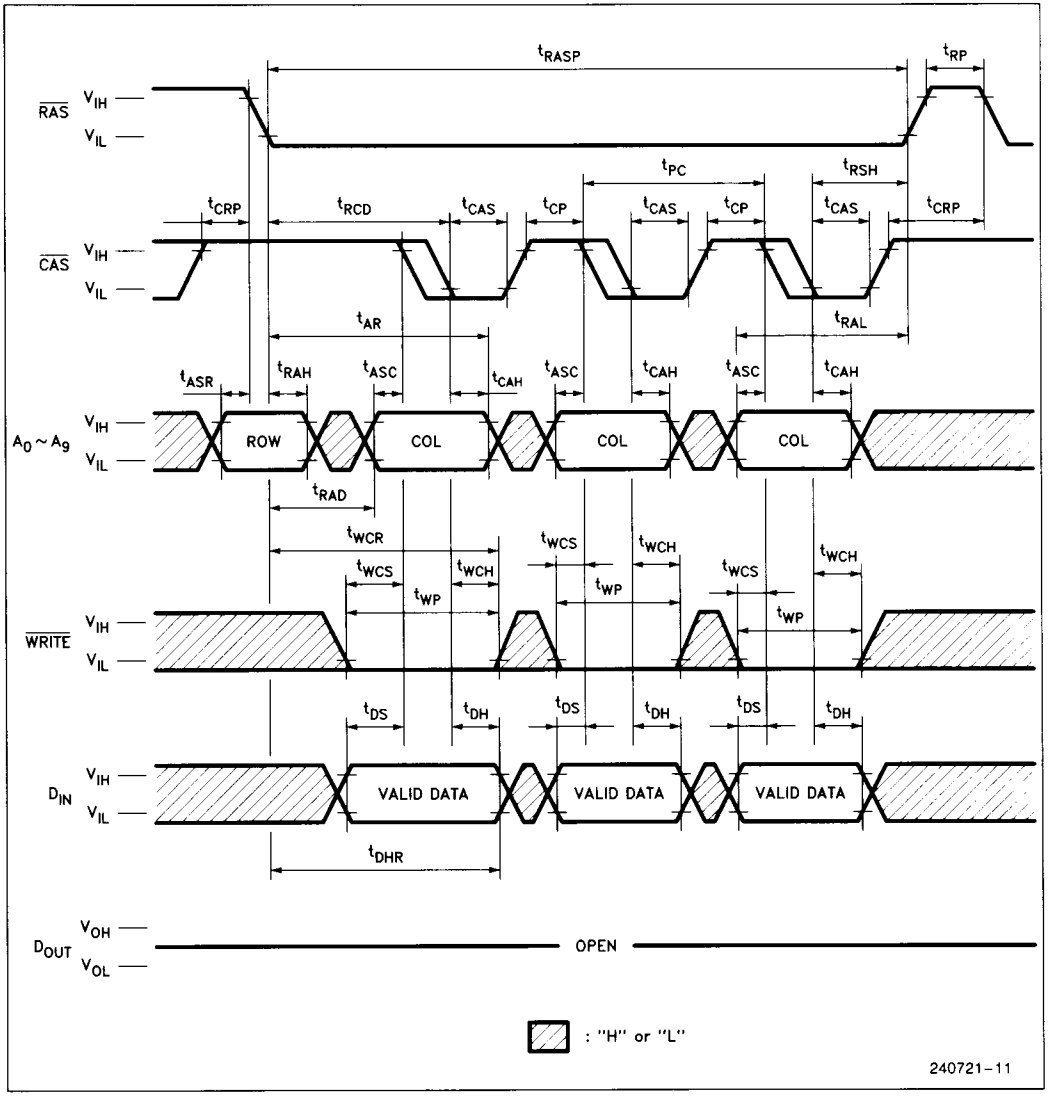
TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



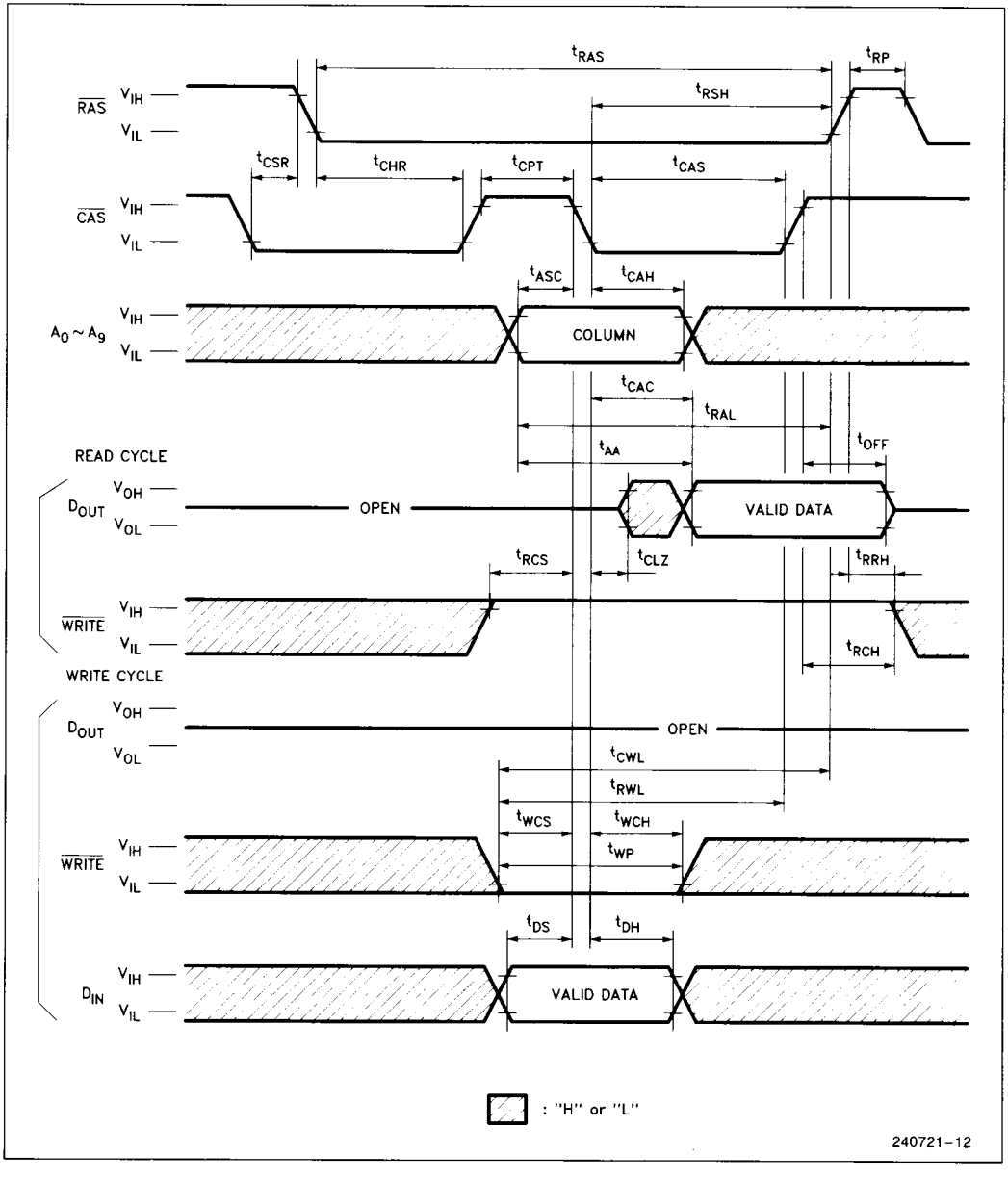
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSIONS

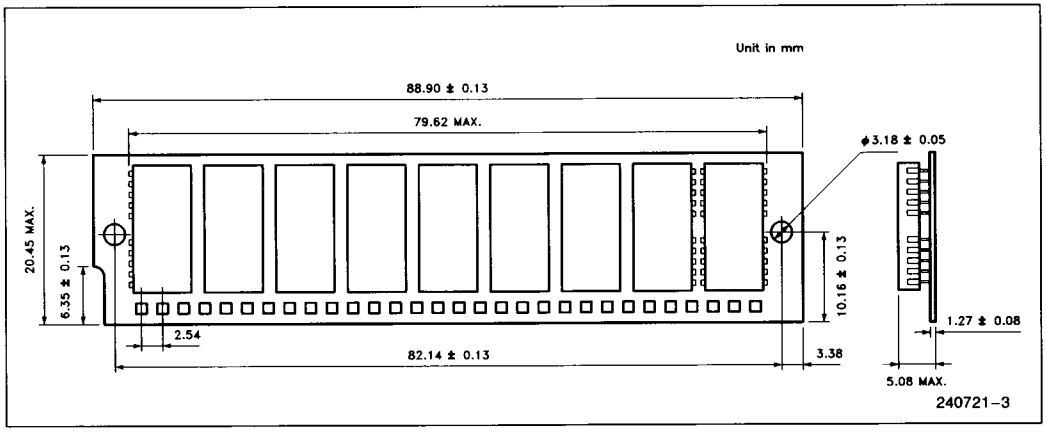


Figure 3. 30-Pin Single In-Line Leadless Memory Module (9-Chip) SIMM

REVISION SUMMARY

1. Deleted 3-chip version. (See Literature Order Number 241190-001 for specifications on that version.)
2. Updated AC Characteristics.