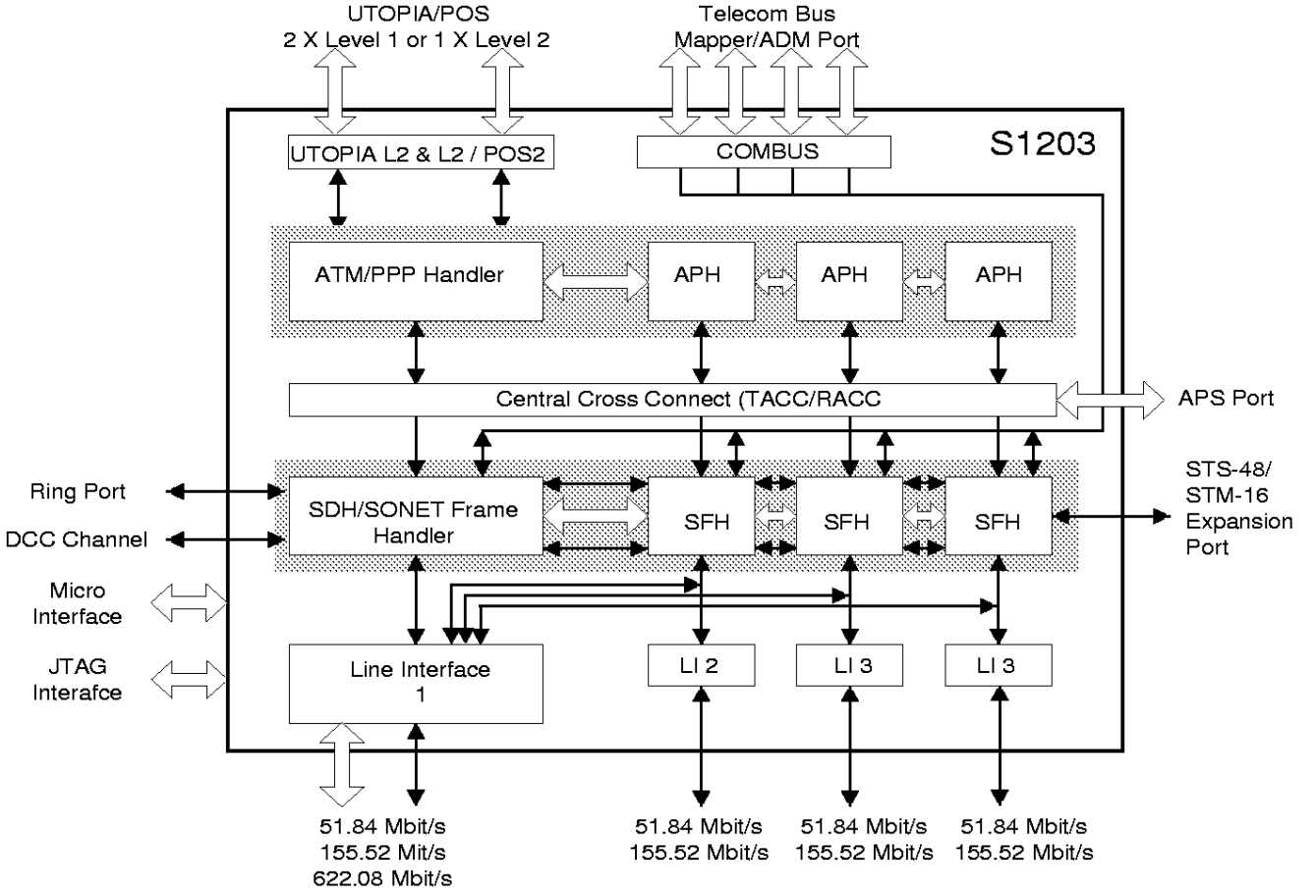
# EXPLORER

*SUMMARY DATASHEET*

## MULTIRATE POS/ATM SONET MAPPER FOR OC-48/12/3/1

### Features

- Complies with ANSI, Bellcore and ITU-T specifications for Jitter Tolerance, Jitter Transfer and Jitter Generation
- On chip high frequency PLL's for clock recovery and clock synthesis, supporting SONET/SDH rates for OC-12, QUAD OC-3 and QUAD OC-1
- Selectable reference frequencies of 19.44, 77.76, 38.88 or 155.52 MHz for CDR and CSU
- LVTTL and Differential PECL Interface
- Processes SONET/SDH STS-12c/(STM-4/AU-4-4c) STS-3(3c)/(STM-1/AU-4c or AU-3 mapped) or STS-1 data streams with full duplex mapping of ATM cells or packets into SONET/SDH payloads.
- Terminates and generates SONET/SDH section, line, and path layers, with transport/section E1, E2, F1 and DCC overhead serial interfaces in both transmit and receive directions.
- Provides a UTOPIA Level2/Level1 - operating at 50 MHz, on the System Side.
- Provides COMBUS interface to industry standard PDH mappers for T1, E1 and DS-3 applications
- Provides cross-connect for STS-1, STS-3 and STS-12 streams
- Provides APS port for 1:n systems
- Provides Expansion port for STS-48/STM-16 applications
- Selectable scrambling/descrambling ($1+X^6+X^7$) of SONET/SDH frame
- Selectable self-synchronous scramblers, ATM/HDLC processors, for implementing ($X^{43}+1$) polynomial for ATM or Packet over SONET applications.
- Generic 8-bit microprocessor interface for configuration, control, and status monitoring.
- Provides a standard 5 signal IEEE 1149.1 JTAG Test Port for Boundary Scan board test purposes.
- Implemented in CMOS, 3.3V technology.
- 474 pin CBGA package



# S1203 Multirate ATM/POS SONET MAPPER

***SUMMARY DATASHEET***

## Overview and Applications

### SONET Processing

The S1203 implements SONET/SDH processing and full-duplex ATM/POS mapping functions for STS-12/STM-4, STS-3/STM-1 and STS-1 data streams. It supports a single concatenated STS-12(c)/AU-4-4(c) signal within an STS-12/STM-4 and a single concatenated STS-3(c)/AU-4(c) signal within an STS-3/STM-1. A TOH/SOH interface provides direct add/drop capability for E1, E2, F1, and both Section and Line DCC channels. The S1203 also includes a clear channel mode that enables the direct transmission of system payload from the system interface to the line-side interface via the COMBUS. A Cross Connection feature allows the cross connectin of the separate ports or the APS port.

On the transmit side the S1203 generates section, line, and path overhead. Idle cells or flag patterns are generated for rate decoupling the system traffic into the SONET frames. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and generates section, line and path Bit Interleaved Parity (B1/B2/B3) for far-end performance monitoring.

On the receive side the S1203 processes section, line, and path overhead. It performs framing (A1, A2), descrambling, alarm detection, Pointer Interpretation, Bit Interleaved Parity monitoring (B1/B2/B3), and error count accumulation for performance monitoring.

### ATM Processing

When configured for ATM cell processing, the S1203's transmit ATM processor will perform all necessary cell encapsulation including HEC generation, cell payload scrambling ($X^{43}+1$) and idle cell insertion to adapt the cell rate to the SONET/SDH SPE. When receiving data from the line side, it performs cell delineation, Rx header error correction/detection, descrambling, and detects & delets idle cells. Cell statistics are accumulated for performance monitoring.

### Packet/HDLC Processing

When configured for POS mode, the S1203's transmit HDLC processor provides the insertion of HDLC framed packets SONET/SDH SPE. It will perform packet framing, inter-frame fill and Tx FIFO error recovery. In addition, it optionally performs scrambling ($X^{43}+1$), performs transparency processing as required by RFC 1662 and will optionally generate a 16/32 bit FCS.

The receive HDLC processor provides for the extraction of packets from HDLC frames, transparency removal, descrambling (if enabled), FCS error checking, and optionally deletes the HDLC address and control fields.

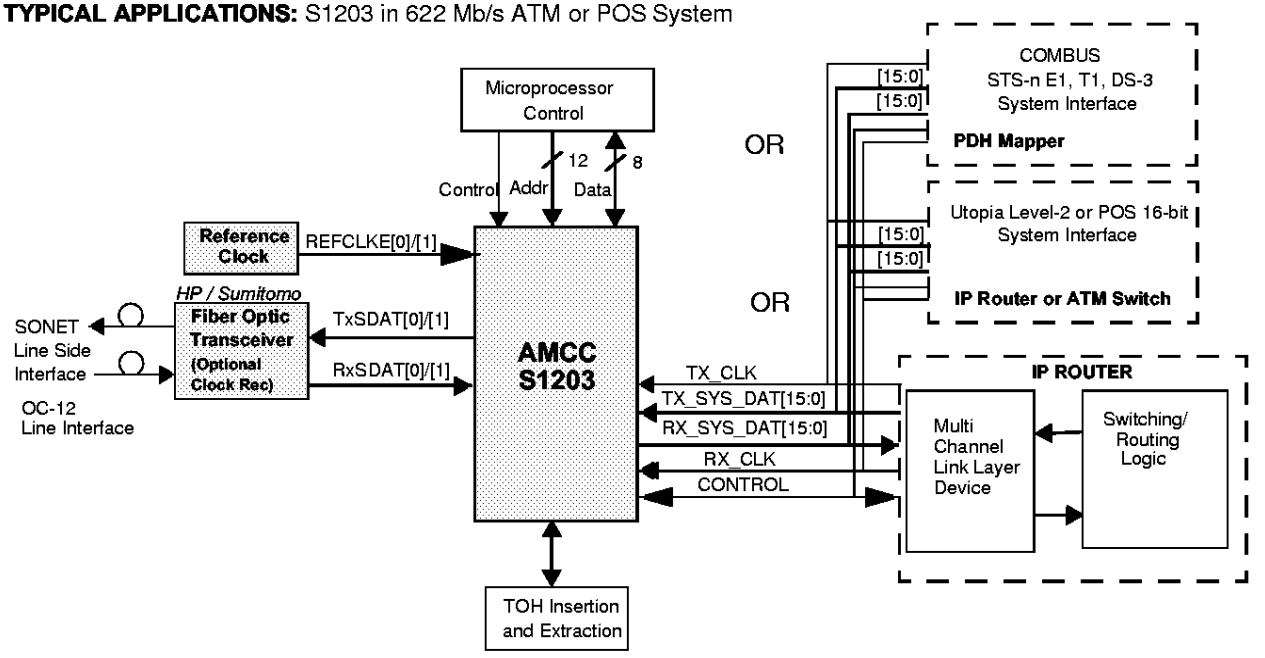
### Line-side Interface

On the line-side, the S1203 supports a serial PECL interface operating at 622MHz. The S1203 is typically connected to an electrical-to-optical converter for interfacing to the fiber optic interface. (See figure below.) The clock recovery function requires a 155, 77.76, 19.44 or 38.88MHz reference clock for phase locked loop startup and proper operation during LOS conditions. In the transmit direction this reference clock is used to synthesize the output data rate and must therefore be less than 20ppm accuracy.

### System Interface

The S1203 supports a UTOPIA level 1 and UTOPIA level 2 50 MHz system interface. When operating in POS mode, the S1203 supports the 16-bit, 500 MHz, Nu-TOPIA interface.

**TYPICAL APPLICATIONS:** S1203 in 622 Mb/s ATM or POS System

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