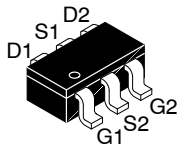
Dual, N & P-Channel, Digital FET

FDC6321C

N−Channel		
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
25 V	0.45 Ω @ 4.5 V	0.68 A

P−Channel		
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
−25 V	1.1 Ω @ −4.5 V	−0.46 A



TSOT23 6−Lead
SUPERSOT™ −6
CASE 419BL

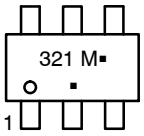
General Description

These dual N & P Channel logic level enhancement mode field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors in load switching applications. Since bias resistors are not required this dual digital FET can replace several digital transistors with different bias resistors.

Features

- N−Channel 0.68 A, 25 V
  $R_{DS(ON)}$ = 0.45 Ω @ V_{GS} = 4.5 V
- P−Channel −0.46 A, −25 V
  $R_{DS(ON)}$ = 1.1 Ω @ V_{GS} = −4.5 V
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits. $V_{GS(th)}$ < 1.0 V.
- Gate−Source Zener for ESD Ruggedness. >6 kV Human Body Model
- Replace Multiple Dual NPN & PNP Digital Transistors
- This is a Pb−Free Device

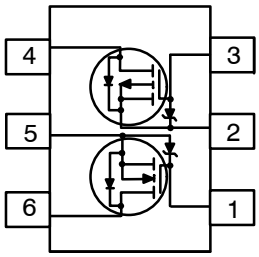
MARKING DIAGRAM



321 = Specific Device Code
M = Assembly Operation Month
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
FDC6321C	TSOT−23−6 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 1999

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		N−Channel	P−Channel	Unit
V_{DSS}, V_{CC}	Drain−Source Voltage, Power Supply Voltage		25	−25	V
V_{GSS}, V_{IN}	Gate−Source Voltage		8	−8	V
I_D, I_O	Drain/Output Current	− Continuous	0.68	−0.46	A
		− Pulsed	2	−1.5	A
P_D	Power Dissipation	(Note 1a)	0.9		W
		(Note 1b)	0.7		W
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150		°C
ESD	Electrostatic Discharge Rating MIL−STD−883D Human Body Model (100 pF / 1500 Ω)		6		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	140	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	60	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

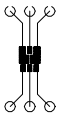
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = −250 μA	N−Ch P−Ch	25 −25	− −	− −	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C I_D = −250 μA,Referenced to 25°C	N−Ch P−Ch	− −	26 −22	− −	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C	N−Ch	− −	− −	1 10	μA
		V_{DS} = −20 V, V_{GS} = 0 V V_{DS} = −20 V, V_{GS} = 0 V, T_J = 55°C	P−Ch	− −	− −	−1 −10	nA
I_{GSS}	Gate−Body Leakage Current	V_{GS} = 8 V, V_{DS} = 0 V V_{GS} = −8 V, V_{DS} = 0 V	N−Ch P−Ch	−	−	100 −100	nA
ON CHARACTERISTICS (Note 2)							
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = −250 μA, Referenced to 25°C	N−Ch P−Ch	− −	−2.6 2.1	− −	mV/°C
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA V_{DS} = V_{GS}, I_D = −250 μA	N−Ch P−Ch	0.65 −0.65	0.8 −0.86	1.5 −1.5	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 4.5 V, I_D = 0.5 A V_{GS} = 4.5 V, I_D = 0.5 A, T_J = 125°C V_{GS} = 2.7 V, I_D = 0.25 A V_{GS} = −4.5 V, I_D = −0.5 A V_{GS} = −4.5 V, I_D = −0.5 A, T_J = 125°C V_{GS} = −2.7 V, I_D = −0.25 A	N−Ch N−Ch N−Ch P−Ch P−Ch P−Ch	− − − − − −	0.33 0.51 0.44 0.87 1.21 1.22	0.45 0.72 0.6 1.1 1.8 1.5	Ω
$I_{D(on)}$	On−State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V V_{GS} = −4.5 V, V_{DS} = −5 V	N−Ch P−Ch	1 −1	− −	− −	A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 0.5 A V_{DS} = −5 V, I_D = −0.5 A	N−Ch P−Ch	− −	1.45 0.8	− −	S

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (continued)

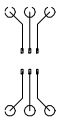
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N−Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz P−Channel V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz	N−Ch P−Ch	− −	50 63	− −	pF
C_{oss}	Output Capacitance		N−Ch P−Ch	− −	28 34	− −	pF
C_{rss}	Reverse Transfer Capacitance		N−Ch P−Ch	− −	9 10	− −	pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{d(on)}$	Turn−On Delay Time	N−Channel V_{DD} = 6 V, I_D = 0.5 A, V_{GS} = 4.5 V, R_{GEN} = 50 Ω P−Channel V_{DD} = −6 V, I_D = −0.5 A, V_{GS} = −4.5 V, R_{GEN} = 50 Ω	N−Ch P−Ch	− −	3 7	6 20	ns
t_r	Turn−On Rise Time		N−Ch P−Ch	− −	8 9	16 18	ns
$t_{d(off)}$	Turn−Off Delay Time		N−Ch P−Ch	− −	17 55	30 110	ns
t_f	Turn−Off Fall Time		N−Ch P−Ch	− −	13 35	25 70	ns
Q_g	Total Gate Charge	N−Channel V_{DS} = 5 V, I_D = 0.5 A, V_{GS} = 4.5 V P−Channel V_{DS} = −5 V, I_D = −0.25 A, V_{GS} = −4.5 V	N−Ch P−Ch	− −	1.64 1.1	2.3 1.5	nC
Q_{gs}	Gate−Source Charge		N−Ch P−Ch	− −	0.38 0.32	− −	nC
Q_{gd}	Gate−Drain Charge		N−Ch P−Ch	− −	0.45 0.25	− −	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain−Source Diode Forward Current		N−Ch P−Ch	− −	− −	0.3 −0.5	A
V_{SD}	Drain−Source Diode Forward Voltage (Note 2)	V_{GS} = 0 V, I_S = 0.5 A V_{GS} = 0 V, I_S = 0.5 A, T_J = 125°C V_{GS} = 0 V, I_S = −0.5 A V_{GS} = 0 V, I_S = −0.5 A, T_J = 125°C	N−Ch N−Ch P−Ch P−Ch	− − − −	0.83 0.69 −0.89 −0.75	1.2 0.85 −1.2 −0.85	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where thecase thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 140°C/W on a 0.125 in^2 pad of 2 oz. copper.



b. 180°C/W on a 0.005 in2 pad of 2 oz. copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS: N−CHANNEL

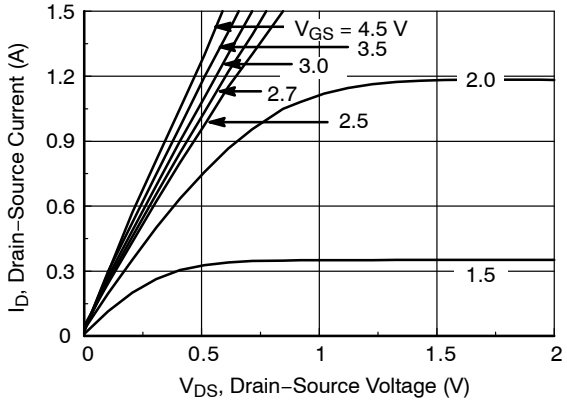


Figure 1. On−Region Characteristics

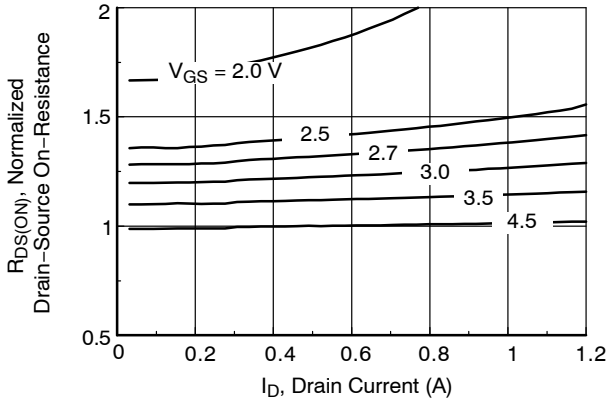


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

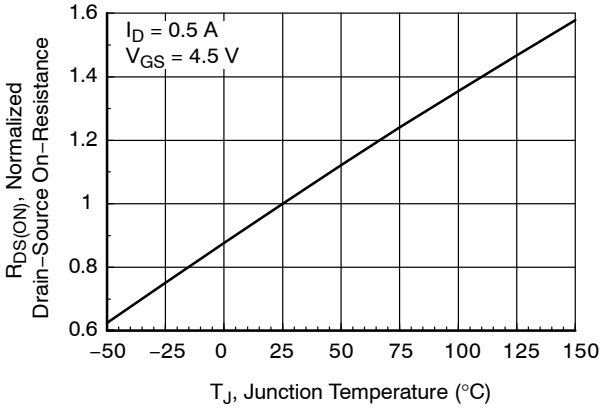


Figure 3. On−Resistance Variation with Temperature

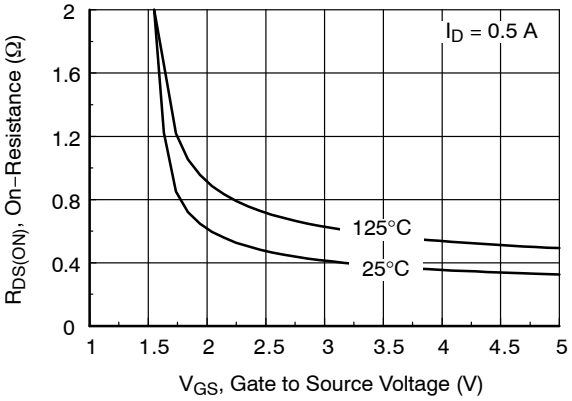


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

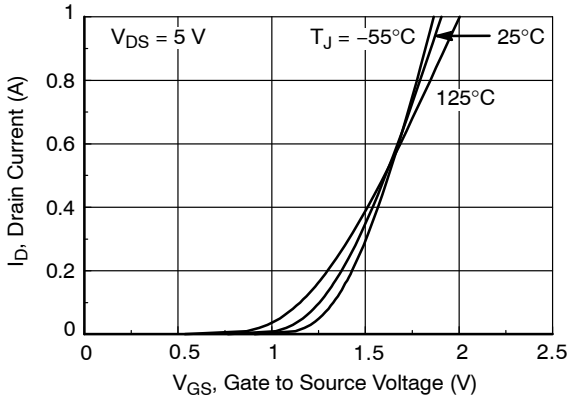


Figure 5. Transfer Characteristics

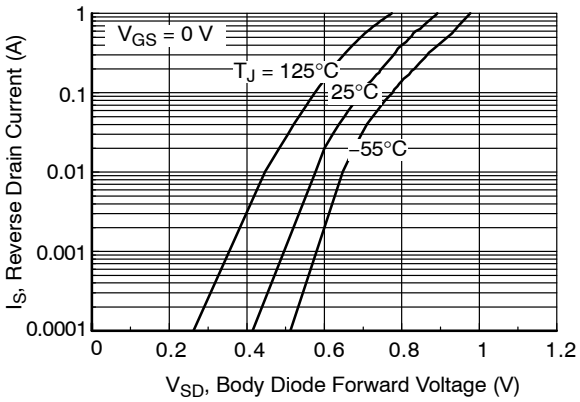


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: N−CHANNEL (continued)

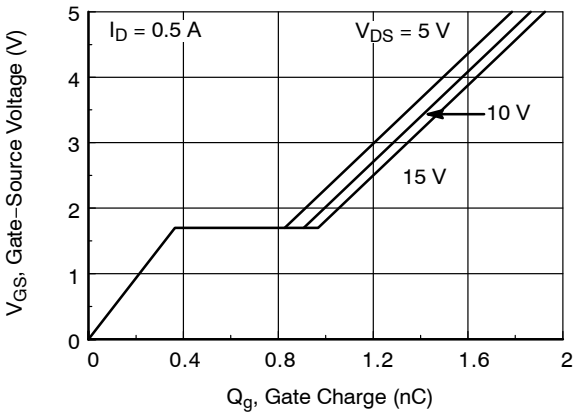


Figure 7. Gate Charge Characteristics

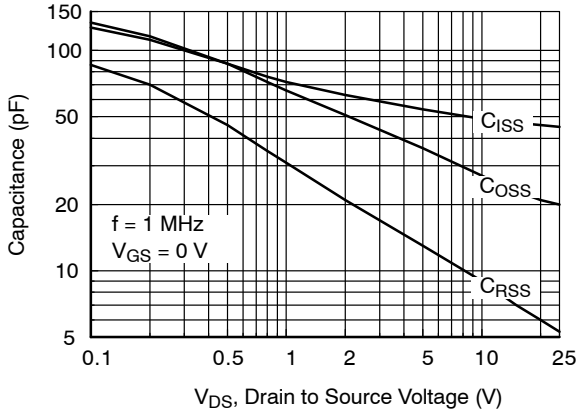


Figure 8. Capacitance Characteristics

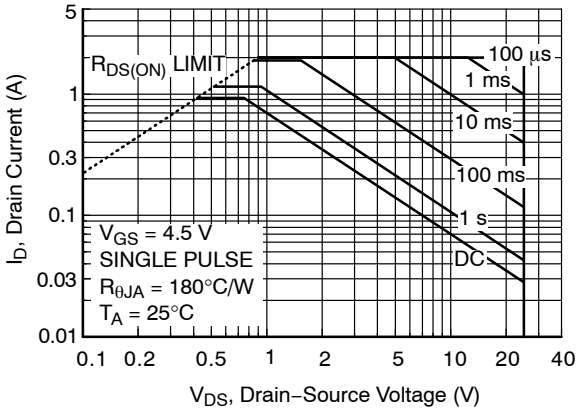


Figure 9. Maximum Safe Operating Area

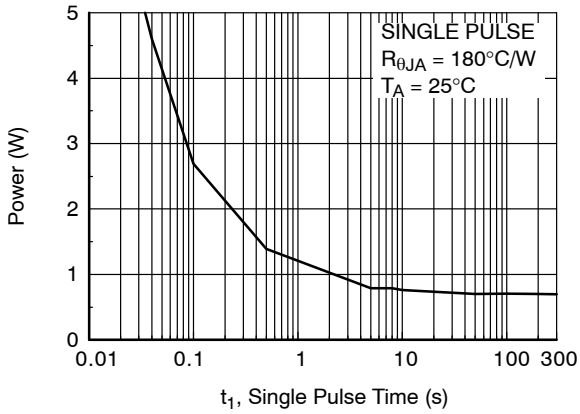


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS: P−CHANNEL

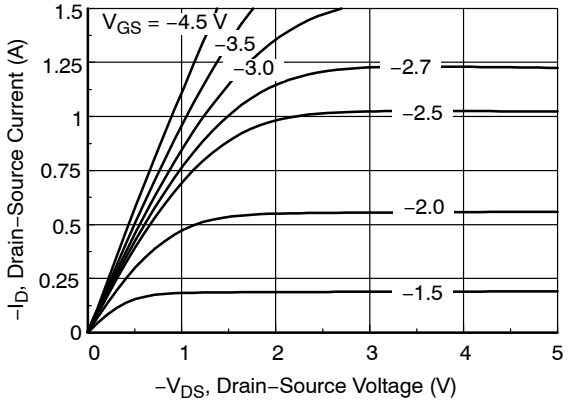


Figure 11. On−Region Characteristics

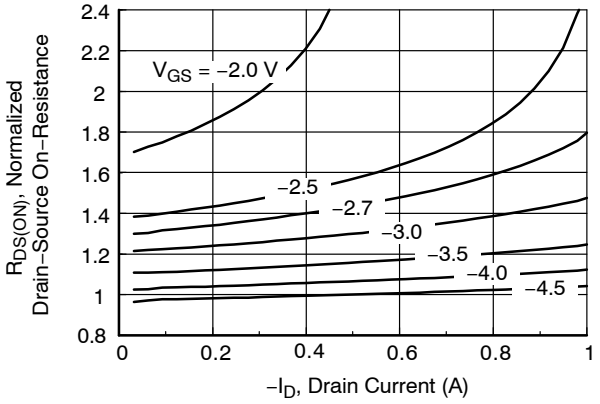


Figure 12. On−Resistance Variation with Drain Current and Gate Voltage

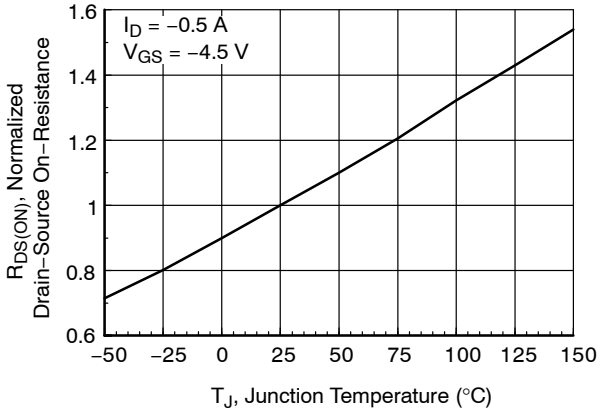


Figure 13. On−Resistance Variation with Temperature

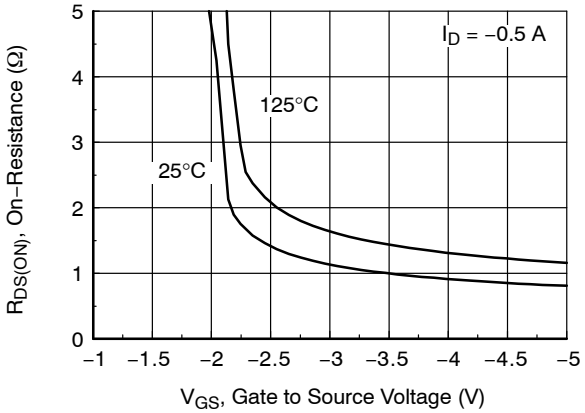


Figure 14. On−Resistance Variation with Gate−to−Source Voltage

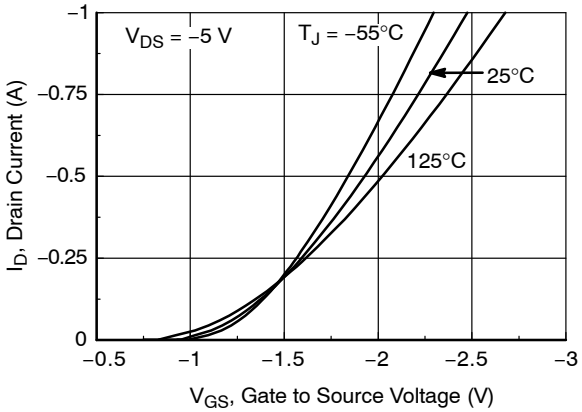


Figure 15. Transfer Characteristics

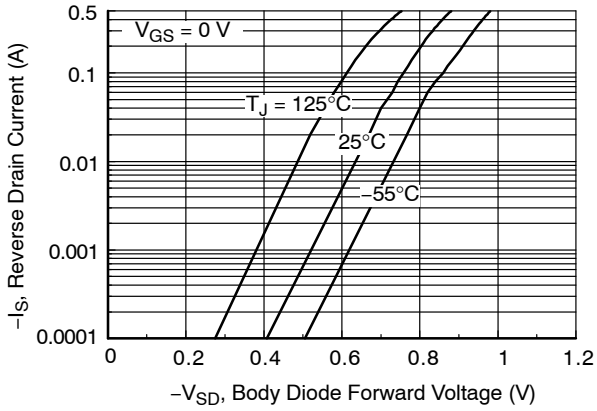


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: P−CHANNEL (continued)

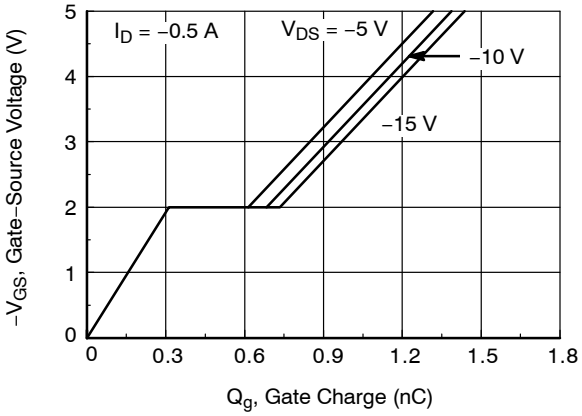


Figure 17. Gate Charge Characteristics

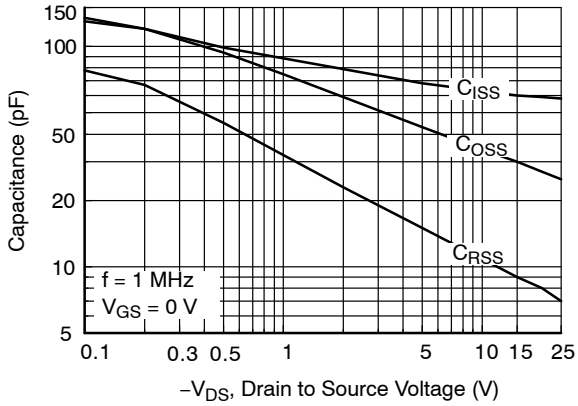


Figure 18. Capacitance Characteristics

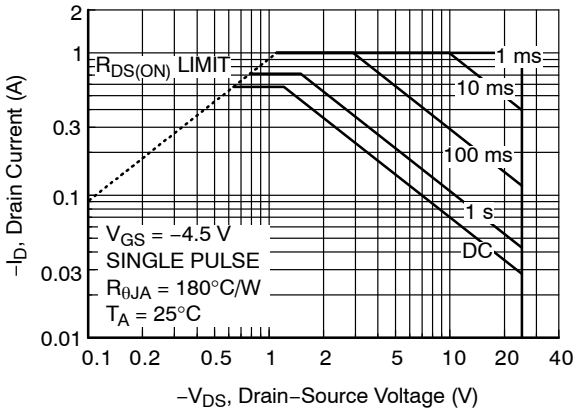


Figure 19. Maximum Safe Operating Area

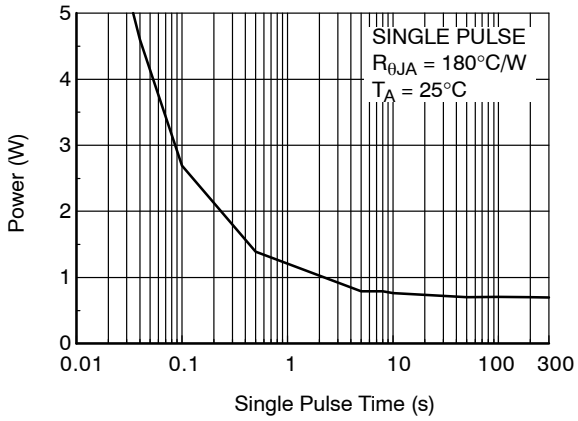


Figure 20. Single Pulse Maximum Power Dissipation

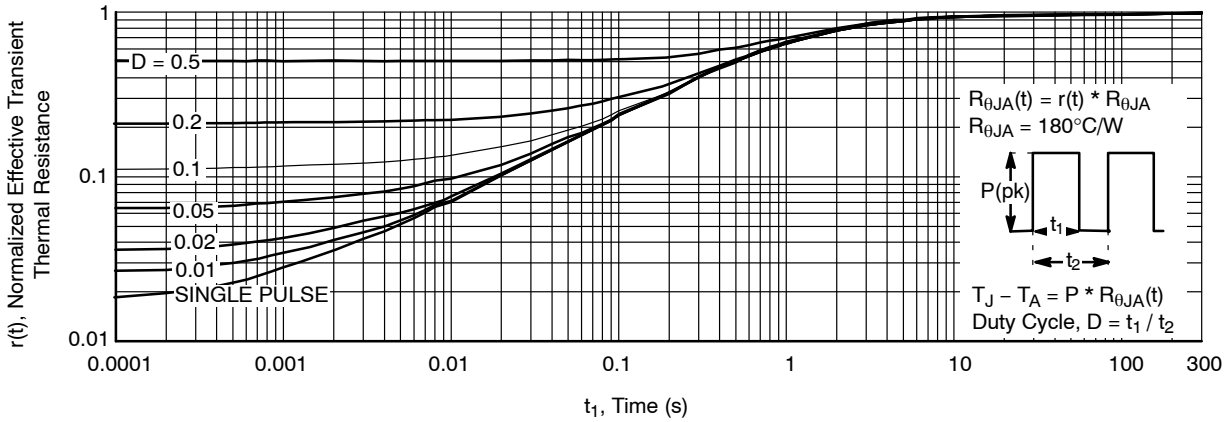


Figure 21. Transient Thermal Response Curve

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

SUPERSOT is a trademark of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries.

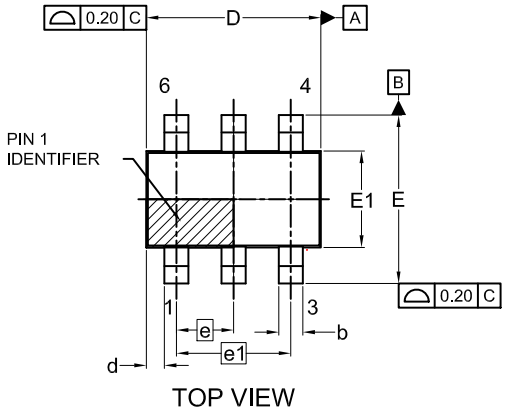
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

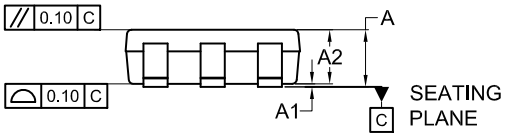
1
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

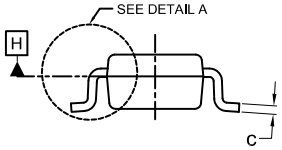


TOP VIEW

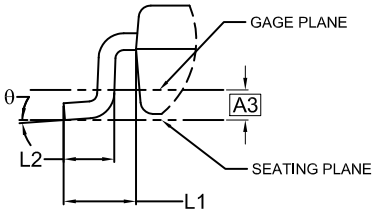


FRONT VIEW

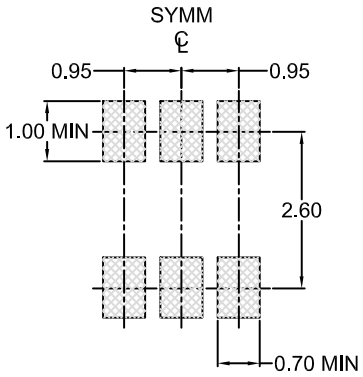
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

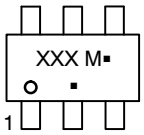
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON83292G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2018

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:
FDC6321C