

256MB – 64Mx32 DDR2 SDRAM UNBUFFERED

FEATURES

- 200-pin, Small-Outline DIMM (SO-DIMM)
- Fast data transfer rates: PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 667*, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, and 5
- Programmable burst: length (4, 8)
- Adjustable data-output drive strength
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Auto & self refresh (64ms: 8,192 cycle refresh)
- Row Addr: A0~A13, Column Addr: A0~A9, Bank Addr: BA0~BA1
- Gold edge contacts
- RoHS Compliant
- JEDEC Package option
 - 200 Pin (SO-DIMM)
 - PCB – 30.00mm (1.181") TYP.

DESCRIPTION

The WV3HG64M32EEU is a 64Mx32 Double Data Rate 2 SDRAM memory module based on 512Mb DDR2 SDRAM components. The module consists of four 64Mx8, in FBGA package mounted on a 200 pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

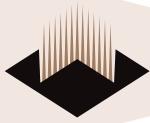
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	333MHz	266MHz	200MHz
CL-tRCD-tRP	5-5-5	4-4-4	3-3-3

Note:
• Consult factory for availability



PIN CONFIGURATION

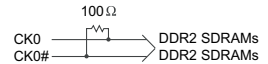
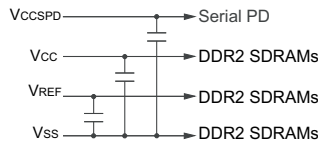
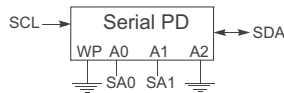
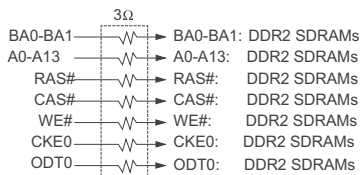
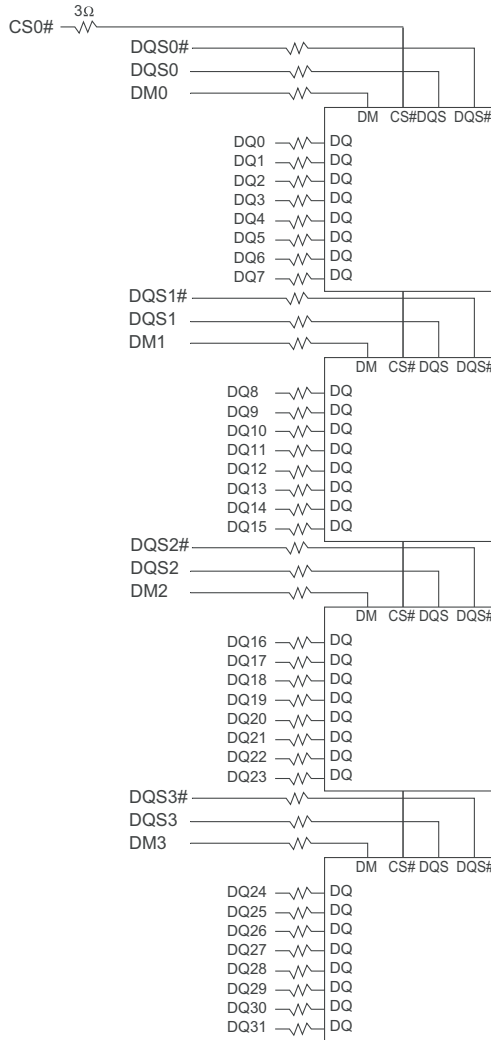
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	DQS2	101	A1	151	NC
2	Vss	52	DM2	102	A0	152	NC
3	Vss	53	Vss	103	vcc	153	NC
4	DQ4	54	Vss	104	vcc	154	NC
5	DQ0	55	DQ18	105	A10/AP	155	Vss
6	DQ5	56	DQ22	106	BA1	156	Vss
7	DQ1	57	DQ19	107	BA0	157	NC
8	Vss	58	DQ23	108	RAS#	158	NC
9	Vss	59	Vss	109	WE#	159	NC
10	DM0	60	Vss	110	CS0#	160	NC
11	DQS0#	61	DQ24	111	vcc	161	Vss
12	Vss	62	DQ28	112	vcc	162	Vss
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	NC
15	Vss	65	Vss	115	NC	165	Vss
16	DQ7	66	Vss	116	A13	166	NC
17	DQ2	67	DM3	117	vcc	167	NC
18	Vss	68	DQS3#	118	vcc	168	Vss
19	DQ3	69	NC	119	NC	169	NC
20	DQ12	70	DQS3	120	NC	170	NC
21	Vss	71	Vss	121	Vss	171	Vss
22	DQ13	72	Vss	122	Vss	172	Vss
23	DQ8	73	DQ26	123	NC	173	NC
24	Vss	74	DQ30	124	NC	174	NC
25	DQ9	75	DQ27	125	NC	175	NC
26	DM1	76	DQ31	126	NC	176	NC
27	Vss	77	Vss	127	Vss	177	Vss
28	Vss	78	Vss	128	Vss	178	Vss
29	DQS1#	79	CKE0	129	NC	179	NC
30	CK0	80	NC	130	NC	180	NC
31	DQS1	81	vcc	131	NC	181	NC
32	CK0#	82	vcc	132	Vss	182	NC
33	Vss	83	NC	133	Vss	183	Vss
34	Vss	84	NC	134	NC	184	Vss
35	DQ10	85	NC	135	NC	185	NC
36	DQ14	86	NC	136	NC	186	NC
37	DQ11	87	vcc	137	NC	187	Vss
38	DQ15	88	vcc	138	Vss	188	NC
39	Vss	89	A12	139	Vss	189	NC
40	Vss	90	A11	140	NC	190	Vss
41	Vss	91	A9	141	NC	191	NC
42	Vss	92	A7	142	NC	192	NC
43	DQ16	93	A8	143	NC	193	Vss
44	DQ20	94	A6	144	Vss	194	NC
45	DQ17	95	vcc	145	Vss	195	SDA
46	DQ21	96	vcc	146	NC	196	Vss
47	Vss	97	A5	147	NC	197	SCL
48	Vss	98	A4	148	NC	198	SA0
49	DQS2#	99	A3	149	Vss	199	VCCSPD
50	NC	100	A2	150	Vss	200	SA1

PIN NAMES

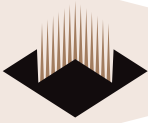
SYMBOL	DESCRIPTION
A0-A13	Address input
ODT0	On-Die Termination
CK0, CK0#	Differential Clock Inputs
CKE0	Clock Enable input
CS0#	Chip select
RAS#, CAS#, WE#	Command Inputs
BA0, BA1	Bank Address Inputs
DM0-DM3	Input Data Mask
A10/AP	Address input/Auto precharge
DQ0-DQ31	Data Input/Output
DQS0-DQS3 DQS0#-DQS3#	Data Strobe
SCL	Serial Clock for Presence Detect
SA0-SA1	Presence Detect Address Inputs
SDA	Serial Presence Detect Data
Vcc	Power Supply: +1.8V ±0.1V
VREF	SSTL_18 reference voltage
Vss	Ground
VCCSPD	Serial EEPROM Positive Power Supply
NC	No Connect



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor value, are 22 ohms ± 5% unless otherwise specified.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-0.5	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
I _L	Input leakage current; Any input 0V < V _{IN} < V _{CC} ; V _{REF} input 0V < V _{IN} < 0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-20	20	μA
		CS#, CKE	-20	20	μA
		CK, CK#	-20	20	μA
		DM	-5	5	μA
I _{oz}	Output leakage current; 0V < V _{IN} < V _{CC} ; DQs and ODT are disable	-5	5	μA	
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-8	8	μA	

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	3
I/O Reference Voltage	V _{REF}	0.49 x V _{CC}	0.50 x V _{CC}	0.51 x V _{CC}	V	1
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	2

Notes:

- V_{REF} is expected to equal V_{CC}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCQ} of all IC's are tied to V_{CC}.



INPUT/OUTPUT CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 100\text{MHz}$

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}	8	12	pF
Input Capacitance CKE0, ODT	C_{IN2}	8	12	pF
Input Capacitance CS0#	C_{IN3}	8	12	pF
Input Capacitance (CK0, CK0#)	C_{IN4}	8	12	pF
Input Capacitance (DM0 ~ DM3), (DQS0 ~ DQS3)	C_{IN5} (665)	6.5	7.5	pF
	C_{IN5} (534)	6.5	8	pF
Input Capacitance (DQ0 ~ DQ31)	C_{OUT1} (665)	6.5	7.5	pF
	C_{OUT1} (534)	6.5	8	pF

Notes:

- AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature (Commercial)	TOPER	0° to 85°	°C	1, 2

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	$V_{IH}(DC)$	$V_{REF} + 0.125$	$V_{CC} + 0.300$	V
Input Low (Logic 0) Voltage	$V_{IL}(DC)$	-0.300	$V_{REF} - 0.125$	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	$V_{IH}(AC)$	$V_{REF} + 0.250$	-	V
Input Low (Logic 1) Voltage DDR2-667	$V_{IH}(AC)$	$V_{REF} + 0.200$	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	$V_{IL}(AC)$	-	$V_{REF} - 0.250$	V
Input Low (Logic 0) Voltage DDR2-667	$V_{IL}(AC)$	-	$V_{REF} - 0.200$	V



Icc SPECIFICATION

V_{CC} = +1.8V ± 0.1V

Symbol	Proposed Conditions	665	534	403	Units	
I _{CC0} *	Operating one bank active-precharge; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	340	320	320	mA	
I _{CC1} *	Operating one bank active-read-precharge; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}	400	380	380	mA	
I _{CC2P} **	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	32	32	32	mA	
I _{CC2Q} **	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	140	120	120	mA	
I _{CC2N} **	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	160	140	140	mA	
I _{CC3P} **	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	120	120	120	mA
		Slow PDN Exit MRS(12) = 1	48	48	48	mA
I _{CC3N} **	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	220	200	200	mA	
I _{CC4W} *	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RAS} max(I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	560	480	440	mA	
I _{CC4R} *	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RAS} max(I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}	580	500	440	mA	
I _{CC5} **	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{REFC} (I _{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	600	560	560	mA	
I _{CC6} **	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	32	32	32	mA	
I _{CC7} *	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RC} D(I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	880	880	880	mA	

I_{CC} specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

Note:

*: Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** : Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS			665		534		403			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
	CL = 5	t _{CK (5)}	3,000	8,000					ps	
	CL = 4	t _{CK (4)}	3,750	8,000	3,750	8,000	5,000	8,000	ps	
	CL = 3	t _{CK (3)}	5,000	8,000	5,000	8,000	5,000	8,000	ps	
	CK high-level width		t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}
	CK low-level width		t _{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}
	Half clock period		t _{HP}	MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		ps
	Clock jitter		t _{JIT}	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t _{AC}	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t _{HZ}		t _{AC} MAX		t _{AC} MAX		t _{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t _{LZ}	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t _{DS}	100		100		150		ps
	DQ and DM input hold time relative to DQS		t _{DH}	225		225		275		ps
	DQ and DM input pulse width (for each input)		t _{DLPW}	0.35		0.35		0.35		t _{CK}
	Data hold skew factor		t _{QHS}		340		400		450	ps
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access		t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps
	Data valid output window (DVW)		t _{DVW}	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns
Data Strobe	DQS input high pulse width		t _{DQSH}	0.35		0.35		0.35		t _{CK}
	DQS input low pulse width		t _{DQSL}	0.35		0.35		0.35		t _{CK}
	DQS output access time from CK/CK#		t _{DQSCK}	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising ... setup time		t _{DSS}	0.2		0.2		0.2		t _{CK}
	DQS falling edge from CK rising ... hold time		t _{DSH}	0.2		0.2		0.2		t _{CK}
	DQS...DQ skew, DQS to last DQ valid, per group, per access		t _{DQSQ}		240		300		350	ps
	DQS read preamble		t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}
	DQS read postamble		t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}
	DQS write preamble setup time		t _{WPRES}	0		0		0		ps
	DQS write preamble		t _{WPRE}	0.35		0.35		0.35		t _{CK}
	DQS write postamble		t _{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}
	Write command to first DQS latching transition		t _{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t _{CK}
	Address and control input pulse width for each input		t _{IPW}	0.6		0.6		0.6		t _{CK}
	Address and control input setup time		t _{IS}	200		250		350		ps
	Address and control input hold time		t _{IH}	275		375		475		ps
	Address and control input hold time		t _{CCD}	2		2		2		t _{CK}

Note:
 AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.
 Continued on next page



AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t _{RC}	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCO}	15		15		15		ns
	Four Bank Activate period	t _{FAW}	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	45	70,000	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	7.5		7.5		7.5		ns
	Write recovery time	t _{WR}	15		15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	t _{WR} + t _{RP}		t _{WR} + t _{RP}		t _{WR} + t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	7.5		7.5		10		ns
	PRECHARGE command period	t _{RP}	15		15		15		ns
	PRECHARGE ALL command period	t _{RPA}	t _{RP} + t _{CK}		t _{RP} + t _{CK}		t _{RP} + t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	2		2		2		t _{CK}
	CKE low to CK,CK# uncertainty	t _{DELAY}	t _{IS} + t _{CK} + t _{IH}		t _{IS} + t _{CK} + t _{IH}		t _{IS} + t _{CK} + t _{IH}		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interval	t _{RFC}	105	70,000	105	70,000	105	70,000	ns
	Average periodic refresh interval	t _{REFI}		7.8		7.8		7.8	μs
	Exit self refresh to non-READ command	t _{XSNR}	t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t _{XSRD}	200		200		200		t _{CK}
	Exit self refresh timing reference	t _{ISXR}	t _{IS}		t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AO_{ND}}	2	2	2	2	2	2	t _{CK}
	ODT turn-on	t _{AO_N}	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	ps
	ODT turn-off delay	t _{AO_{FD}}	2.5	2.5	2.5	2.5	2.5	2.5	t _{CK}
	ODT turn-off	t _{AO_F}	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t _{AO_{NP_D}}	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t _{AO_{FP_D}}	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t _{AN_{PD}}	3		3		3		t _{CK}
	ODT power-down exit latency	t _{AX_{PD}}	8		8		8		t _{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	2		2		2		t _{CK}
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	7 - AL		6 - AL		6 - AL		t _{CK}
	A Exit precharge power-down to any non-READ command.	t _{XP}	2		2		2		t _{CK}
	CKE minimum high/low time	t _{CKE}	3		3		3		t _{CK}

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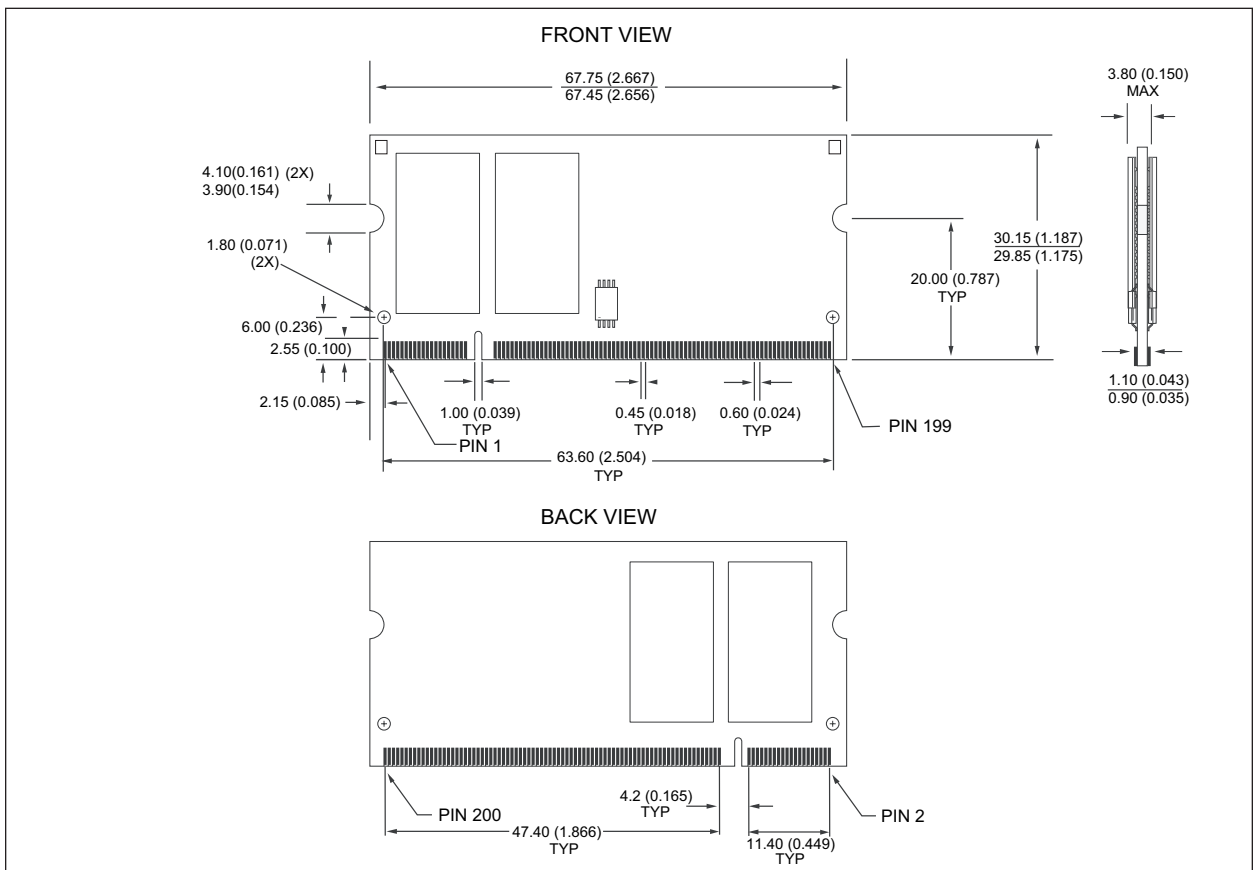
ORDERING INFORMATION FOR D4

Part Number	Clock/Data Rate Frequency	CAS Latency	t _{RCD}	t _{RP}	Height**
WV3HG64M32EEU665D4xxG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M32EEU534D4xxG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M32EEU403D4xxG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

* Consult Factory for availability

- NOTES:
- RoHS product. ("G" = RoHS Compliant)
 - Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
 - Consult factory for availability of industrial temperature (-40°C to 85°C) option

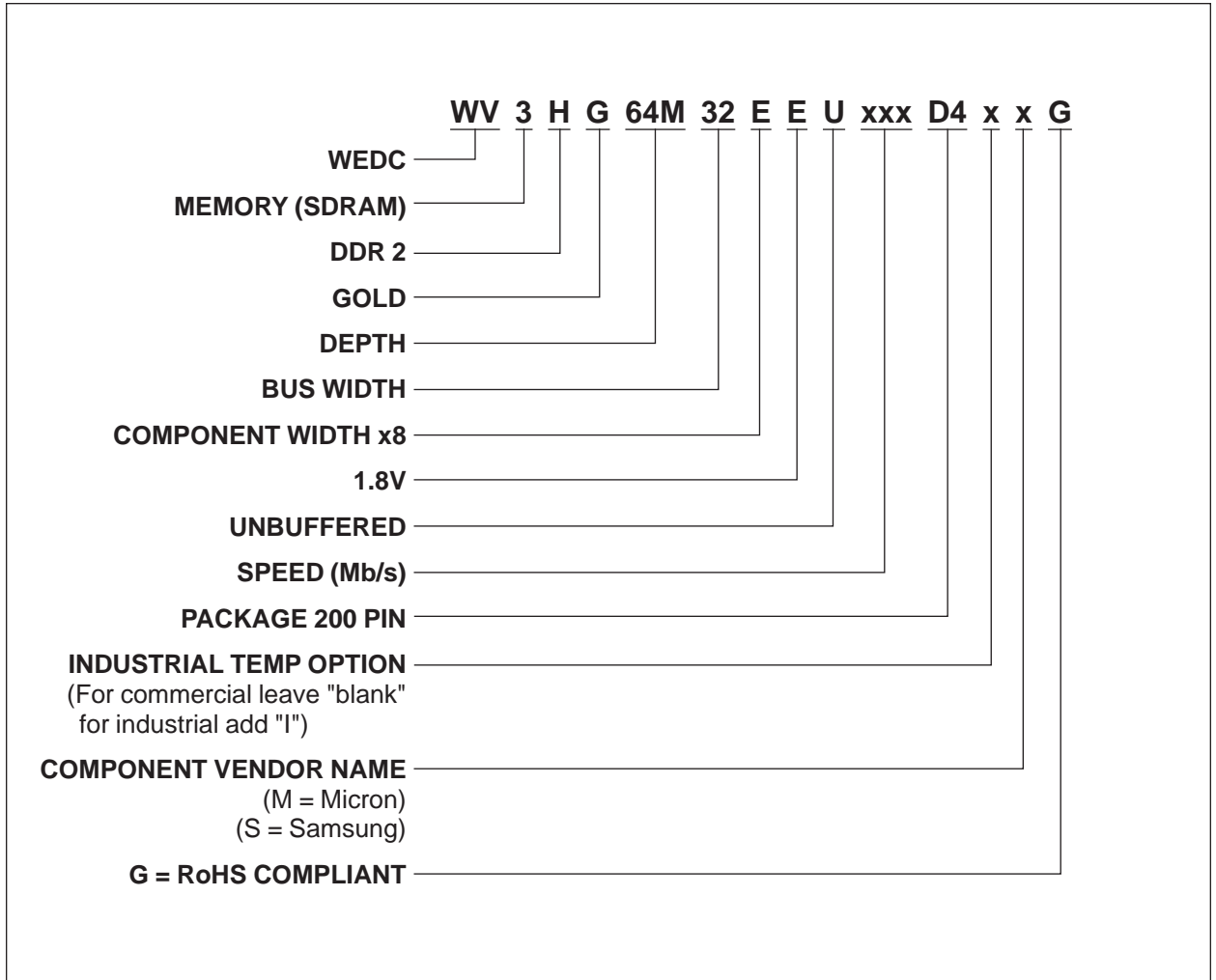
PACKAGE DIMENSIONS FOR D4

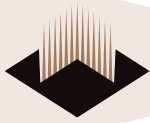


** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

256MB – 64Mx32 DDR2 SDRAM UNBUFFERED

DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q2'06
- MICRON: U37Y: B-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	3-06	Advanced
Rev 1	1.1 Added row, column, and bank address	3-23-06	Advanced
Rev 2	2.1 Correction on component used, (512Mb) 2.2 Added V _{CCQ} update 2.3 Added "x" to part number to indicate industrial temp option 2.4 Added "x" to part numbering guide to indicate industrial temp option 2.5 Added die rev info	5-06	Advanced