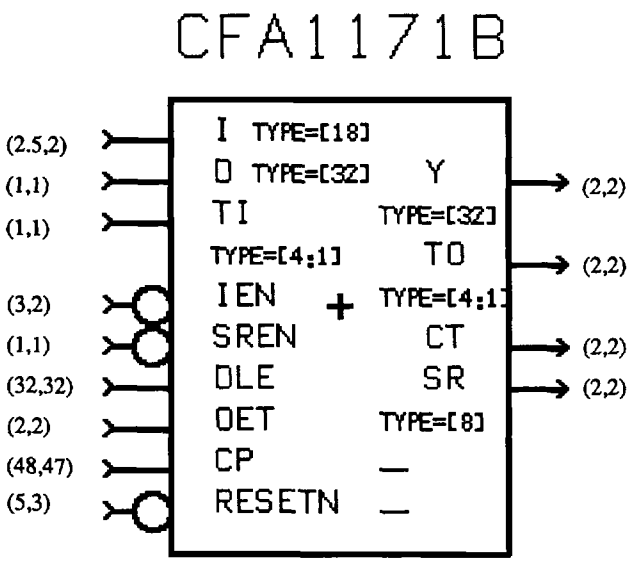
GENERAL DESCRIPTION: AM29117 - 32-BIT VERSION

The megafunction is designed to be functionally a 32-bit AM29117. Two instruction lines are added and data paths are expanded to 32-bit wide. The most significant instruction line, I17, is added to be an additional bit in the 'N' field as required for 32-bit rotate and bit instructions. The next most significant bit, I16, is added to indicate Long Word mode. OET and OEYN work the same as in the CFA1170C to control the three-state or bidirectional signals.

User can use RESETN input to reset the internal flips or tie this signal to High and enter two NO-OP instructions for initialization. User should refer to 29117 data sheet for detail instruction operations.

PIN CONNECTION DIAGRAM:



FEATURES:

- 32-bit Arithmetic, Logic, CRC, Rotate, Rotate-and-Merge, Rotate-and-Compare, Prioritize, and other functions
- In LongWord mode: 32-bit data is written to destination
- In Word mode: lower word of 16-bit data is written and the upper 16 bits of destination is not modified
- In Byte mode: only the lowest byte is changed

EQUIVALENT USED GATES: 7381 GATES
(for rough area estimates)

THIS MEGAFUNCTION CONSISTS OF :
Two 22 cols x 108 rows metal megacells;
5242 soft-coded gates.

POWER: NOT AVAILABLE.

FAULT COVERAGE(%): 95%

PIN DESCRIPTION:

Inputs:

D31:0 Data input lines.
D15:0 are used as external data inputs which allow data to be directly loaded into the 16-bit Data Latch.

DLE Data Latch Enable
When DLE is HIGH, the 16-bit Data Latch is transparent and is latched when DLE is LOW.

I17:0 Instruction Inputs
Sixteen Instruction Inputs, used to select the operation to be performed in the CFA1171B. Also used as data inputs while performing immediate instructions.

$\overline{\text{IEN}}$ Instruction Enable (low)
When IEN is LOW, data can be written into RAM when the clock is LOW. The Accumulator can accept data during the LOW-to-HIGH transition of the clock. Having IEN LOW, the Status Register can be updated when SRE is LOW. With IEN HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs.

SREN Status Register Enable (low)
When SRE and IEN are both LOW, the Status Register is updated at the end of all instruction with the exception of NO-OP, Save Status, and Test Status. Having either SRE or IEN HIGH will inhibit the Status Register from changing.

CP Clock Pulse
The clock input to the CFA1171B. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the LOW period of the clock, provided IEN is LOW, and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-to-HIGH transition of the clock if IEN is also LOW. The Instruction Latch becomes transparent when it exits an immediate instruction mode during a LOW-to-HIGH transition of the clock.

OET Output Enable
When OET is LOW, 4-bit T outputs are disabled; when OET is HIGH, the 4-bit T outputs are enabled.

RESETN Reset Pin
This Reset Signal is used to reset the internal Flip-Flop.

Outputs:

Y31:0 Data Output Lines
The sixteen data output lines are always enable in CFA1171B.

CT Conditional Test
The condition code multiplexer selects one of the twelve condition code signals and places it on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

Bidirections:

T4:1 Test I/O Pins (input/output)
Under the control of OET, the four lower status bits (Z,C,N, and OVR) become outputs on T4:1, respectively, when OET goes HIGH. When OET is HIGH, the OET is LOW, T4:1 are used as inputs to generate the CT output.

Characteristics

A. Combinational Delays

Inputs	Y31:0	TO4:1	CT
I4:0 (Addr)	34.4	38.5	-
I17:0(Data)	24.1	29.5	-
I17:0(Instr)	32.1	36.2	23.3
DLE	24.7	28.5	-
TI4:1	-	-	9.1
CP	27.5	32.0	10.7
D31:0	24.3	28.1	-
IEN	-	-	11.2

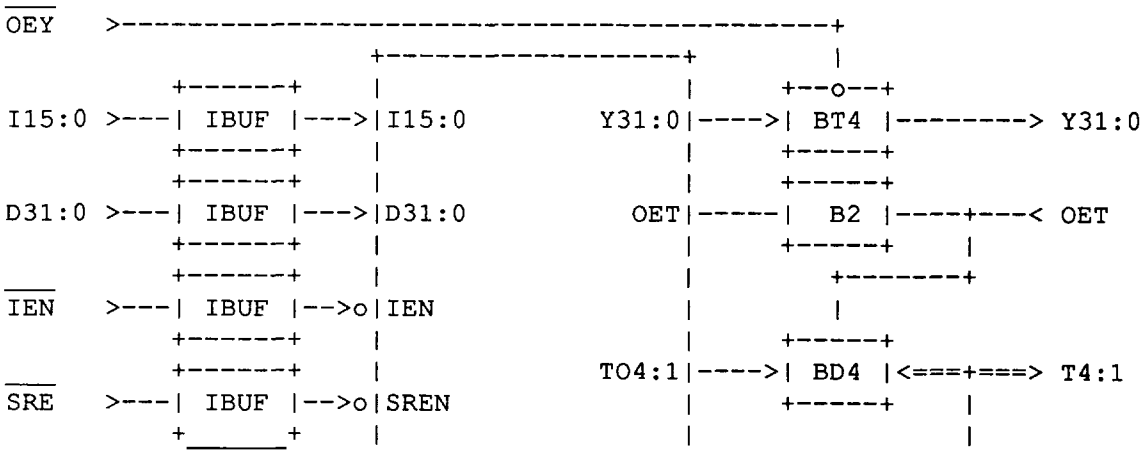
All delays are nominal case with fanout=2

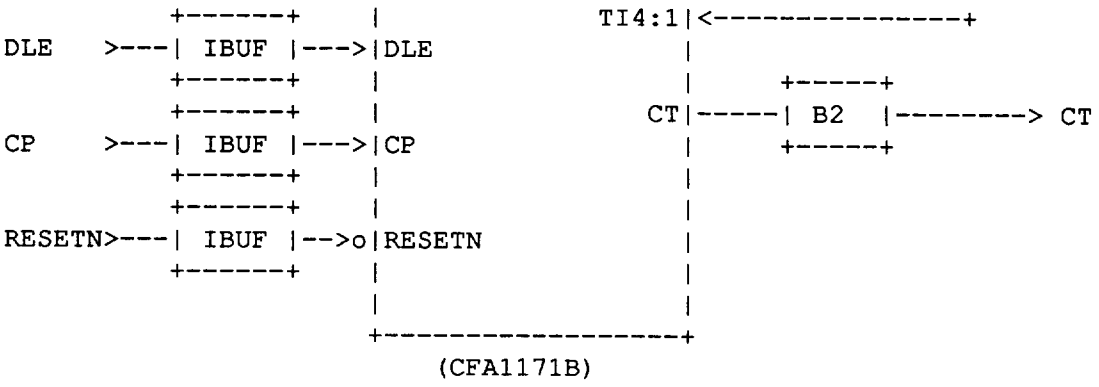
B. Set-up and Hold Times

Inputs	With Respect To	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold
I4:0(Addr)	CP	ts1 13.5	th1 0	-	-
I4:0(Addr)	CP IEN low	ts2 6.8	-	-	th7 0
I17:0(Data)	CP	-	-	ts8 30	th8 0
I17:0(Instr)	CP	ts3 11.4	th3 0	ts9 36	th9 0
I17:0(Instr)	IEN	ts16 8.7	th16 0	-	-
IEN high	CP	ts4 5.5	-	-	th10 0
IEN low	CP	ts5 3.0	th5 0	ts11 7.6	th11 0
SREN	CP	-	-	ts12 7.6	th12 0
D31:0	CP	-	-	ts13 26	th13 0
D31:0	DLE	ts6 2	th6 2	-	-
DLE	CP	-	-	-	th14 27

All delays are nominal case with fanout=2

MACRO TO STANDARD PART I/O CONVERSION




DLE
CP
RESETN
IBUF
IBUF
IBUF
DLE
CP
RESETN
TI4:1
CT
B2
CT
(CFA1171B)