

Philips Components-Signetics

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Application Specific Product	

80C32/80C52/87C52

CMOS single-chip

8-bit microcontroller

DESCRIPTION

The Philips 80C32/80C52/87C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC52 is functionally compatible with the NMOS SCN-8032/8052 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

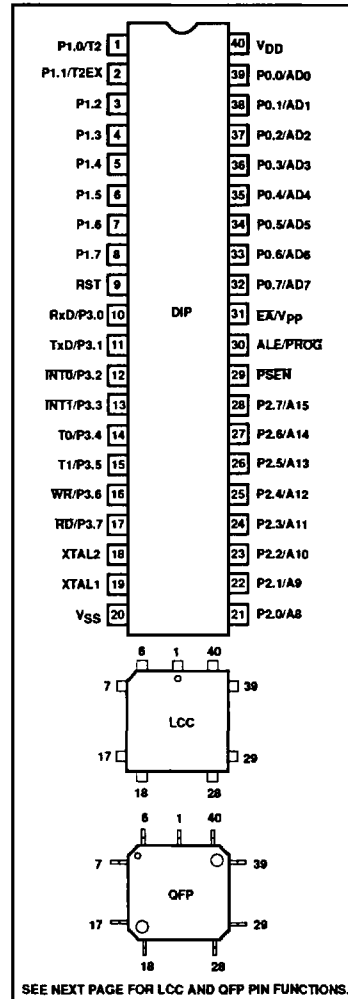
The 8XC52 contains an 8K x 8 ROM (80C52) EPROM (87C52), a 256 x 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 8XC52 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
- 8032/8052 compatible
 - 8k x 8 ROM (80C52)
 - 8k x 8 EPROM (87C52)
 - ROMless (80C32)
 - 256 x 8 RAM
 - Three 16-bit counter/timers
 - Full duplex serial channel
 - Boolean processor
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- Two speed ranges:
 - 3.5 to 16MHz
 - 3.5 to 20MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



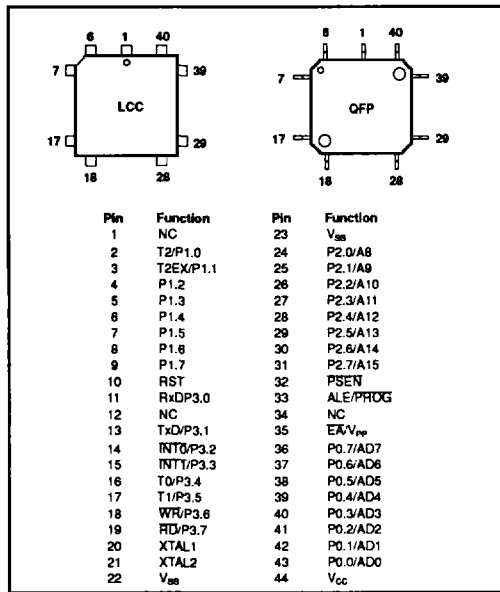
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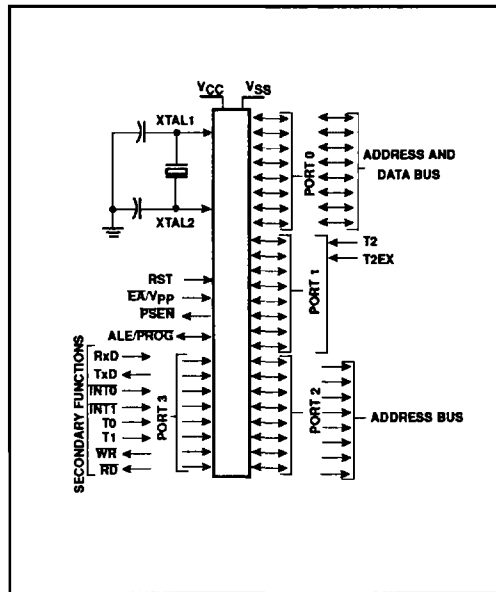
PART NUMBER SELECTION

ROMless	ROM	EPROM	TEMPERATURE °C AND PACKAGE	FREQUENCY (MHz)
P80C32EBP	P83C52EBP	P87C52EBP	0 to +70, plastic DIP	16
P80C32EBA	P83C52EBA	P87C52EBA	0 to +70, plastic LCC	16
		P87C52GFF	-40 to +85, ceramic DIP	20
P80C32GFP	P83C52GFP	P87C52GFP	-40 to +85, plastic DIP	20
		P87C52GFL	-40 to +85, ceramic LCC	20
P80C32GFA	P83C52GFA	P87C52GFA	-40 to +85, plastic LCC	20
P80C32GGB	P83C52GGB	P87C52GGB	0 to +70, plastic QFP	20

LCC AND QFP PIN FUNCTIONS



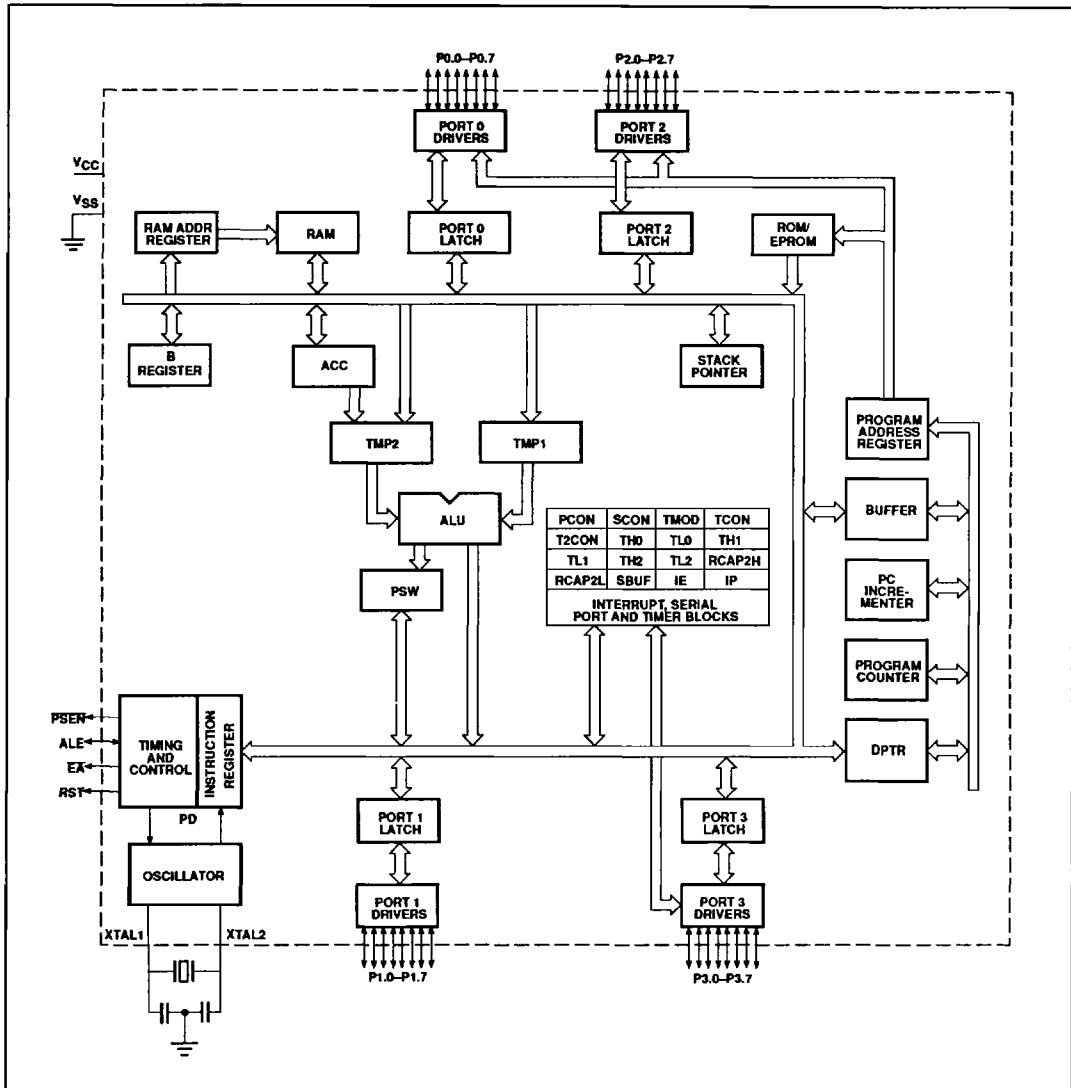
LOGIC SYMBOL



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BLOCK DIAGRAM



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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LCC/ QFP		
V _{SS}	20	22	I	Ground: 0V reference.
V _{CC}	40	44	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–46	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C52. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2: T2 (P1.0): Timer/counter 2 external count input. T2EX (P1.1): Timer/counter 2 trigger input.
P2.0–P2.7	21–28	24–31	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below: RxD (P3.0): Serial input port TxD (P3.1): Serial output port INT0 (P3.2): External interrupt INT1 (P3.3): External interrupt T0 (P3.4): Timer 0 external input T1 (P3.5): Timer 1 external input WR (P3.6): External data memory write strobe RD (P3.7): External data memory read strobe
RST	9	10	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
E _A /V _{PP}	31	35	I	External Access Enable/Programming Supply Voltage: E _A must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If E _A is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming.
XTAL1	19	21	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	O	Crystal 2: Output from the inverting oscillator amplifier.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 1.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At

power-up, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are pre-

served. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory.

Table 1 shows the state of I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Electrical Deviations from Commercial Specifications for Extended Temperature Range (87C52)

DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage, except EA		-0.5	$0.2V_{CC}-0.15$	V
V_{IL1}	Input low voltage to EA		0	$0.2V_{CC}-0.35$	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}+1$	$V_{CC}+0.5$	V
V_{IH1}	Input high voltage to XTAL1, RST		$0.7V_{CC}+0.1$	$V_{CC}+0.5$	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.45\text{V}$		-75	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	$V_{IN} = 2.0\text{V}$		-750	μA
I_{CC}	Power supply current: Active mode Idle mode Power-down mode	$V_{CC} = 4.5-5.5\text{V}$, Frequency range = 3.5 to 12MHz		35 6 50	mA mA μA

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ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on EA/V _{PP} pin to V _{SS}	0 to +13.0	V
Voltage on any other pin to V _{SS}	-0.5 to +6.5	V
Input, output current on any two pins	±10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C52)T_A = 0°C to +70°C or -40°C to +85°C, V_{CC} = 5V ±20%, V_{SS} = 0V (80C32/80C52)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYPICAL ¹	MAX	
V _{IL}	Input low voltage, except EA ⁷		-0.5		0.2V _{CC} -0.1	V
V _{IL1}	Input low voltage to EA ⁷		0		0.2V _{CC} -0.3	V
V _{IH}	Input high voltage, except XTAL1, RST ⁷		0.2V _{CC} +0.9		V _{CC} +0.5	V
V _{IH1}	Input high voltage, XTAL1, RST ⁷		0.7V _{CC}		V _{CC} +0.5	V
V _{OL}	Output low voltage, ports 1, 2, 3	I _{OL} = 1.6mA ²			0.45	V
V _{OL1}	Output low voltage, port 0, ALE, PSEN	I _{OL} = 3.2mA ²			0.45	V
V _{OH}	Output high voltage, ports 1, 2, 3, ALE, PSEN ³	I _{OH} = -60µA	2.4			V
		I _{OH} = -25µA	0.75V _{CC}			V
		I _{OH} = -10µA	0.9V _{CC}			V
V _{OH1}	Output high voltage (port 0 in external bus mode)	I _{OH} = -800µA	2.4			V
		I _{OH} = -300µA	0.75V _{CC}			V
		I _{OH} = -80µA	0.9V _{CC}			V
I _{IL}	Logical 0 input current, ports 1, 2, 3 ⁷	V _{IN} = 0.45V			-50	µA
I _{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁷	See note 4			-650	µA
I _{LI}	Input leakage current, port 0	V _{IN} = V _{IL} or V _{IH}			±10	µA
I _{CC}	Power supply current: ⁷ Active mode @ 12MHz ⁵ Idle mode @ 12MHz Power-down mode	See note 6		11.5	25	mA
				1.3	4	mA
				3	50	µA
R _{RST}	Internal reset pull-down resistor		50		300	kohm
C _{ID}	Pin capacitance				10	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9V_{CC} specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- I_{CC}MAX at other frequencies is given by: Active mode: I_{CC}MAX = 0.94 X FREQ + 13.71; Idle mode: I_{CC}MAX = 0.14 X FREQ + 2.31, where FREQ is the external oscillator frequency in MHz. I_{CC}MAX is given in mA. See Figure 8.
- See Figures 9 through 12 for I_{CC} test conditions.
- These values apply only to T_A = 0°C to +70°C. For T_A = -40°C to +85°C, see table on previous page.

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AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (87C52)^{1,2}

SYMBOL	FIGURE	PARAMETER	20MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency: <i>Speed Versions</i> 8XC52 E 8XC52 G			3.5 3.5	16 20	MHz MHz
t_{HLL}	1	ALE pulse width	60		$2t_{CLCL}-40$		ns
t_{AVLL}	1	Address valid to ALE low	18		$t_{CLCL}-32$		ns
t_{LLAX}	1	Address hold after ALE low	30		$t_{CLCL}-20$		ns
t_{LLIV}	1	ALE low to valid instruction in		100		$4t_{CLCL}-100$	ns
t_{LLPL}	1	ALE low to PSEN low	33		$t_{CLCL}-17$		ns
t_{PLPH}	1	PSEN pulse width	115		$3t_{CLCL}-35$		ns
t_{PLIV}	1	PSEN low to valid instruction in		45		$3t_{CLCL}-105$	ns
t_{PXIX}	1	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	1	Input instruction float after PSEN		25		$t_{CLCL}-25$	ns
t_{AVIV}	1	Address to valid instruction in		175		$5t_{CLCL}-75$	ns
t_{PLAZ}	1	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	2, 3	RD pulse width	200		$6t_{CLCL}-100$		ns
t_{WLWH}	2, 3	WR pulse width	200		$6t_{CLCL}-100$		ns
t_{RLDV}	2, 3	RD low to valid data in		85		$5t_{CLCL}-165$	ns
t_{RHDX}	2, 3	Data hold after RD	0		0		ns
t_{RHDX}	2, 3	Data float after RD		72		$2t_{CLCL}-28$	ns
t_{LLDV}	2, 3	ALE low to valid data in		250		$8t_{CLCL}-150$	ns
t_{AVDV}	2, 3	Address to valid data in		285		$9t_{CLCL}-165$	ns
t_{LLWL}	2, 3	ALE low to RD or WR low	100	200	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to WR low or RD low	70		$4t_{CLCL}-130$		ns
t_{QVWX}	2, 3	Data valid to WR transition	10		$t_{CLCL}-40$		ns
t_{WHQX}	2, 3	Data hold after WR	10		$t_{CLCL}-40$		ns
t_{RLAZ}	2, 3	RD low to address float		0		0	ns
t_{WHLH}	2, 3	RD or WR high to ALE high	10	90	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	5	High time	20		20		ns
t_{CLCX}	5	Low time	20		20		ns
t_{CLCH}	5	Rise time		20		20	ns
t_{CHCL}	5	Fall time		20		20	ns
Shift Register							
t_{XLXL}	4	Serial port clock cycle time	600		$12t_{CLCL}$		ns
t_{QVXH}	4	Output data setup to clock rising edge	367		$10t_{CLCL}-133$		ns
t_{XHDX}	4	Output data hold after clock rising edge	20		$2t_{CLCL}-80$		ns
t_{XHDX}	4	Input data hold after clock rising edge	0		0		ns
t_{XHDX}	4	Clock rising edge to input data valid		367		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.

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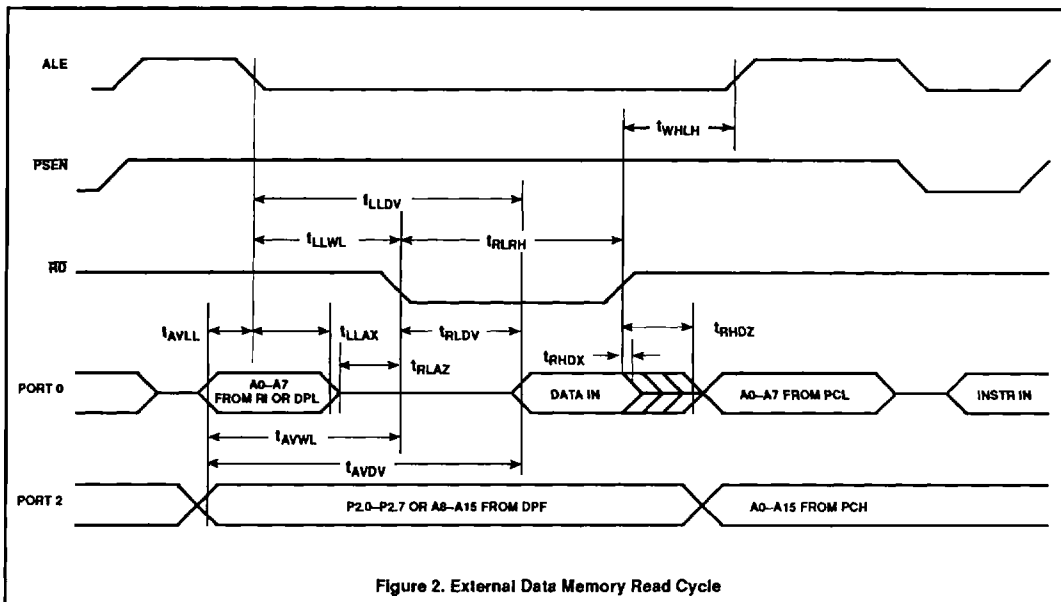
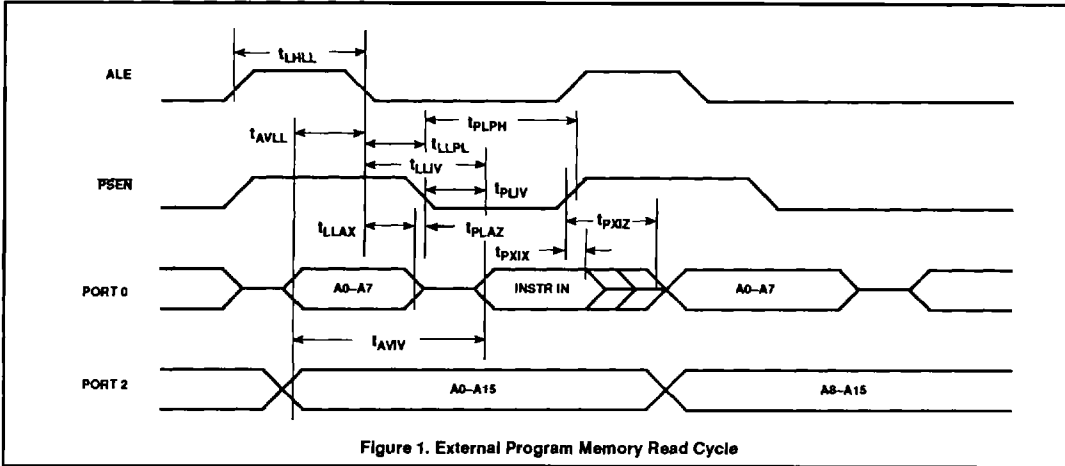
EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A - Address
- C - Clock
- D - Input data
- H - Logic level high
- I - Instruction (program memory contents)
- L - Logic level low, or ALE

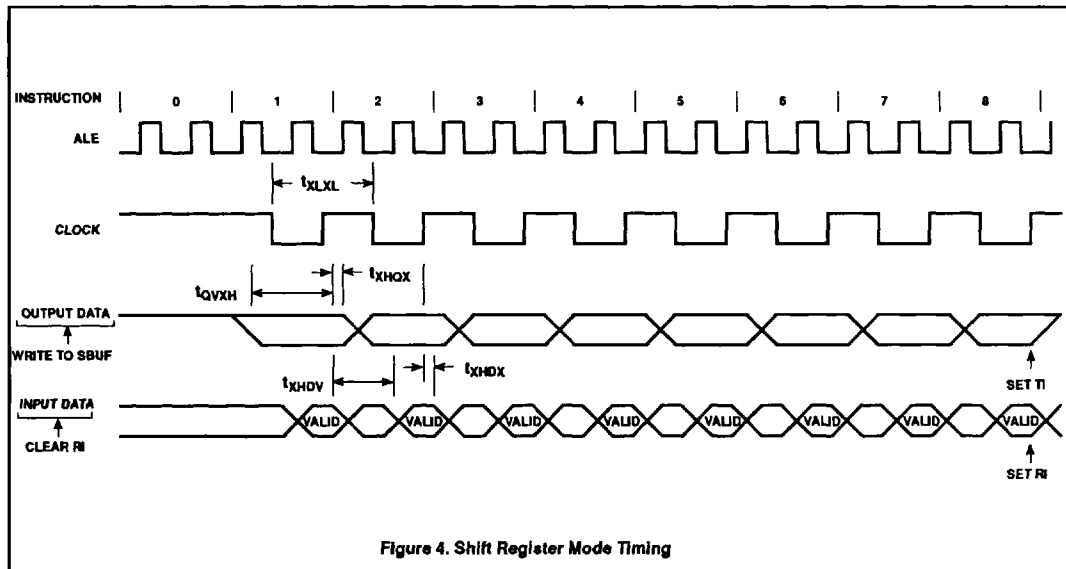
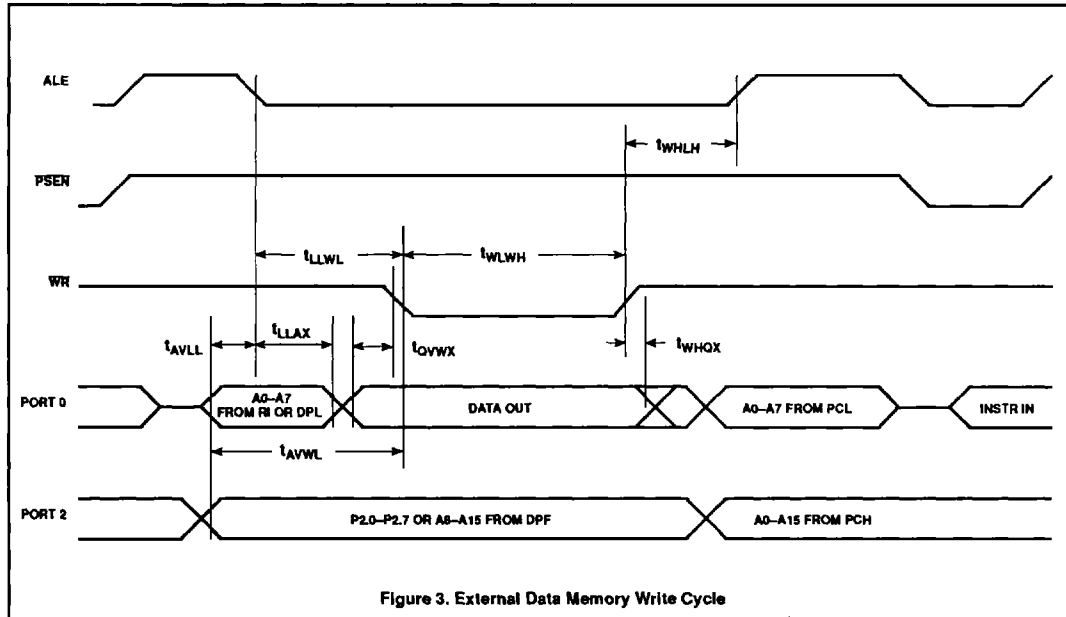
- P - PSEN
- O - Output data
- R - RD signal
- t - Time
- V - Valid
- W - WR signal
- X - No longer a valid logic level
- Z - Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to PSEN low.



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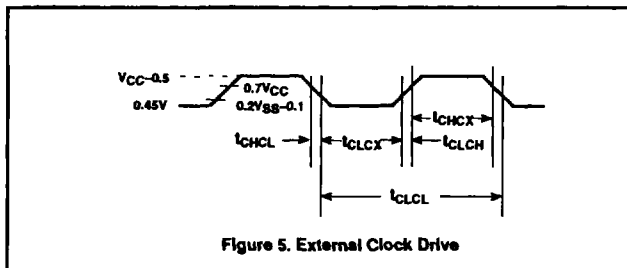


Figure 5. External Clock Drive

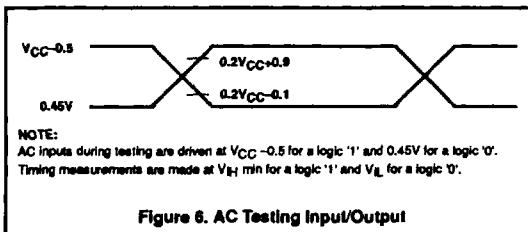


Figure 6. AC Testing Input/Output

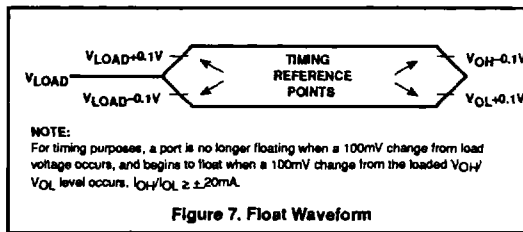
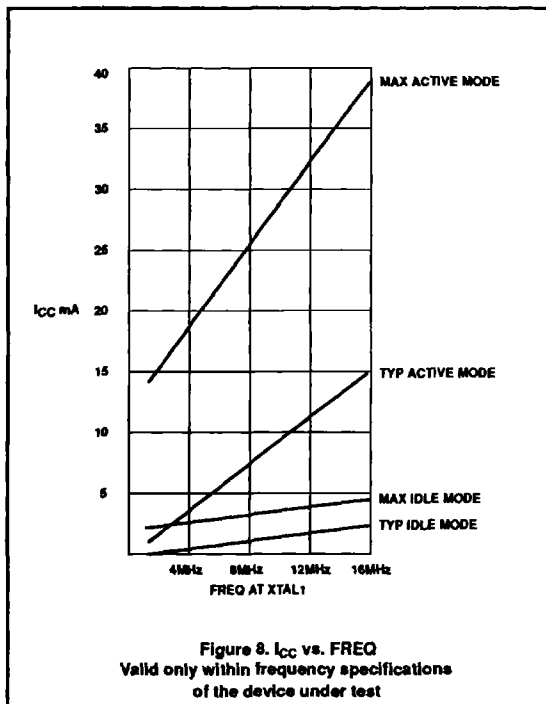
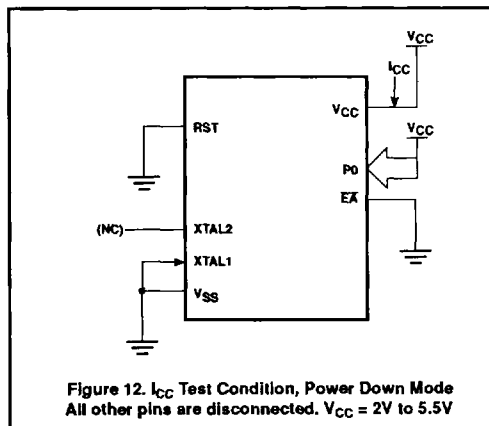
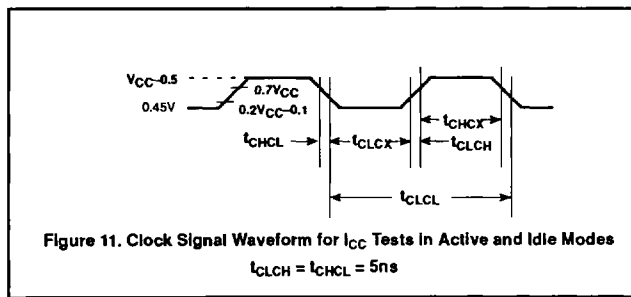
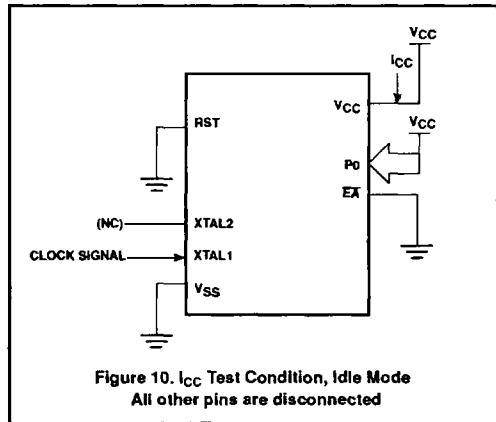
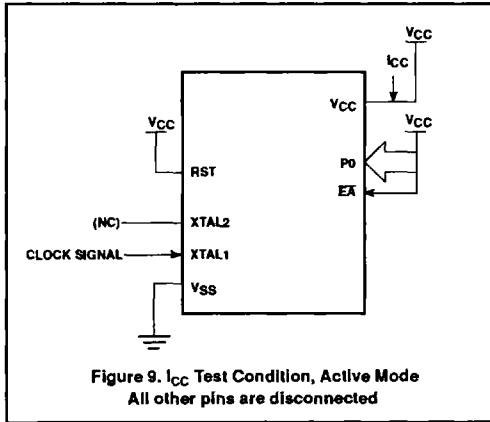


Figure 7. Float Waveform



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EPROM CHARACTERISTICS

The 87C52 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C52 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C52 manufactured by Philips.

Table 2 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 13 and 14. Figure 15 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the 87C52 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 13. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 2 are held at the 'Program Code Data' levels indicated in Table 2. The ALE/PROG is pulsed low 25 times as shown in Figure 14.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the \overline{EA}/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the 'Verify Code Data' levels indicated in Table 2. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = 97H indicates 87C52

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 2, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm². Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 2. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	\overline{EA}/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:

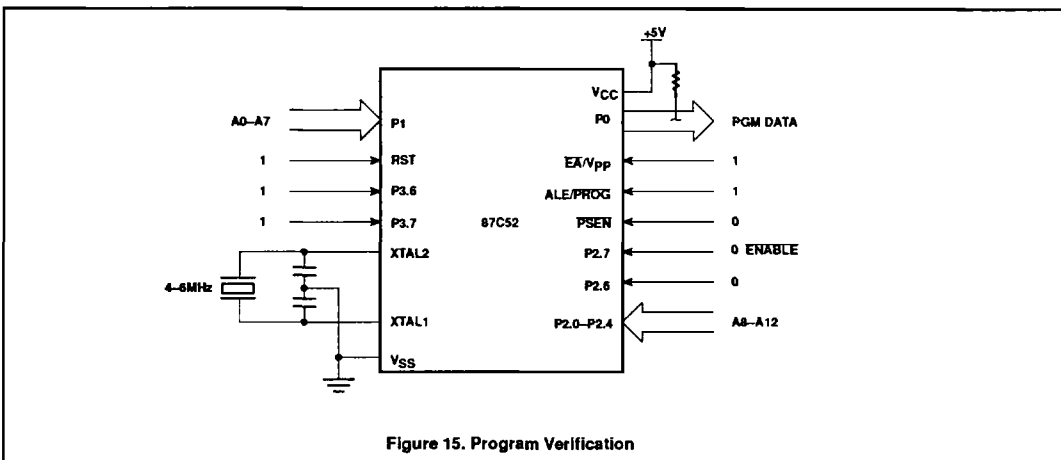
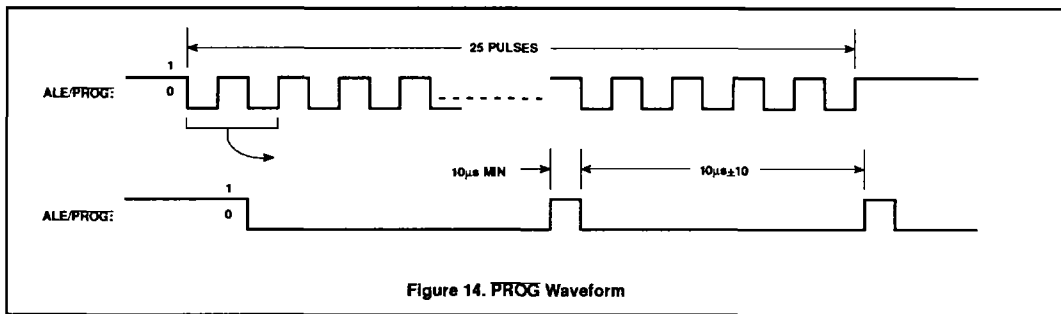
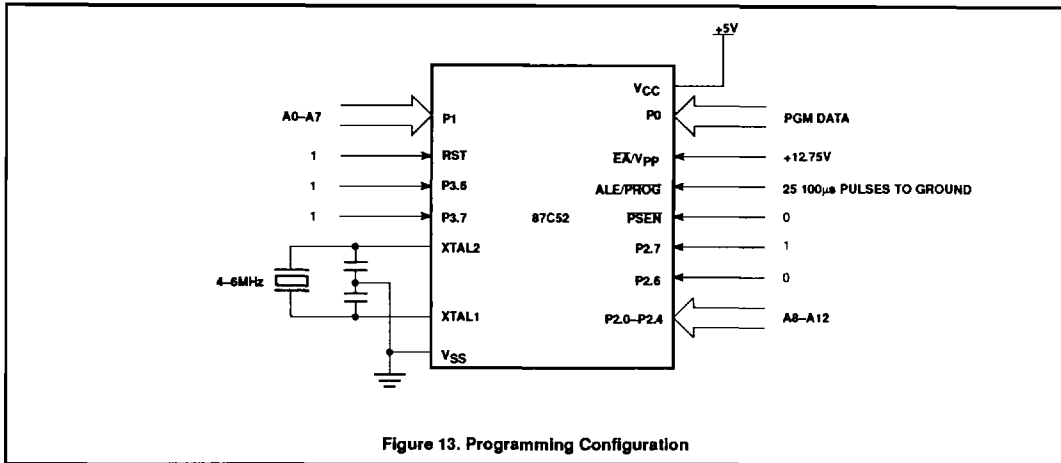
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. $V_{PP} = 12.75V \pm 0.25V$.
3. $V_{CC} = 5V \pm 10\%$ during programming and verification.

*ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100μs ($\pm 10\mu s$) and high for a minimum of 10μs.

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CMOS single-chip 8-bit microcontroller

80C32/80C52/87C52



CMOS single-chip 8-bit microcontroller

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V _{PP}	Programming supply voltage	12.5	13.0	V
I _{PP}	Programming supply current		50	mA
1/t _{CLCL}	Oscillator frequency	4	6	MHz
t _{AVGL}	Address setup to PROG low	48t _{CLCL}		
t _{GHAX}	Address hold after PROG	48t _{CLCL}		
t _{DVGL}	Data setup to PROG low	48t _{CLCL}		
t _{GHDX}	Data hold after PROG	48t _{CLCL}		
t _{ESH}	P2.7 (ENABLE) high to V _{PP}	48t _{CLCL}		
t _{SHGL}	V _{PP} setup to PROG low	10		μs
t _{GHSL}	V _{PP} hold after PROG	10		μs
t _{GLGH}	PROG width	90	110	μs
t _{AVQV}	Address to data valid		48t _{CLCL}	
t _{ELQV}	ENABLE low to data valid		48t _{CLCL}	
t _{EHQZ}	Data float after ENABLE	0	48t _{CLCL}	
t _{GHGL}	PROG high to PROG low	10		μs

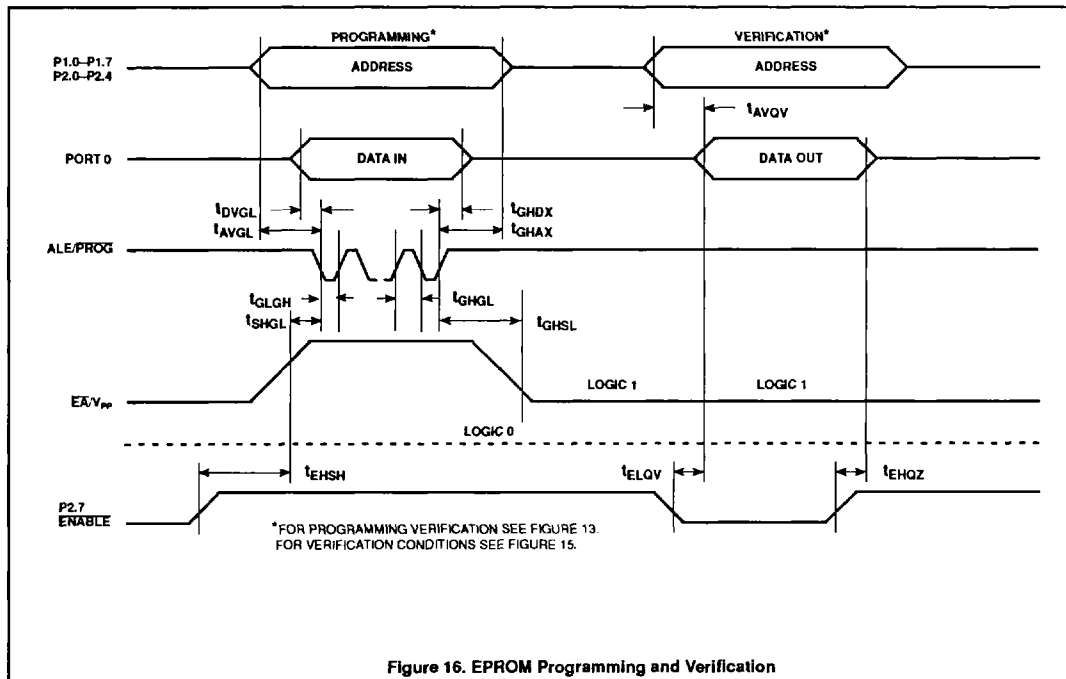


Figure 16. EPROM Programming and Verification