Triple Line Receiver

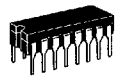
MC10114

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmit trigger, allowing single–ended driving of the inputs, or other applications where a stable reference voltage is necessary. See MECL Design Handbook (HB205) pages 226 and 228.



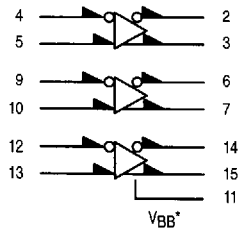
L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

P_D = 145 mW typ/pkg
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
t_r, t_f = 2.1 ns typ (20% to 80%)

LOGIC DIAGRAM

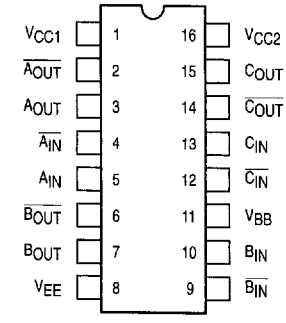


V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

*V_{BB} to be used to supply bias to the MC10114 only and bypassed (when used) with 0.01 µF to 0.1 µF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, its respective output pin with bubble goes positive.

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		39		28	35		39	mAdc
Input Current	I_{inH}	4		70			45		45	µAdc
	I_{CBO}	4		1.5			1.0		1.0	µAdc
Output Voltage Logic 1	V_{OH}	2 3	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		−1.655 −1.655			−1.630 −1.630		−1.595 −1.595	Vdc
Reference Voltage	V_{BB}	11	−1.420	−1.280	−1.350		−1.230	−1.295	−1.150	Vdc
Common Mode Rejection Test	V_{OH}	2 3	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
	V_{OL}	2 3	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Switching Times (50Ω Load)			Min	Max	Min	Typ	Max	Min	Max	ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.0 1.0 1.0 1.0	4.4 4.4 4.4 4.4	1.0 1.0 1.0 1.0	2.4 2.4 2.4 2.4	4.0 4.0 4.0 4.0	0.9 0.9 0.9 0.9	4.3 4.3 4.3 4.3	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	1.5 1.5	3.8 3.8	1.5 1.5	2.1 2.1	3.5 3.5	1.5 1.5	3.7 3.7	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	1.5 1.5	3.8 3.8	1.5 1.5	2.1 2.1	3.5 3.5	1.5 1.5	3.7 3.7	

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}
–30°C	–0.890	–1.890	–1.205	–1.500	From Pin 11
+25°C	–0.810	–1.850	–1.105	–1.475	
+85°C	–0.700	–1.825	–1.035	–1.440	

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Unit
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	
Power Supply Drain Current		I_E	8		4, 9, 12			5, 10, 13	mAdc
Input Current		I_{inH}	4	4	9, 12			5, 10, 13	µAdc
		I_{inL}	4		9, 12			5, 10, 13	µAdc
Output Voltage	Logic 1	V_{OH}	2 3	4 9, 12	9, 12 4			5, 10, 13 5, 10, 13	Vdc
Output Voltage	Logic 0	V_{OL}	2 3	9, 12 4	4 9, 12			5, 10, 13 5, 10, 13	Vdc
Threshold Voltage	Logic 1	V_{OHA}	2 3	 9, 12	9, 12	4	 4	5, 10, 13 5, 10, 13	Vdc
Threshold Voltage	Logic 0	V_{OLA}	2 3	9, 12	 9, 12	 4	4	5, 10, 13 5, 10, 13	Vdc
Reference Voltage		V_{BB}	11					5, 10, 13	Vdc
Common Mode Rejection Test		V_{OH}	2 3						Vdc
		V_{OL}	2 3						Vdc
Switching Times	(50Ω Load)					Pulse In	Pulse Out		
Propagation Delay		t_{4+2+}	2			4	2	5, 10, 13	ns
		t_{4-2-}	2			4	2	5, 10, 13	
		t_{4+3-}	3			4	3	5, 10, 13	
		t_{4-3+}	3			4	3	5, 10, 13	
Rise Time	(20 to 80%)	t_{2+}	2			4	2	5, 10, 13	
		t_{3+}	3			4	3	5, 10, 13	
Fall Time	(20 to 80%)	t_{2-}	2			4	2	5, 10, 13	
		t_{3-}	3			4	3	5, 10, 13	

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
–30°C	+0.110	–0.890	–1.890	–2.890	–5.2
+25°C	+0.190	–0.850	–1.810	–2.850	–5.2
+85°C	+0.300	–0.825	–1.700	–2.825	–5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4					8	1, 16
		I_{inL}	4					8, 4	1, 16
Output Voltage	Logic 1	V_{OH}	2 3					8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 3					8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 3					8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 3					8 8	1, 16 1, 16
Reference Voltage		V_{BB}	11					8	1, 16
Common Mode Rejection Test		V_{OH}	2 3	4	5	 5	 4	8 8	1, 16 1, 16
		V_{OL}	2 3	 4	 5	5	4	8 8	1, 16 1, 16
Switching Times	(50Ω Load)							**–3.2 V**	**+2.0 V**
Propagation Delay		t_{4+2+}	2					8	1, 16
		t_{4-2-}	2					8	1, 16
		t_{4+3-}	3					8	1, 16
		t_{4-3+}	3					8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2					8	1, 16
		t_{3+}	3					8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2					8	1, 16
		t_{3-}	3					8	1, 16

* V_{IHH} = Input Logic 1 level shifted positive one volt for common mode rejection tests
V_{ILH} = Input Logic 0 level shifted positive one volt for common mode rejection tests
V_{IHL} = Input Logic 1 level shifted negative one volt for common mode rejection tests
V_{ILL} = Input Logic 0 level shifted negative one volt for common mode rejection tests

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.