

ADC-HX, ADC-HZ Series

12-Bit, Analog-to-Digital Converters

FEATURES

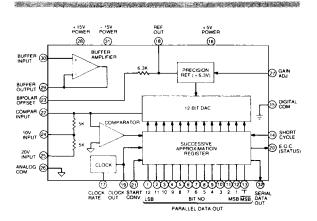
- · 12-Bit resolution
- · 8-or 20-Microseconds conversions
- 5 Input ranges
- Internal high Z buffer
- · Short-cycle operation

GENERAL DESCRIPTION

The ADC-HX12B and ADC-HZ12B are self-contained, high performance, 12-bit A/D converters manufactured with thick-and thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12-bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

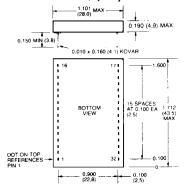
These converters utilize a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12-bit successive approximation register, a clock and a monolithic buffer amplifier. Nonlinearity is specified at ±1/2 LSB maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3 microseconds, the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary two's complement. Serial data is also brought out. The package is a 32-pin ceramic case.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE. ± 0.01"

INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|------------------|-----|----------------|
| 1 | BIT 12 OUT (LSB) | 17 | CLOCK RATE |
| 2 | BIT 11 OUT | 18 | REF OUT |
| 3 | BIT 10 OUT | 19 | CLOCK OUT |
| 4 | BIT 9 OUT | 20 | EOC (STATUS) |
| 5 | BIT 8 OUT | 21 | START CONVERT |
| 6 | BIT 7 OUT | 22 | COMPAR INPUT |
| 7 | BIT 6 OUT | 23 | BIPOLAR OFFSET |
| 8 | BIT 5 OUT | 24 | 10V RANGE |
| 9 | BIT 4 OUT | 25 | 20V RANGE |
| 10 | BIT 3 OUT | 26 | ANALOG COM |
| 11 | BIT 2 OUT | 27 | GAIN ADJ |
| 12 | BIT 1 OUT (MSB) | 28 | + 15V POWER |
| 13 | BIT 1 OUT (MSB) | 29 | BUFFER OUTPUT |
| 14 | SHORT CYCLE | 30 | BUFFER INPUT |
| 15 | DIGITAL COM | 31 | - 15V POWER |
| 16 | +5V POWER | 32 | SERIAL OUTPUT |



FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +15V and +5V supplies unless otherwise noted.

| INPUTS | ADC-HX12B ADC-HZ12B |
|--|--|
| Analog Input Ranges, unipolar Analog Input Ranges, bipolar Input Impedance | ±2.5V, ±5V, ±10V FS 2.5K (0 to +5V, ±2.5V) 5K (0 to +10V, ±5V) |
| Input Impedance with Buffer Input Bias Current of Buffer Input Overvoltage | 125 nA typical, 250 nA max. + 15V |
| OUTPUTS! | resets converter and initiates next conversion. Loading: 2 TTL loads |

| Parallel Output Data | 12 parallel lines of data held until next conversion command. V_{OUT} ("0") $\leq +0.4V$ V_{OUT} ("1") $\geq +2.4V$ |
|----------------------------|---|
| Coding, unipolar | Complementary Binary |
| Coding, bipolar | Complementary Offset Binary Complementary Two's |
| | Complement |
| Serial Output Data | NRZ successive decision pulses |
| | out, MSB first. Compl. Binary or Compl. Offset Binary Coding |
| End of Conversion (Status) | Conversion status signal. Output |
| | is logic "1" during reset and |
| | conversion and logic "0" when conversion complete. |
| Clock Output | Train of positive going +5V 100 |
| | nsec. pulses. 600 kHz for ADC- HX12B and 1.5 MHz for ADC- |
| | HZ12B (pin 17 grounded). |
| | |

PERFORMANCE

POWER REQUIREMENTS

| Power Supply Voltage | + 15V dc ± 0.5V dc at 20 mA |
|----------------------|----------------------------------|
| | $-15V$ dc $\pm 0.5V$ dc at 25 mA |
| | + 5V dc ± 0.25V dc at 85 mA |

PHYSICAL/ENVIRONMENTAL

| Operating Temperature Range | |
|-----------------------------|------------------------------|
| | or -55 to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Package Size | 1.700 x 1.100 x 0.160 inches |
| Package Type | 32 pin ceramic |
| Pins | 0.010 x 0.018 inch Kovar |
| Weight | 0.5 ounces (14 grams) |
| | · · · · |

FOOTNOTES:

- 1. All digital outputs can drive 2 TTL loads
- 2. Without buffer amplifier used. ADC-HZ12B may require external adjustment of
- 3. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ± 10V input
- 4. Short cycled operation.

TECHNICAL NOTES

- 1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01 µF ceramic capacitor in parallel with a 1 µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10 μF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01 µF ceramic capacitor. These precautions will assure noise free operation of the converter.
- 2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V dc ground should be run to pin 15.
- 3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/ °C cermet types. The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.
- 4. Short-cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases the clock rate is also speeded up by connecting the clock rate adjust (pin 17) to +5V dc (10 bits) or +15V dc (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.



- 5. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary or complementary 2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of -1.0000). The converter is then calibrated so that -FS analog input gives an output code of 0000 0000 0000, and +FS-1 LSB gives 1111 1111 1111.
- 6. These converters dissipate 1.7 watts maximum of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
- 7. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see clock rate adjustment diagram) for the converter resolution selected. The pulse width of the external clock should be between 100 nanoseconds and 300 nanoseconds. Each N-bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N-bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.
- 8. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between the input level change. such as a multiplexer channel change, and the negativegoing edge of the START CONVERSION pulse. If the buffer is not required, its input (pin 30) should be tied to ANALOG GROUND (pin 26). This prevents the unused amplifier from introducing noise into the converter. For applications not using the internal buffer, the converter must be driven from a source with an extremely low input impedance.

CONNECTIONS AND CALIBRATION

Input Connections

| INPUT VOLT. RANGE | WITHOUT BUFFER | | | WITH BUFFER | | | |
|---|----------------------------------|--------------------|--|----------------------------------|--------------------|--|---|
| | INPUT PIN | | T THESE GETHER | INPUT | | NNECT THE | |
| 0 to +5V 0 to +10V ±2.5V ±5V ±10V | 24 24 24 24 24 25 | 22 & 25 22 & 25 | 23 & 26 23 & 26 23 & 22 23 & 22 23 & 22 23 & 22 | 30 30 30 30 30 30 | 22 & 25 22 & 25 | 23 & 26 23 & 26 23 & 22 23 & 22 23 & 22 23 & 22 | 29 & 24 29 & 24 29 & 24 29 & 24 29 & 25 |

CALIBRATION PROCEDURE

1. Connect the converter for bipolar or unipolar operation. Use the input connection table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nanoseconds minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.

2. Zero and Offset Adjustments

Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + 1/2 LSB) or the bipolar offset adjustment (-FS+1/2 LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.

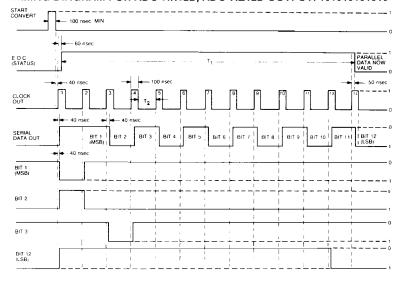
3. Full Scale Adjustment

Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS-11/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

TIMING DIAGRAM **OPERATING PERIODS** ADC-HX12B ADC-HZ12B

T, 20 µsec. 8.0 µsec. 1.56 µsec. 0.56 usec.

TIMING DIAGRAM FOR ADC-HX12B, ADC-HZ12B OUTPUT: 101010101010





Calibration Table

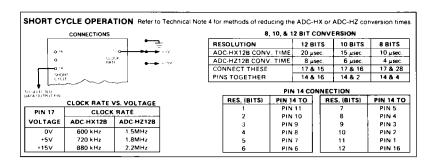
| UNIPOLAR RANGE | ADJUST. | INPUT VOLTAGE |
|----------------|----------------|------------------------|
| 0 to +5V | ZERO GAIN | + 0 6 mV + 4 9982V |
| 0 to +10V | ZERO GAIN | + 1 2 mV + 9 9963V |
| BIPOLAR RANGE | | |
| ± 2.5V | OFFSET GAIN | - 2 4994V + 2 4982V |
| ± 5V | OFFSET GAIN | - 4 9988V + 4 9963V |
| <u>+</u> 10V | OFFSET GAIN | - 9 9976V + 9 9927V |

Coding Table, Unipolar Operation

| INPUT | COMP. BINARY CODING | | |
|-----------|------------------------|-----------|---------|
| 0 TO +10V | 0 TO +5V | MSB | LSB |
| +9 9976V | + 4 9988V | 0000 00 | 00 0000 |
| + 8.7500 | + 4 3750 | 0001 11 | 11 1111 |
| + 7 5000 | + 3 7500 | 0011 11 | 11 *111 |
| + 5.0000 | + 2 5000 | 0111 11 | 11 1111 |
| + 2 5000 | + 1 2500 | 1011 11 | 11 1111 |
| + 1 2500 | + 0 6250 | 1101 11 | 11 1111 |
| + 0 0024 | +0.0012 | 1111 11 | 11 '110 |
| 0.0000 | 0.0000 | . 1111 11 | 11 1111 |

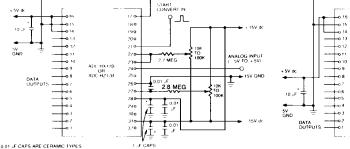
Coding Table, Bipolar Operation

| INPUT VOLTAGE RANGE | | | COMP. OFFSET BINARY | | COMP. TWO'S COMPLEMENT | |
|----------------------------|------------|-----------|------------------------|-----------|---------------------------|-----------|
| ± 10V | ± 5V | 2.5V | MSB | LSB | MSB | LSE |
| + 9 9951V | + 4 9976V | + 2 4988V | 0000 0 | 0000 0000 | 1000 | 0000 0000 |
| + 7 5000 | ; + 3.7500 | 1 8750 | 0001 1 | 111 1111 | 1001 | 1111 1111 |
| 5 0000 | 1 2 5000 | 1 1 2500 | 0011 1 | 111 1111 | 1011 | 1111 1111 |
| 0.0000 | 0 0000 | 0 0000 | 0111 1 | 111 1111 | 1111 | 1111 1111 |
| 5 0000 | 2 5000 | 1.2500 | 1011 1 | 111 1111 | 0011 | 1111 1111 |
| 7 5000 | 3 7500 | 1.8750 | 1101 1 | 111 1111 | 0101 | 1111 1111 |
| 9 9951 | 4 9976 | 2 4988 | 1111 1 | 111 7110 | 0111 | 1111 1110 |
| 10 0000 | 5 0000 | 2 5000 | | 111 1111 | 0111 | 1111 1111 |



BIPOLAR OPERATION, -5V TO +5V

UNIPOLAR OPERATION, 0 TO +10V



| | r | | START CONVERT IN |
|----------|-----------------|-----------------|--|
| | 0 16 | | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, |
| | o 15 | | 18 0 + 15V dc |
| | 0 14 | | 190 |
| | 0 13 | | 200 |
| | a 12 | | 21 C 10K |
| | 011 | | 22 0 TO ANALOG INPUT |
| | O 10 | | 230 2.7 MEG (0 TO + 10V) |
| + 5V dc | 9 | ADC-HX12B | |
| | ∐ 8 | OR ADC HZ12B | 250 15V GND |
| | ─ | | 260 ± 2.8 MEG ≥10K = |
| 10 "F" 🛨 | | | 270 + 3 VVV 510 |
| | | | 280 +1 1 0 01 |
| 5V - | 4 | | 290 AT T # |
| GND - | | | 300 /主 章 |
| DATA | 02 | | 310 - 15V dc |
| OUTP | JTS | | 32° 1 T T |
| | L | | |
| | | | 1 "F CAPS 0.01 "F CAPS ARE CERAMIC TYPES |
| | | | |

ORDERING INFORMATION

| MODEL | TEMP. RANGE | SEAL | |
|-------------|----------------|----------|--|
| ADC-HX12BGC | 0 to +70 °C | Ероху | |
| ADC-HX12BMC | 0 to +70 °C | Hermetic | |
| ADC-HX12BMM | -55 to +125 °C | Hermetic | |
| ADC-HX/883B | -55 to +125 °C | Hermetic | |
| ADC-HZ12BGC | 0 to +70 °C | Epoxy | |
| ADC-HZ12BMC | 0 to +70 °C | Hermetic | |
| ADC-HZ12BMM | -55 to +125 °C | Hermetic | |
| ADC-HZ/883B | -55 to +125 °C | Hermetic | |
| | | | |

MIL-STD-883B units are available under DESC Drawing Number 5962-88508.