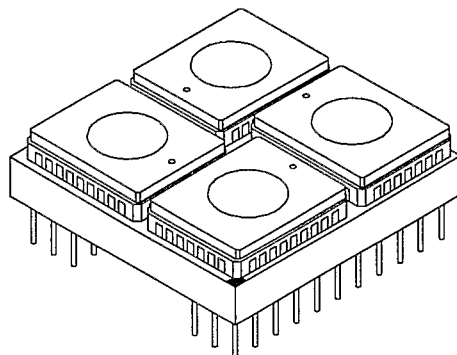


DESCRIPTION:

The DPV6432V is a 66-pin Pin Grid Array (PGA) consisting of four 64K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

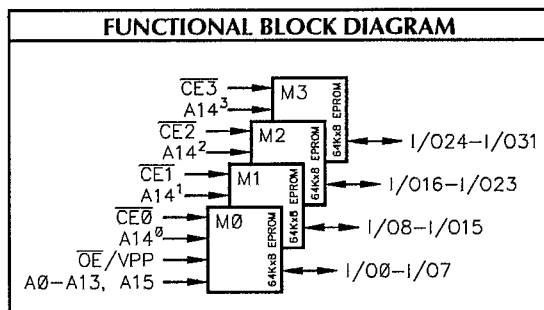
The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors.



FEATURES:

- Organizations Available:
256K X 8, 128K X 16 or 64K X 32
- Access Times:
55*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

* Commercial only.

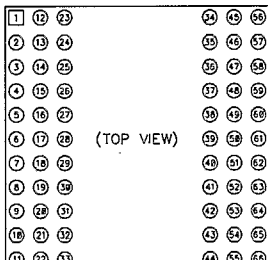


PIN NAMES	
A0-A13, A14 ⁰ -A14 ³ , A15	Address Inputs
I/O0-I/O31	Data In/Out
$\overline{CE0} - \overline{CE3}$	Chip Enables
\overline{OE} / V_{PP}	Output Enable / Programming Voltage
VDD	Power (+5V)
VSS	Ground
N.C.	No Connect

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PIN-OUT DIAGRAM

1 I/O8	12 $\overline{WE1}$	23 I/O14	34 I/O24	45 VDD	56 I/O30
2 I/O9	13 $\overline{CE1}$	24 I/O13	35 I/O25	46 $\overline{CE3}$	57 I/O29
3 I/O10	14 VSS	25 I/O12	36 I/O26	47 $\overline{WE3}$	58 I/O28
4 A13	15 I/O15	26 I/O11	37 A6	48 I/O31	59 I/O27
5 A15	16 A10	27 \overline{OE}/V_{PP}	38 A7	49 A3	60 A0
6 N.C.	17 A11	28 N.C.	39 N.C.	50 A4	61 A1
7 N.C.	18 A12	29 $\overline{WE0}$	40 A8	51 A5	62 A2
8 N.C.	19 VDD	30 I/O6	41 A9	52 $\overline{WE2}$	63 I/O22
9 I/O0	20 $\overline{CE0}$	31 I/O5	42 I/O16	53 $\overline{CE2}$	64 I/O21
10 I/O1	21 N.C.	32 I/O4	43 I/O17	54 VSS	65 I/O20
11 I/O2	22 I/O7	33 I/O3	44 I/O18	55 I/O23	66 I/O19



(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS¹

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ²	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ²	-0.5 to +7.0	V
V _{PP}	Programming Voltage ²	-0.5 to +13.0	V

RECOMMENDED OPERATING RANGE²

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage ⁴	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	-0.1		0.8	V
V _{PP}	V _{PP} Supply Voltage ⁵	12.25	12.5	12.75	V

CAPACITANCE³: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	15	pF	V _{IN} = 0V
C _{ADR}	Address Input	50		
C _{OE}	Output Enable/V _{PP}	130		
C _{I/O}	Data Input/Output	25		

AC TEST CONDITIONS: Including Programming

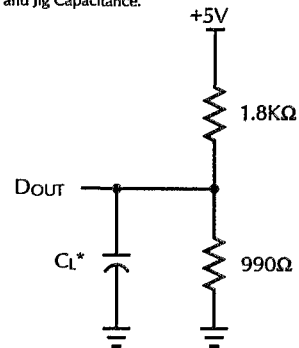
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

Output Load

Float	C _L	Parameters Measured
1	100 pF	except t _{DF} and t _{DFP}
2	5 pF	t _{DF} and t _{DFP}

Figure 1. Output Load

* Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS⁶: Over operating ranges

Symbol	Characteristics	Test Conditions	X8		X16		X32		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = V _{DD}	-40	40	-40	40	-40	40	μA
I _{OUT}	Output Leakage Current	CE = V _{IH} , V _{IN} = V _{DD} or V _{SS}	-40	40	-20	20	-10	10	μA
I _{CC}	V _{DD} Operation Current, Read	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	120-250ns		60	110	200	mA	
		Cycle = min. Duty = 100%	55-90ns		225	270	360		
I _{SB1}	V _{DD} Standby Current (TTL)	CE = V _{IH} , V _{IN} = V _{IH} or V _{IL}		15	15	15		mA	
I _{SB2}	V _{DD} Standby Current (CMOS)	CE = V _{DD} ± 0.3V, I _{OUT} = 0mA V _{IN} ≥ V _{DD} -0.3V or V _{IN} ≤ 0.3V		2.0	2.0	2.0		mA	
I _{PP1}	V _{PP} Supply Current Programming ⁶	CE, OE = V _{IL} , OE = V _{IH}		60	120	240		mA	
I _{PP3}	V _{PP} Supply Current Read ⁴	CE, OE = V _{IL} , I _{OUT} > 0mA		400	400	400		μA	
V _{OL}	Output LOW Voltage	I _{OUT} = 2.1mA		0.45	0.45	0.45		V	
V _{OH1}	Output HIGH Voltage	I _{OUT} = -400μA	2.4		2.4	2.4		V	
V _{IL}	Input LOW Level		-0.2	0.8	-0.2	0.8	-0.2	0.8	V
V _{IH}	Input HIGH Level		2.2	V _{DD} +1	2.2	V _{DD} +1	2.2	V _{DD} +1	V

FUNCTIONS AND PIN CONNECTIONS					
Mode	Function	CE	OE / V _{PP}	V _{DD}	I/O0-I/O31
Read Operations	Read	L	L	5V	Data Out
	Output Deselect	L	H		High Impedance
	Standby	H	X		High Impedance
Program Operations (T _A = +25 ± 5°C)	Program	L	V _{PP}	6V	Data In
	Program Inhibit	H	V _{PP}		High Impedance
	Program Verify	H	L		Data Out

L = LOW, H = HIGH and X = Don't Care

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges									
No.	Symbol	Parameter	-55*		-70		-90		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACC}	Address Access Time ⁸		55		70		90	ns
2	t _{CE}	Chip Enable to Output Valid ⁷		55		70		90	ns
3	t _{OE}	Output Enable to Output Valid ^{7, 8}		30		30		35	ns
4	t _{DF}	OE or CE HIGH to Output Float ^{3, 9}	0	30	0	30	0	35	ns
5	t _{OH}	Output Hold from Address Change	0		0		0		ns

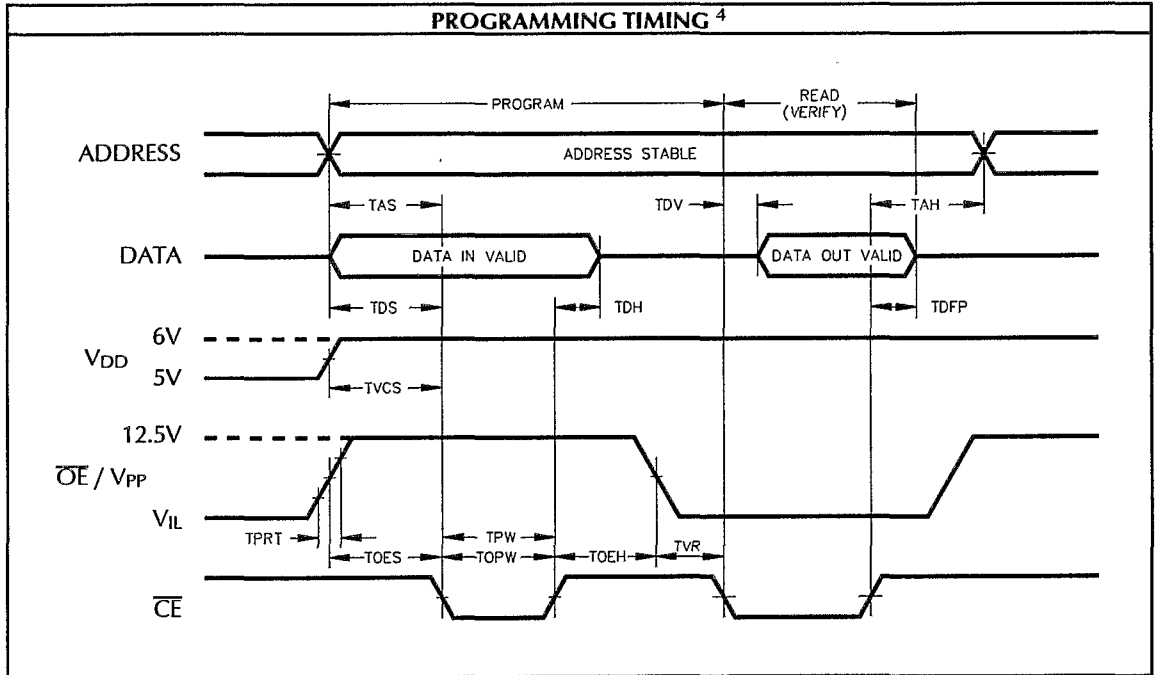
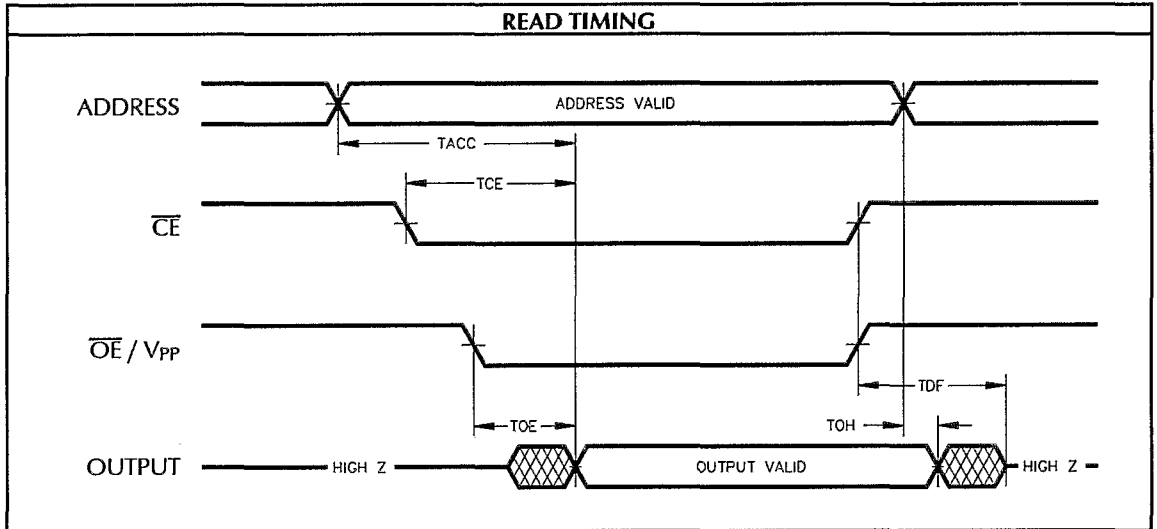
* Commercial only.

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	-120		-150		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACC}	Address Access Time ⁸		120		150		200		250	ns
2	t _{CE}	Chip Enable to Output Valid ⁷		120		150		200		250	ns
3	t _{OE}	Output Enable to Output Valid ^{7, 8}		65		70		75		100	ns
4	t _{DF}	OE or CE HIGH to Output Float ^{3, 9}	0	50	0	50	0	55	0	60	ns
5	t _{OH}	Output Hold from Address Change	0		0		0		0		ns

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AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: T _A = +25°C					
No.	Symbol	Parameter	Min.	Max.	Unit
6	t _{AS}	Address Set-up Time	2		μs
7	t _{OEH}	Output Enable / V _{PP} Hold Time	2		μs
8	t _{OES}	Output Enable / V _{PP} Set-up Time	2		μs
9	t _{DS}	Data Set-up Time	2		μs
10	t _{VCS}	V _{CC} Set-up Time ⁵	2		μs
11	t _{VR}	Output Enable / V _{PP} Recovery Time	2		μs
12	t _{AH}	Address Hold Time	0		μs
13	t _{DH}	Data Hold Time	2		μs
14	t _{DFP}	Output Enable HIGH Output Float Delay ³	0	130	ns
15	t _{PW}	Programming Pulse Width ¹⁰	0.95	1.05	ms
16	t _{OPW}	Over Programming Pulse Width ¹¹	2.85	78.75	ms
17	t _{DV}	Data Valid From Chip Enable		1	μs
18	t _{PRT}	Output Enable / V _{PP} Rise Time During Programming	50		ns





PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure (See *Erasure section*), the DPV6432V contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV6432V through the procedure of programming. A 0.1 μ F capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.0V and +12.5V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode, \overline{CE} is set at V_{IL} , \overline{OE} is set at V_{IH} , V_{DD} is set at +6.0V, and V_{PP} is set at +12.5V. After the applied address and input data signals are stable, programming is accomplished by a 1.0ms V_{IL} pulse on the \overline{CE} pin (refer to the *Programming Timing Diagram*).

The programmed byte is then verified. If the programming was successful, then a 3ms over program pulse is applied. If the programming was unsuccessful after the first 1ms pulse, then up to 25 1ms pulses are applied with a verification after each pulse. When the byte passes, an over program pulse of 3ms times the number of initial programming pulses (78.75ms max.) is applied.

If the device fails to program after 25 attempts, the programming is considered failed. After the first byte is programmed, continue the algorithm through all the required addresses. Then lower V_{DD} and V_{PP} to +5.0Vdc and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

To clear all locations of their programmed contents it is necessary to expose the DPV6432V to an ultraviolet light source. A dosage of 15W-seconds/cm² is required to completely erase a DPV6432V. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (\AA) with an intensity of 12,000 μ W/cm²] for 21 minutes.

The DPV6432V and similar devices can be erased by light sources having wavelengths shorter than 4000 \AA . Although erasure time will be much longer than with UV sources at 2537 \AA , nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV6432V. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

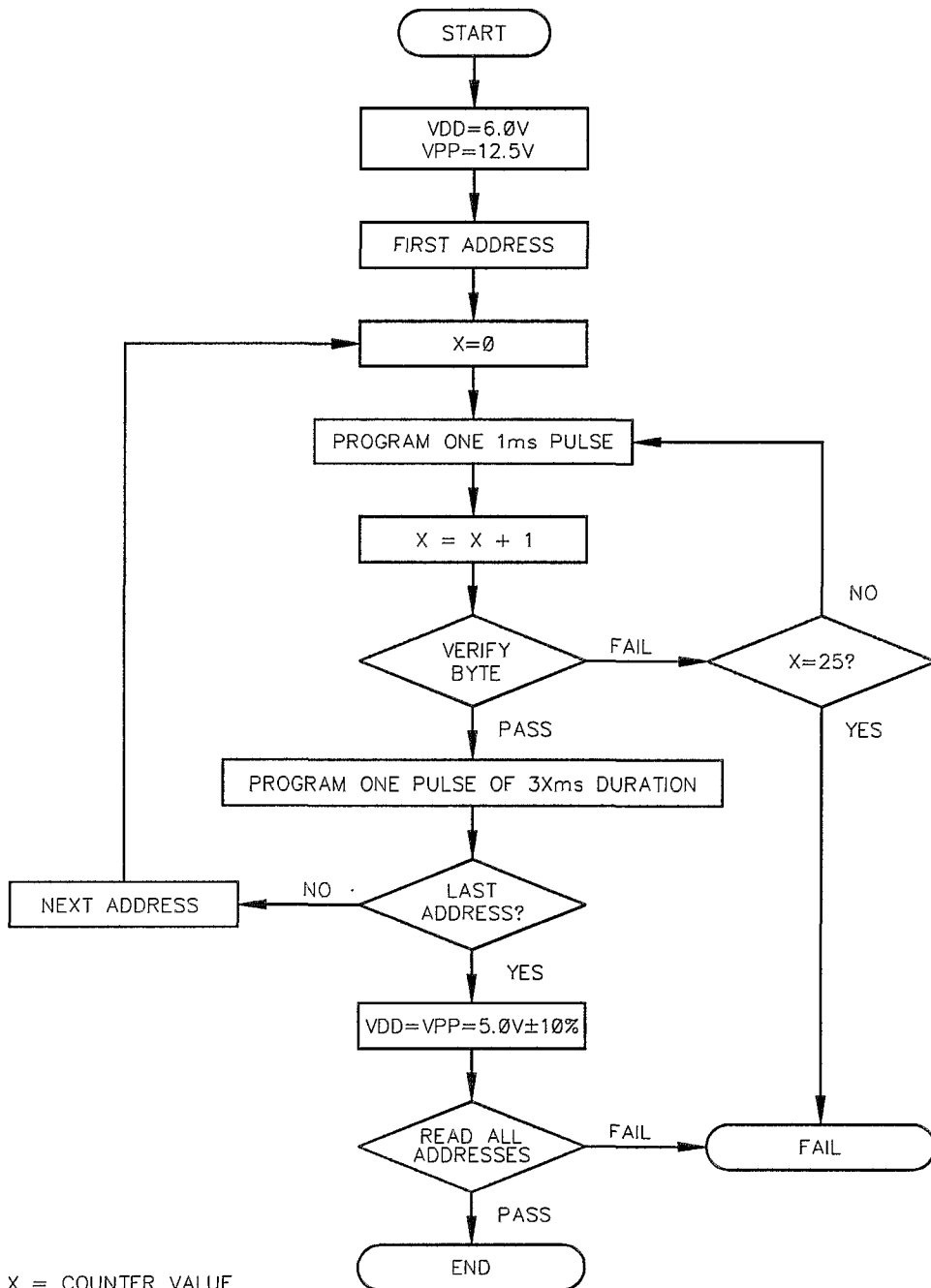
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NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to V_{SS} .
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP} .
5. V_{PP} must not be greater than 13.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with $V_{PP} = 13.0V$. Also, during $\overline{CE} = V_{IL}$, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. $t_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = 5.0V \pm 0.5V$, and $V_{PP} = V_{DD}$ reading. $t_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$ programming.
7. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the following edge of \overline{CE} without impact on t_{CE} .
8. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the following Address is valid without impact on t_{ACC} .
9. T_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first.
10. Initial Program Pulse Width Tolerance is 1ms \pm 5%.
11. The length of the overprogram pulse may vary from 2.85ms to 78.75ms as a function of the iteration counter value X.



Figure 2. Programming Flow Chart



ORDERING INFORMATION

DP V6432 V - XXX X
 PREFIX DEVICE TYPE PACKAGE SPEED GRADE

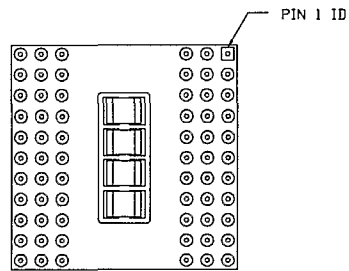
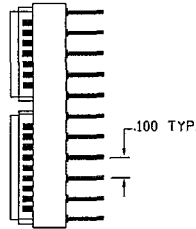
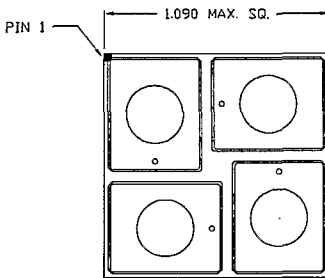
C COMMERCIAL 0°C to +70°C
 I INDUSTRIAL -40°C to +85°C
 M MILITARY -55°C to +125°C
 B* MIL-PROCESSED -55°C to +125°C

55 55ns (COMMERCIAL ONLY)
 70 70ns
 90 90ns
 120 120ns
 150 150ns
 200 200ns
 250 250ns

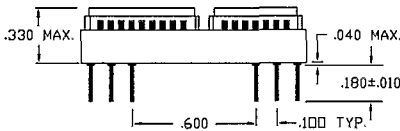
V 66-PIN PGA VERSAPAC
 UVEPROM 256KX8, 128KX16, OR 64KX32

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



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Dense-Pac Microsystems, Inc.

7321 Lincoln Way • Garden Grove, California 92641-1428
 (714) 898-0007 • (800) 642-4477 (Outside CA) • FAX: (714) 897-1772



