Document Title

512Mbit (64Mx8bit / 32Mx16bit) NAND Flash Memory

Revision History

No.	History	Draft Date	Remark
0.0	Initial Draft	Sep.17.2003	Preliminary
0.1	Renewal Product Group	Oct.07.2003	Preliminary
0.2	Make a decision of PKG information	Nov.08.2003	Preliminary
0.3	Append 1.8V Operation Product to Data sheet	Dec.01.2003	Preliminary
0.4	1) Add Errata tWC tWH tWP tRC tREH tRP tREA@ID Read Specification 50 15 25 50 15 30 35 Relaxed value 60 20 40 60 20 40 45 2) Modify the description of Device Operations - /CE Don't Care Enabled(Disabled) -> Sequential Row Read Disabled (Enabled) (Page23) 3) Add the description of System Interface Using /CE don't care (Page39)	Mar.28.2004	Preliminary

FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

NAND INTERFACE

- x8 or x16 bus width.
- Multiplexed Address/ Data
- Pinout compatibility for all densities

SUPPLY VOLTAGE

- 3.3V device: VCC = 2.7 to 3.6V : HY27USXX121M
- 1.8V device: VCC = 1.7 to 1.95V : HY27SSXX121M

Memory Cell Array

- 528Mbit = 528 Bytes x 32 Pages x 4,096 Blocks

PAGE SIZE

- x8 device : (512 + 16 spare) Bytes
  : HY27(U/S)S08121M
- x16 device: (256 + 8 spare) Words
  : HY27(U/S)S16121M

BLOCK SIZE

- x8 device: (16K + 512 spare) Bytes
- x16 device: (8K + 256 spare) Words

PAGE READ / PROGRAM

- Random access: 12us (max)
- Sequential access: 50ns (min)
- Page program time: 200us (typ)

COPY BACK PROGRAM MODE

- Fast page copy without external buffering

CACHE PROGRAM MODE

- Internal Cache Register to improve the program throughput

FAST BLOCK ERASE

- Block erase time: 2ms (Typ)

STATUS REGISTER

ELECTRONIC SIGNATURE

SEQUENTIAL ROW READ OPTION

AUTOMATIC PAGE 0 READ AT POWER-UP OPTION

- Boot from NAND support
- Automatic Memory Download

SERIAL NUMBER OPTION

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions

DATA INTEGRITY

- 100,000 Program/Erase cycles
- 10 years Data Retention

PACKAGE

- HY27US(08/16)121M-T(P)
  : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
  - HY27US(08/16)121M-T (Lead)
  - HY27US(08/16)121M-TP (Lead Free)

- HY27US08121M-V(P)
  : 48-Pin WSOP1 (12 x 17 x 0.7 mm)
  - HY27US08121M-V (Lead)
  - HY27US08121M-VP (Lead Free)

- HY27(U/S)S(08/16)121M-F(P)
  : 63-Ball FBGA (8.5 x 15 x 1.2 mm)
  - HY27US(08/16)121M-F (Lead)
  - HY27US(08/16)121M-FP (Lead Free)
  - HY27SS(08/16)121M-F (Lead)
  - HY27SS(08/16)121M-FP (Lead Free)

DESCRIPTION

The HYNIX HY27(U/S)SXX121M series is a family of non-volatile Flash memories that use NAND cell technology. The devices operate 3.3V and 1.8V voltage supply. The size of a Page is either 528 Bytes (512 + 16 spare) or 264 Words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/ Output signals on a multiplexed x8 or x16 Input/ Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). A Write Protect pin is available to give a hardware protection against program and erase operations.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/ Erase/Read (PER) Controller is currently active. The use of an open-drain output allows the Ready/ Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Each device has a Cache Program feature which improves the program throughput for large files. It loads the data in a Cache Register while the previous data is transferred to the Page Buffer and programmed into the memory array.

The devices are available in the following packages:
- **48-TSOP1** (12 x 20 x 1.2 mm)
- **48-WSOP1** (12 x 17 x 0.7 mm)
- **63-FBGA** (8.5 x 15 x 1.2 mm, 6 x 8 ball array, 0.8mm pitch)

Three options are available for the NAND Flash family:
- Automatic Page 0 Read after Power-up, which allows the microcontroller to directly download the boot code from page 0.
- Chip Enable Dont Care, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.
- A Serial Number, which allows each device to be uniquely identified. The Serial Number options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest HYNIX Sales office.

Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

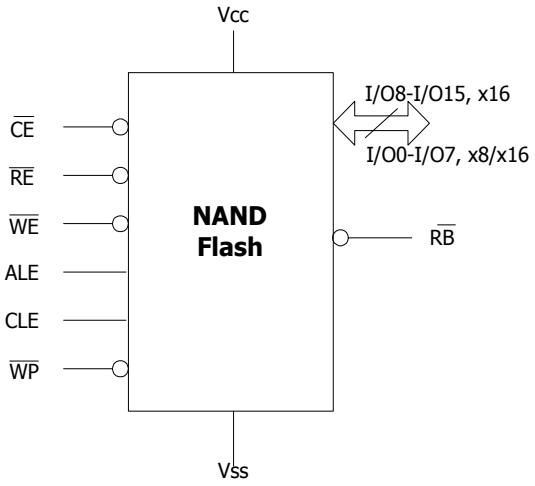


Figure 1: Logic Diagram

I/O_{8-15}	Data Input/Outputs for x16 Device
I/O_{0-7}	Data Input/Output, Address Inputs, or Command Inputs for x8 and x16 device
ALE	Address Latch Enable
CLE	Command Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{RB}$	Read/Busy (open-drain output)
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
VCC	Supply Voltage
VSS	Ground
NC	Not Connected Internally
DU	Do Not Use

Table 1: Signal Name

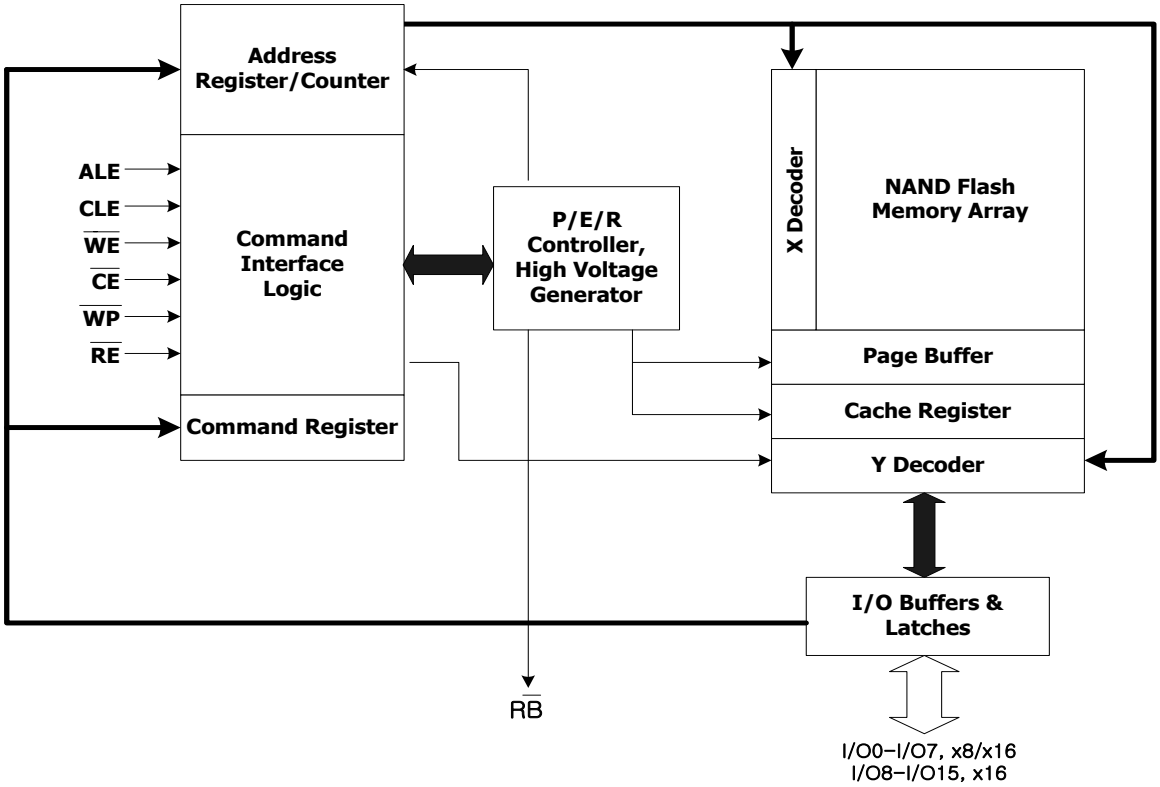


Figure 2. LOGIC BLOCK DIAGRAM

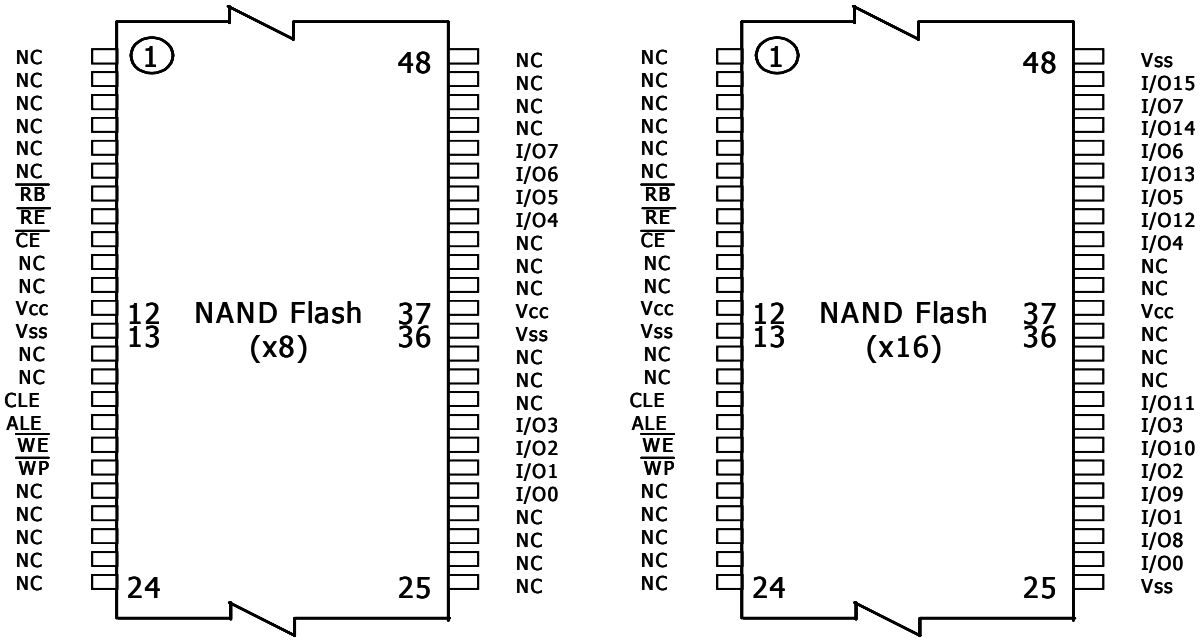


Figure 3. 48-TSOP1 Contactions, x8 and x16 Device

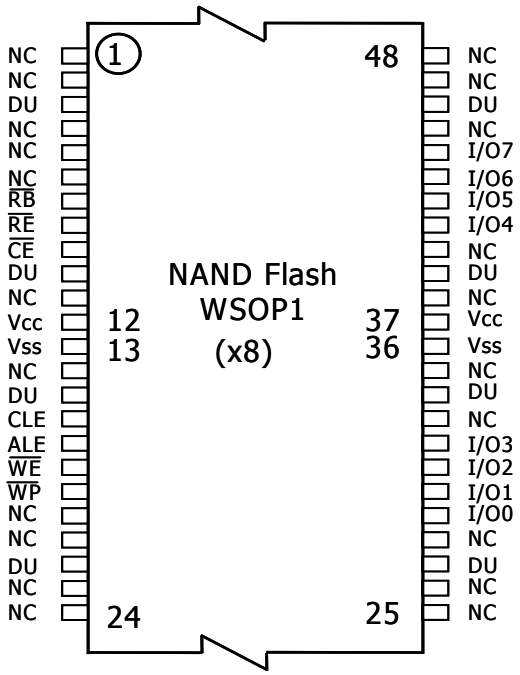


Figure 4. 48-WSOP1 Contactions, x8 Device

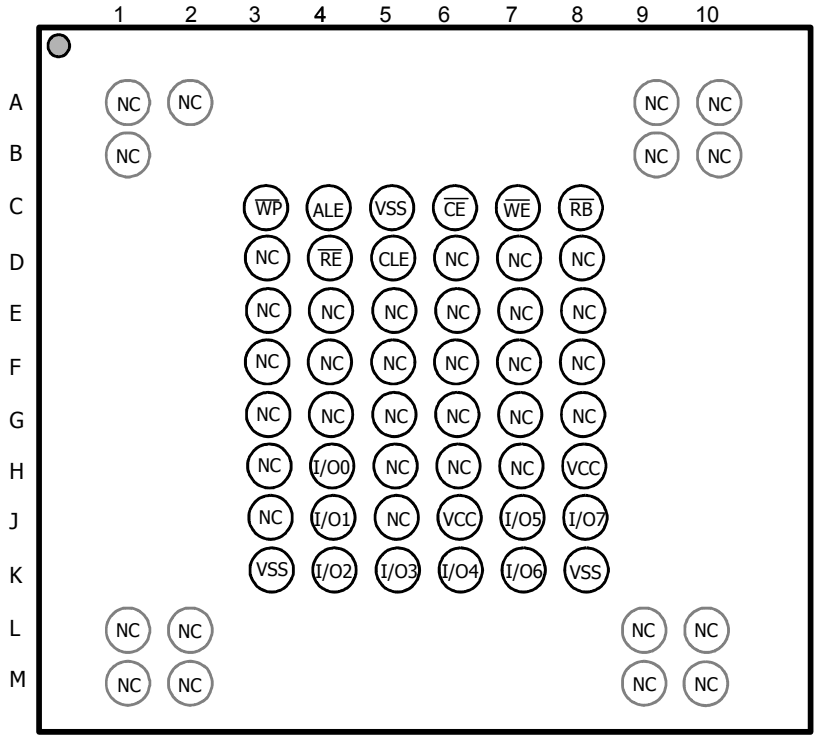


Figure 5. 63-FBGA Contactions, x8 Device (Top view through package)

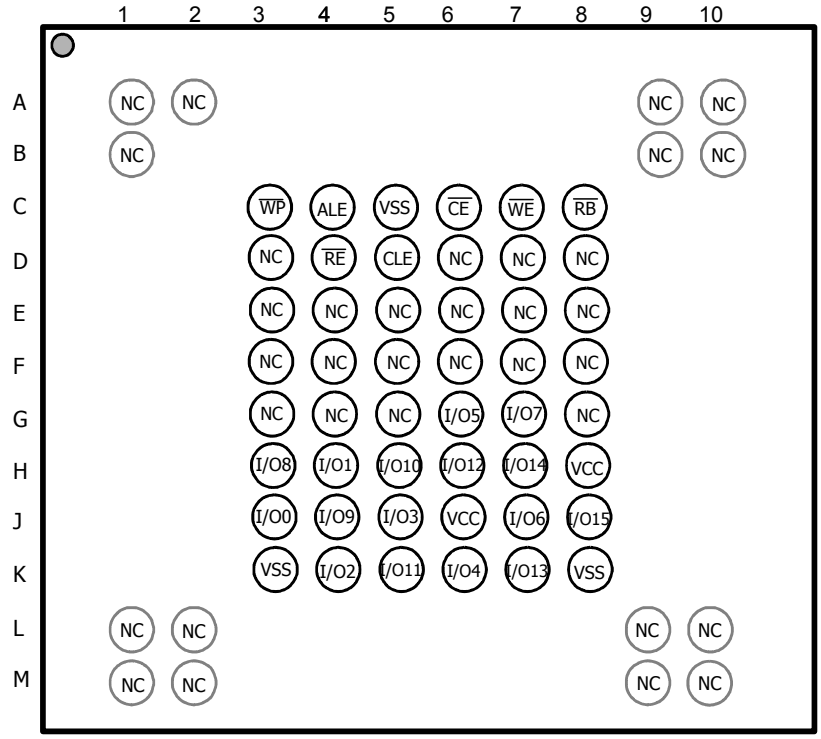


Figure 6. 63-FBGA Contactions, x16 Device (Top view through package)

MEMORY ARRAY ORGANIZATION

The memory array is made up of NAND structures where 16 cells are connected in series.
The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store Error Correction Codes, software flags or Bad Block identification.
In x8 devices the pages are split into a main area with two half pages of 256 Bytes each and a spare area of 16 Bytes. In the x16 devices the pages are split into a 256 Word main area and an 8 Word spare area. Refer to Figure 8, Memory Array Organization.

Bad Blocks

The NAND Flash 528 Byte/ 264 Word Page devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device. The Bad Block Information is written prior to shipping (refer to Bad Block Management section for more details). The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.
These blocks need to be managed using Bad Blocks Management, Block Replacement or Error Correction Codes.

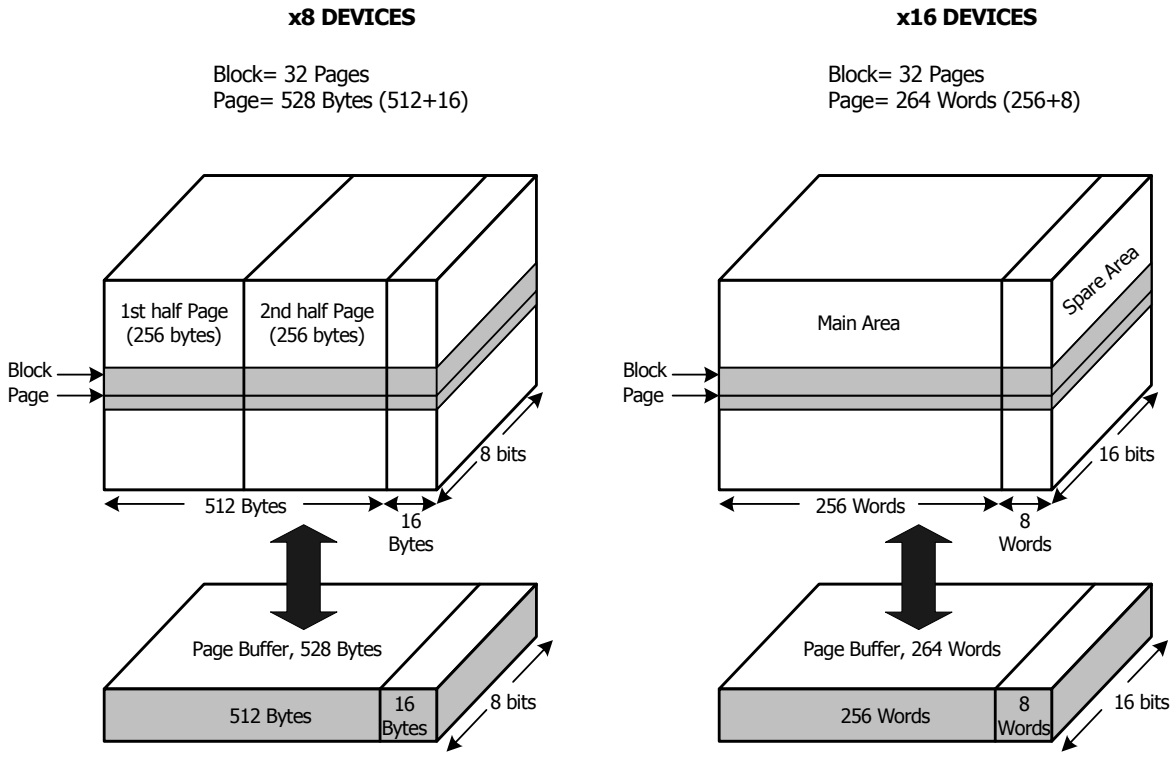


Figure 7. Memory Array Organization

SIGNAL DESCRIPTIONS

See Figure 1, Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Inputs/Outputs (I/O_0-I/O_7)

Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read opertion or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O_0-I/O_7 can be left floating when the device is deselected or the outputs are disabled.

Inputs/Outputs (I/O_8-I/O_{15})

Input/Outputs 8 to 15 are only available in x16 devices. They are used to output the data during a Read operation or input data during a Write operation. Command and Address Inputs only require I/O_0 to I/O_7.

The inputs are latched on the rising edge of Write Enable. I/O_8-I/O_{15} can be left floating when the device is deselected or the outputs are disabled.

Address Latch Enable (ALE)

The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When ALE is high, the inputs are latched on the rising edge of Write Enable.

Command Latch Enable (CLE)

The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CLE is high, the inputs are latched on the rising edge of Write Enable.

Chip Enable ($\overline{CE}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

When the device is executing a Sequential Row Read operation, Chip Enable must be held low (from the second page read onwards) during the time that the device is busy (t_{BLBH1}). If Chip Enable goes high during t_{BLBH1} the operation is aborted.

Read Enable ($\overline{RE}$)

The Read Enable, $\overline{RE}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{RE}$. The falling edge of $\overline{RE}$ also increments the internal column address counter by one.

Write Enable ($\overline{WE}$). The Write Enable input, $\overline{WE}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 1us (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

Write Protect ($\overline{WP}$).

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

Ready/Busy ($\overline{RB}$)

The Ready/Busy output, $\overline{RB}$, is an open-drain output that can be used to identify if the Program/ Erase/ Read (PER) Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/ Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the Ready/Busy Signal Electrical Characteristics section for details on how to calculate the value of the pull-up resistor.

V_{CC} Supply Voltage

V_{CC} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read,program and erase).

An internal voltage detector disables all functions whenever V_{CC} is below 2.5V (for 3V devices) or 1.5V (for 1.8V devices) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{CC} decoupled with a 0.1uF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

V_{SS} Ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

BUS OPERATIONS

There are six standard bus operations that control the memory. Each of these is described in this section, see Tables 2, Bus Operations, for a summary.

Command Input

Command Input bus operations are used to give commands to the memory. Command are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O_0 to I/O_7 are used to input commands. See Figure 21 and Table 14 for details of the timings requirements.

Address Input

Address Input bus operations are used to input the memory address. Four bus cycles are required to input the addresses for the 512Mb devices (refer to Tables 3 and 4, Address Insertion). The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O_0 to I/O_7 are used to input addresses.

See Figure 22 and Table 14 for details of the timings requirements.

Data Input

Data Input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See Figure 23 and Tables 14 and 15 for details of the timings requirements.

Data Output

Data Output bus operations are used to read: the data in the memory array, the Status Register, the Electronic Signature and the Serial Number. Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low. The data is output sequentially using the Read Enable signal.
See Figure 24 and Table 15 for details of the timings requirements.

Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 2. Bus Operation

BUS Operation	$\overline{CE}$	ALE	CLE	$\overline{RE}$	$\overline{WE}$	$\overline{WP}$	I/O_0 - I/O_7	I/O_8 - I/O_{15}(1)
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	X	Data Input	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	X	X	X

Note : (1) Only for x16 devices.
(2) $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 3: Address Insertion, x8 Devices

Bus Cycle	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
1st Cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd Cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd Cycle	A24	A23	A22	A21	A20	A19	A18	A17
4th Cycle	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A25

Note: (1). A8 is set Low or High by the 00h or 01h Command, see Pointer Operations section.
(2). Any additional address input cycles will be ignored.

Table4: Address Insertion, x16 Devices

Bus Cycle	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
1st Cycle	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd Cycle	X	A16	A15	A14	A13	A12	A11	A10	A9
3rd Cycle	X	A24	A23	A22	A21	A20	A19	A18	A17
4th Cycle	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A25

Note: (1). A8 is Don't Care in x16 devices.
(2). Any additional address input cycles will be ignored.
(3). A1 is the Least Significant Address for x16 devices.
(4). The 01h Command is not used in x16 devices.

COMMAND SET

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O_0-I/O_7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.
The Commands are summarized in Table 5, Commands.

Table 5: Command Set

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	Command accepted during busy
READ A	00h	-	-	
READ B	01h	-	-	
READ C	50h	-	-	
READ ELECTRINIC SIGNATURE	90h	-	-	
READ STATUS REGISTER	70h	-	-	Yes
PAGE PROGRAM	80h	10h	-	
COPY BACK PROGRAM	00h	8Ah	10h	
CACHE PROGRAM	80h	15h	-	
BLOCK ERASE	60h	D0h	-	
RESET	FFh	-	-	Yes

Note: (1). Any undefined command sequence will be ignored by the device.

(2). Bus Write Operation(1^{st}, 2^{nd} and 3^{rd} Cycle) : The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.

DEVICE OPERATIONS

Pointer Operations

As the NAND Flash memories contain two different areas for x16 devices and three different areas for x8 devices (see Figure 8) the read command codes (00h, 01h, 50h) are used to act as pointers to the different areas of the memory array (they select the most significant column address).
The Read A and Read B commands act as pointers to the main memory area. Their use depends on the bus width of the device.

- In x16 devices the Read A command (00h) sets the pointer to Area A (the whole of the main area) that is Words 0 to 255.
- In x8 devices the Read A command (00h) sets the pointer to Area A (the first half of the main area) that is Bytes 0 to 255, and the Read B command (01h) sets the pointer to Area B (the second half of the main area) that is Bytes 256 to 511.

In both the x8 and x16 devices the Read C command (50h), acts as a pointer to Area C (the spare memory area) that is Bytes 512 to 527 or Words 256 to 263.
Once the Read A and Read C commands have been issued the pointer remains in the respective areas until another

pointer code is issued. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A.
The pointer operations can also be used before a program operation, that is the appropriate code (00h, 01h or 50h) can be issued before the program command 80h is issued (see Figure 9).

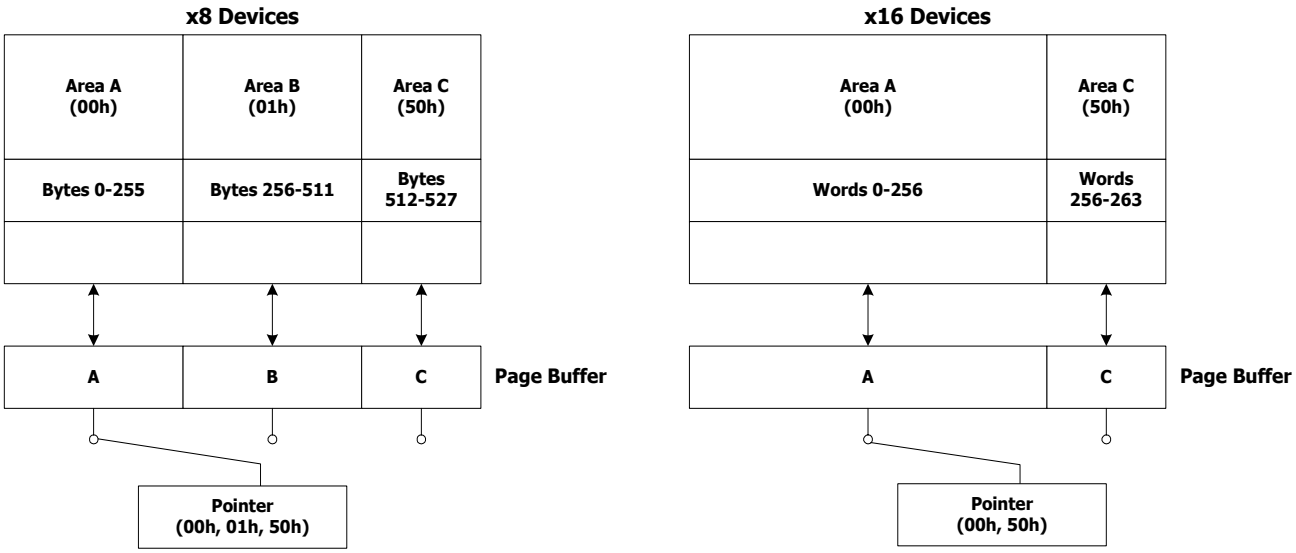


Figure 8. Pointer Operation

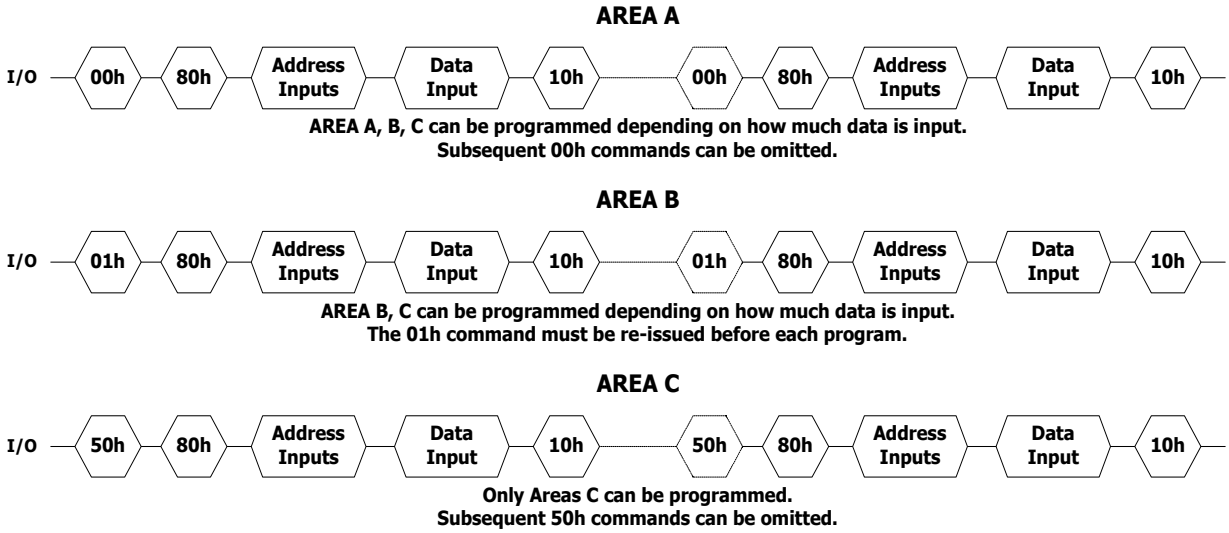


Figure 9. Pointer Operations for Programming

Read Memory Array

Each operation to read the memory area starts with a pointer operation as shown in the Pointer Operations section. The device defaults to Read A mode after powerup or a Reset operation. Devices, where page0 is read automatically at power-up, are available on request.

When reading the spare area addresses:

- A0 to A3 (x8 devices)
- A0 to A2 (x16 devices)

are used to set the start address of the spare area while addresses:

- A4 to A7 (x8 devices)
- A3 to A7 (x16 devices)

are ignored.

Once the Read A or Read C commands have been issued they do not need to be reissued for subsequent read operations as the pointer remains in the respective area. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A and so another Read B command is required to start another read operation in Area B.

Once a read command is issued three types of operations are available: Random Read, Page Read and Sequential Row Read.

Random Read

Each time the command is issued the first read is Random Read.

Page Read

After the Random Read access the page data is transferred to the Page Buffer in a time of t_{WHBH} (refer to Table 15 for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

Sequential Row Read

After the data in last column of the page is output, if the Read Enable signal is pulsed and Chip Enable remains Low then the next page is automatically loaded into the Page Buffer and the read operation continues. A Sequential Row Read operation can only be used to read within a block. If the block changes a new read command must be issued. Refer to Figures 12 and 13 for details of Sequential Row Read operations. To terminate a Sequential Row Read operation set the Chip Enable signal to High for more than t_{EHEL}. Sequential Row Read is not available when the Chip Enable Don't Care option is enabled.

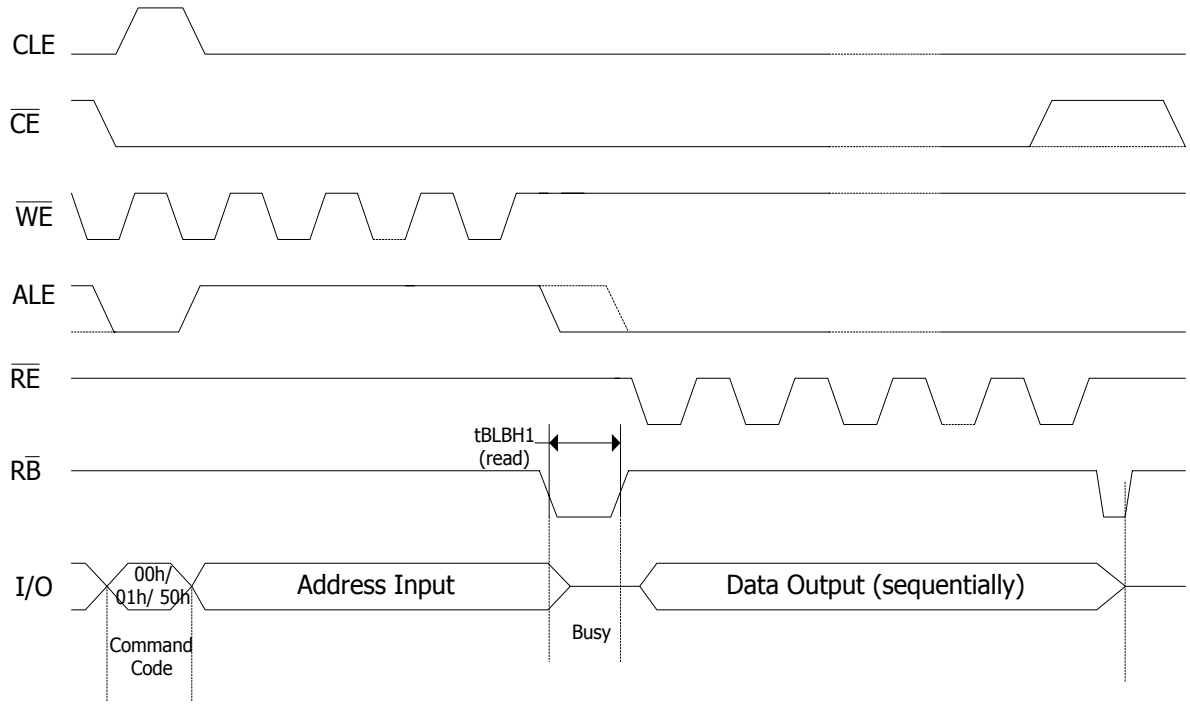


Figure 10. Read (A, B, C) Operation

Note: 1. If t_{ELWL} is less than 10ns, t_{WLWH} must be minimum 35ns, otherwise, t_{WLWH} may be minimum 25ns.

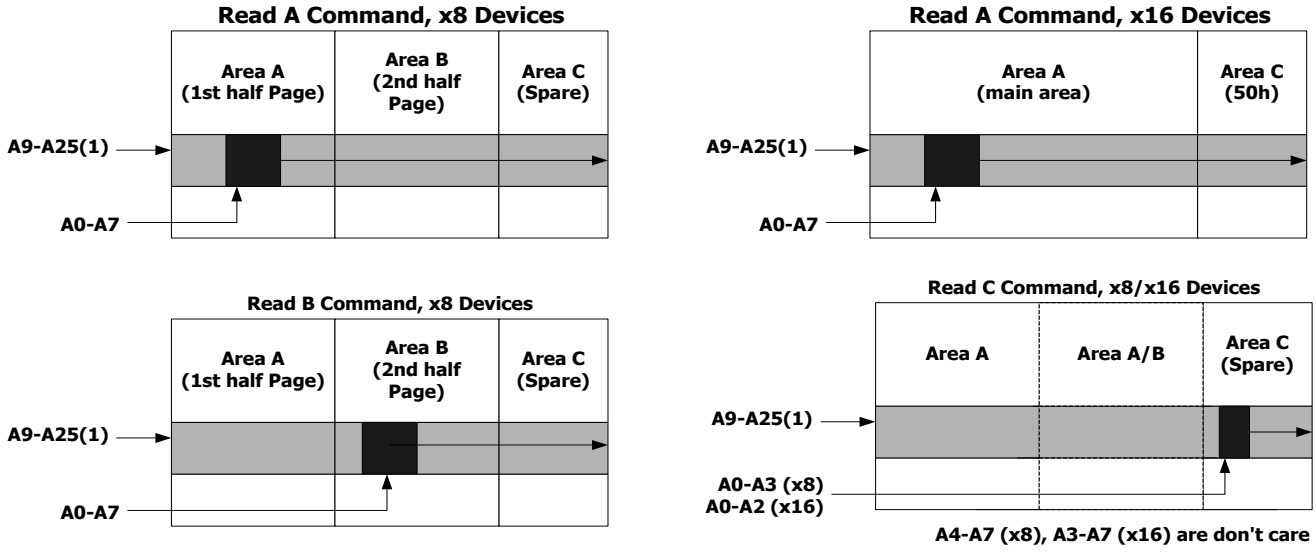


Figure 11. Read Block Diagrams

Note: 1. Highest address depends on device density.

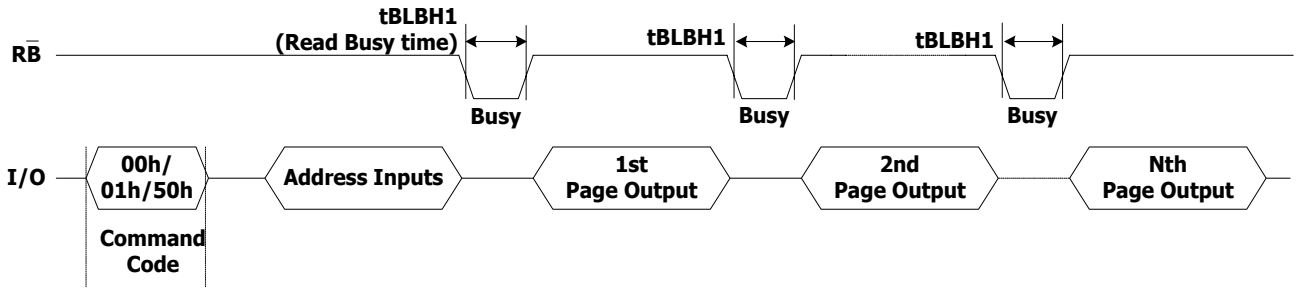


Figure 12. Sequential Row Read Operation

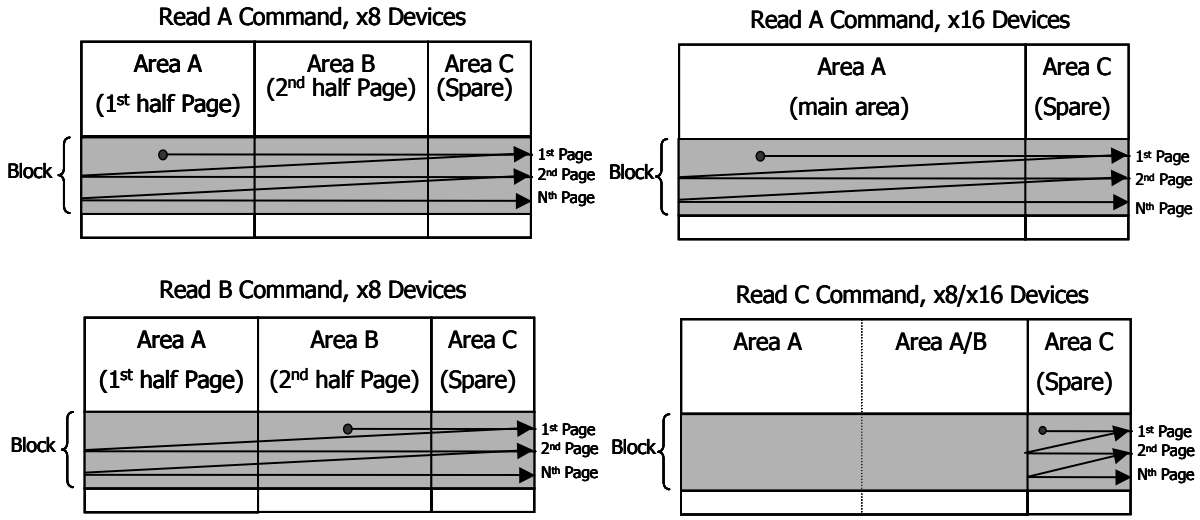


Figure 13. Sequential Row Read Block Diagrams

Page Program

The Page Program operation is the standard operation to program data to the memory array. The main area of the memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 528) or words (1 to 264) can be programmed.
The max number of consecutive partial page program operations allowed in the same page is one in the main area and two in the spare area. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.
Before starting a Page Program operation a Pointer operation can be performed to point to the area to be programmed. Refer to the Pointer Operations section and Figure 9 for details.
Each Page Program operation consists of five steps (see Figure 14):

1. one bus cycle is required to setup the Page Program command
2. four bus cycles are then required to input the program address (refer to Table 3)
3. the data is then input (up to 528 Bytes/ 264 Words) and loaded into the Page Buffer
4. one bus cycle is required to issue the confirm command to start the Program/ Erase/Read Controller.
5. The Program/ Erase/Read Controller then programs the data into the array.

Once the program operation has started the Status Register can be read using the Read Status Register command. During program operations the Status Register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.
During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.
Once the program operation has completed the Program/ Erase/Read Controller bit SR6 is set to '1' and the Ready/ Busy signal goes High.
The device remains in Read Status Register mode until another valid command is written to the Command Interface.

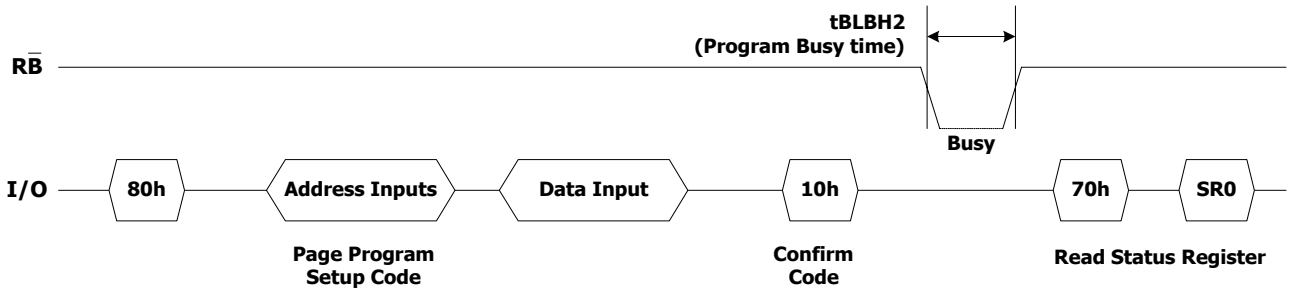


Figure 14. Page Program Operation

Note: Before starting a Page Program operation a Pointer operation can be performed. Refer to Pointer section for details.

Copy Back Program

The Copy Back Program operation is used to copy the data stored in one page and reprogram it in another page. The Copy Back Program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the Copy Back Program operation fails an error is signalled in the Status Register. However as the standard external ECC cannot be used with the Copy Back operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of Copy Back operations on the same data and/or to improve the performance of the ECC.

The Copy Back Program operation requires three steps:

- 1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 264 Words/ 528 Bytes from the page into the Page Buffer.
- 2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4 bus cycles to input the target page address. *A25* must be the same for the Source and Target Pages.
- 3. Then the confirm command is issued to start the P/E/R Controller.

After a Copy Back Program operation, a partial page program is not allowed in the target page until the block has been erased.

See Figure 15 for an example of the Copy Back operation.

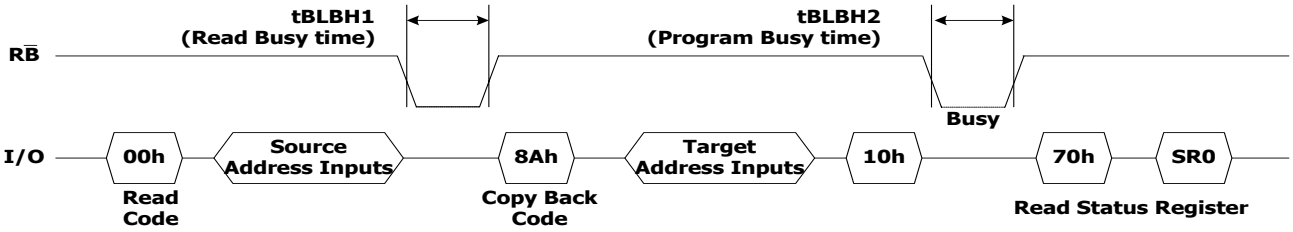


Figure 15. Copy Back Operation

Cache Program

The Cache Program operation is used to improve the programming throughput by programming data using the Cache Register. The Cache Program operation can only be used within one block. The Cache Register allows new data to be input while the previous data that was transferred to the Page Buffer is programmed into the memory array.

Before starting a Cache Program operation a Pointer operation is necessary to point to the area to be programmed. Only the 00h or 50h Pointer operations are valid for the Cache Program operation. Refer to the Pointer Operations section and Figure 9 for details. Each Cache Program operation consists of five steps (refer to Figure 16):

1. First of all the program setup command is issued (one bus cycle to issue the program setup command then four bus write cycles to input the address), the data is then input (up to 528 Bytes/ 264 Words) and loaded into the Cache Register.

2. One bus cycle is required to issue the confirm command to start the P/E/R Controller.
3. The P/E/R Controller then transfers the data to the Page Buffer. During this the device is busy for a time of t_{BLBH5}.
4. Once the data is loaded into the Page Buffer the P/E/R Controller programs the data into the memory array. As soon as the Cache Registers are empty (after t_{BLBH5}) a new Cache program command can be issued, while the internal programming is still executing. Once the program operation has started the Status Register can be read using the Read Status Register command. During Cache Program operations SR5 can be read to find out whether the internal programming is ongoing (SR5 = '0') or has completed (SR5 = '1') while SR6 indicates whether the Cache Register is ready to accept new data. If any errors have been detected on the previous page (Page N-1), the Cache Program Error Bit SR1 will be set to '1', while if the error has been detected on Page N the Error Bit SR0 will be set to '1'. When the next page (Page N) of data is input with the Cache Program command, t_{BLBH5} is affected by the pending internal programming. The data will only be transferred from the Cache Register to the Page Buffer when the pending program cycle is finished and the Page Buffer is available. If the system monitors the progress of the operation using only the Ready/Busy signal, the last page of data must be programmed with the Page Program confirm command (10h).
If the Cache Program confirm command (15h) is used instead, Status Register bit SR5 must be polled to find out if the last programming is finished before starting any other operations.

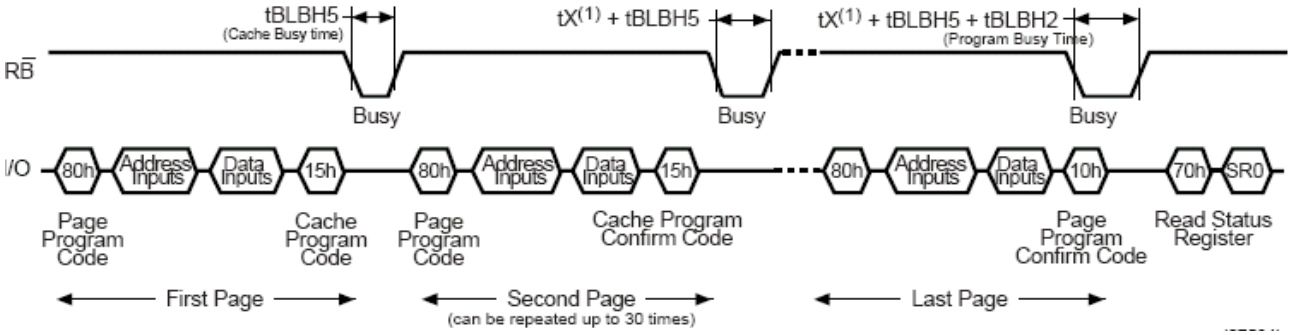


Figure 16. Cashe Program Operation

Note: (1). t_X is a fraction of the Program Busy Time and is less than t_{BLBH2}.
(2). Up to 32 pages can be programmed in one Cache Program operation.

Block Erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost. An erase operation consists of three steps (refer to Figure 17):

1. One bus cycle is required to setup the Block Erase command.
2. Only three bus cycles for 512Mb devices are required to input the block address. The first cycle (A0 to A7) is not required as only addresses A14 to A25 (highest address depends on device density) are valid, A9 to A13 are ignored. In the last address cycle I/O_0 to I/O_7 must be set to V_{IL}.
3. One bus cycle is required to issue the confirm command to start the P/E/R Controller.

Once the erase operation has completed the Status Register can be checked for errors.

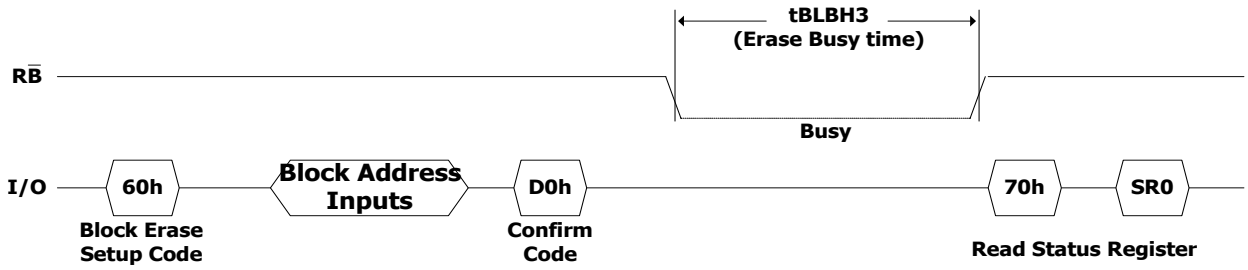


Figure 17. Block Erase Operation

Reset

The Reset command is used to reset the Command Interface and Status Register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.
If the device has already been reset then the new Reset command will not be accepted. The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to Table 15 for the values.

Read Status Register

The device contains a Status Register which provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation.
The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O_0- I/O_7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register.
After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore if a Read Status Register command is issued during a Random Read cycle a new read command must be issued to continue with a Page Read or Sequential Row Read operation.
The Status Register bits are summarized in Table 6, Status Register Bits. Refer to Table 6 in conjunction with the following text descriptions.

Write Protection Bit (SR7)

The Write Protection bit can be used to identify if the device is protected or not. If the Write Protection bit is set to '1' the device is not protected and program or erase operations are allowed. If the Write Protection bit is set to '0' the device is protected and program or erase operations are not allowed.

P/E/R Controller and Cache Ready/Busy Bit (SR6)

Status Register bit SR6 has two different functions depending on the current operation.

During Cache Program operations SR6 acts as a Cache Program Ready/Busy bit, which indicates whether the Cache Register is ready to accept new data. When SR6 is set to '0', the Cache Register is busy and when SR6 is set to '1', the Cache Register is ready to accept new data.

During all other operations SR6 acts as a P/E/R Controller bit, which indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to '0', the P/E/R Controller is active (device is busy); when the bit is set to '1', the P/E/R Controller is inactive (device is ready).

P/E/R Controller Bit (SR5)

The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to '0', the P/E/R Controller is active (device is busy); when the bit is set to '1', the P/E/R Controller is inactive (device is ready).

Cache Program Error Bit (SR1)

The Cache Program Error bit can be used to identify if the previous page (page N-1) has been successfully programed or not in a Cache Program operation. SR1 is set to '1' when the Cache Program operation has failed to program the previous page (page N-1) correctly. If SR1 is set to '0' the operation has completed successfully.

The Cache Program Error bit is only valid during Cache Program operations, during other operations it is Don't Care.

Error Bit (SR0)

The Error bit is used to identify if any errors have been detected by the P/E/R Controller. The Error Bit is set to '1' when a program or erase operation has failed to write the correct data to the memory. If the Error Bit is set to '0' the operation has completed successfully. The Error Bit SR0, in a Cache Program operation, indicates a failure on Page N.

SR4, SR3 and SR2 are Reserved

Table 6: Status Register Bit

Bit	NAME	Logic Level	Definition
SR7	Write Protection	'1'	Not Protected
		'0'	Protected
SR6(1)	Program/Erase/Read Controller	'1'	P/E/R C Inactive, device ready
		'0'	P/E/R C active, device busy
	Cache Read/Busy	'1'	Cache Register ready (Cache Program only)
		'0'	Cache Register busy (Cache Program only)
SR5	Program/ Erase/ Read Controller(2)	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR4, SR3, SR2	Reserved	Don't Care	
SR1	Cache Program Error(3)	'1'	Page N-1 failed in Cache Program operation
		'0'	Page N-1 programmed successfully
SR0(1)	Generic Error	'1'	Error - Operation failed
		'0'	No Error - Operation successful
	Cache Program Error	'1'	Page N failed in Cache Program operation
		'0'	Page N programmed successfully

Note: (1). The SR6 bit and SR0 bit have a different meaning during Cache Program operations.
(2). Only valid for Cache Program operations, for other operations it is same as SR6.
(3). Only valid for Cache Program operations, for other operations it is Don't Care.

Read Electronic Signature

The device contains a Manufacturer Code and Device Code. To read these codes two steps are required:

1. first use one Bus Write cycle to issue the Read Electronic Signature command (90h)
2. then subsequent Bus Read operations will read the Manufacturer Code and the Device Code until another command is issued.

Refer to Table, Read Electronic Signature for information on the addresses.

Part Number	Manufacture Code	Device Code	Bus Width
HY27US08121M	ADh	76h	x8
HY27SS08121M	ADh	36h	x8
HY27US16121M	00ADh	0056h	x16
HY27SS16121M	00ADh	0046h	x16

Automatic Page 0 Read at Power-Up

Automatic Page 0 Read at Power-Up is an option available on all devices belonging to the NAND Flash 528 Byte/264 Word Page family. It allows the microcontroller to directly download boot code from page 0, without requiring any command or address input sequence. The Automatic Page 0 Read option is particularly suited for applications that boot from the NAND.

Devices delivered with Automatic Page 0 Read at Power-Up can have the Sequential Row Read option either enabled or disabled.

Automatic Page 0 Read Description.

At powerup, once the supply voltage has reached the threshold level, V_{CCth}, all digital outputs revert to their reset state and the internal NAND device functions (reading, writing, erasing) are enabled.

The device then automatically switches to read mode where, as in any read operation, the device is busy for a time t_{BLBH1} during the data is transferred to the Page Buffer. Once the data transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially on the I/O bus by pulsing the Read Enable, RE#, signal. Figures 18 and 19 show the power-up waveforms for devices featuring the Automatic Page 0 Read option.

Sequential Row Read Disabled

If the device is delivered with Sequential Row Read disabled and Automatic Read Page 0 at Power-up, only the first page (Page 0) will be automatically read after the power-on sequence. Refer to Figure 18.

Sequential Row Read Enabled

If the device is delivered with the Automatic Page 0 Read option only (Sequential Row Read Enable), the device will automatically enter Sequential Row Read mode after the power-up sequence, and start reading Page 0, Page 1, etc., until the last memory location is reached, each new page being accessed after a time t_{BLBH1}.

The Sequential Row Read operation can be inhibited or interrupted by de-asserting E (set to V_{IH}) or by issuing a command. Refer to Figure 19.

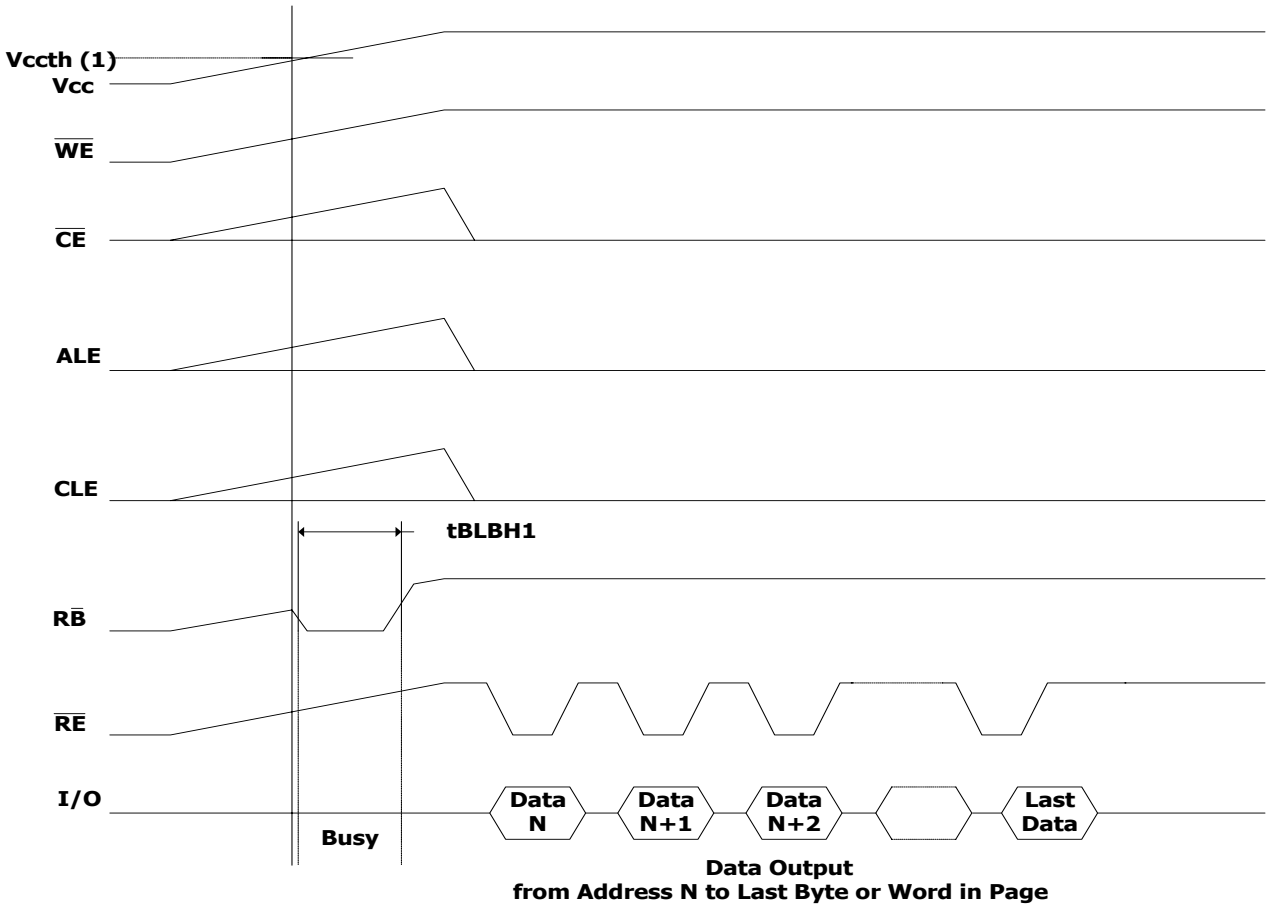


Figure 18. Chip Enable Don't Care and Automatic Page 0 Read at power-up

Note: (1). V_{CCth} is equal to 2.5V for 3.3V Power Supply devices and to 1.5V for 1.8V Power Supply devices.

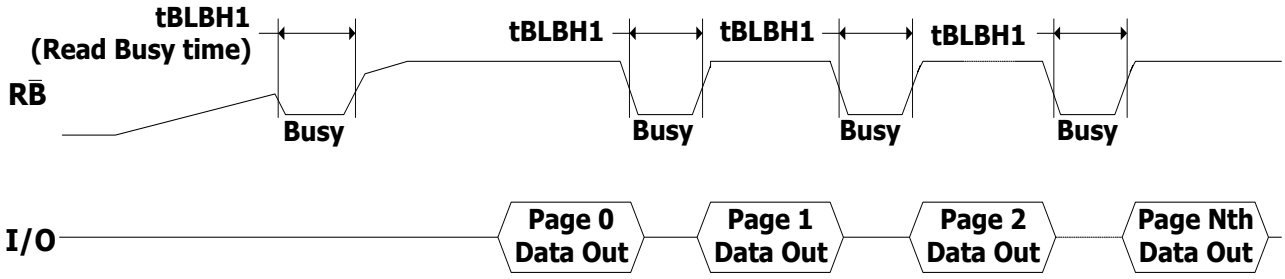


Figure 19. Automatic Page 0 Read at power-up (Chip Enable Don't Disable)

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 6th Byte/ 1st Word in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block.

The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 20.

Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block.

These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

The Copy Back Program command can be used to copy the data to a valid block.

See the "Copy Back Program" section for more details.

Refer to Table 7 for the recommended procedure to follow if an error occurs during an operation.

Table 7: Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC
Read	ECC

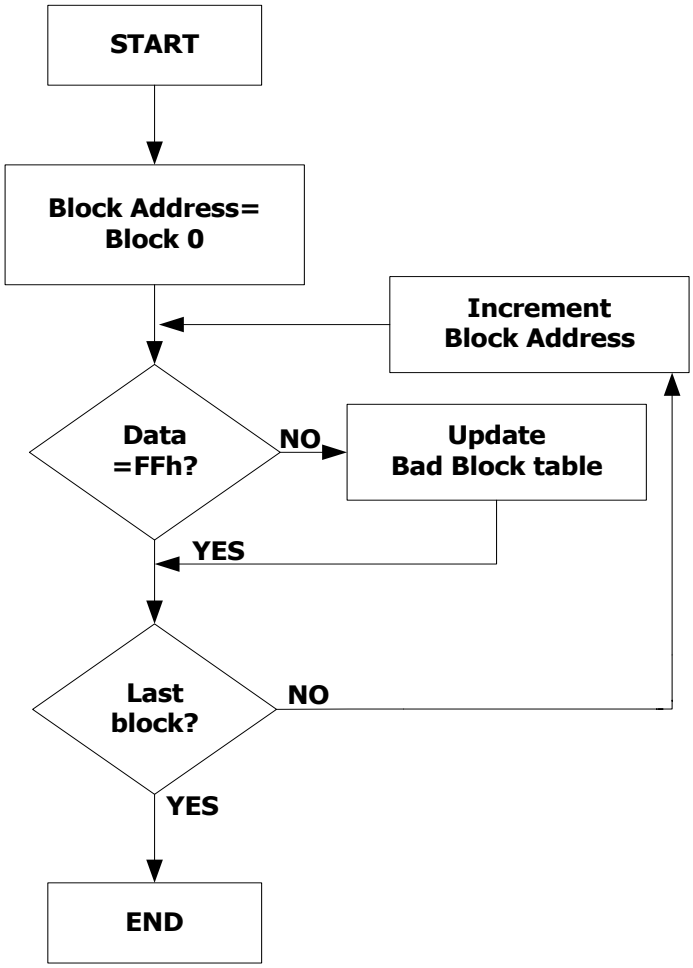


Figure 20. Bad Block Management Flowchart

Table 8: Valid Block

Symbol	Para.	Min	Max	Unit
N_{VB}	# of Valid Block	4016	4096	Blocks

PROGRAM AND ERASE TIMES AND ENDURANCE CYCLES

The Program and Erase times and the number of Program/ Erase cycles per block are shown in Table 9.

Table 9: Program, Erase Time and Program Erase Endurance Cycles

Parameters	NAND Flash			Unit
	Min	Typ	Max	
Page Program Time		200	500	us
Block Erase Time		2	3	ms
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	10			years

MAXIMUM RATING

Stressing the device above the ratings listed in Table 10, Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 10: Absolution Maximum Rating

Symbol	Parameter		NAND Flash		Unit
			Min	Max	
T_{BIAS}	Temperature Under Bias		-50	125	°C
T_{STG}	Storage Temperature		-65	150	°C
V_{IO}(1)	Input or Output Voltage	1.8V devices	-0.6	2.7	V
		3.3 V devices	-0.6	4.6	V
V_{CC}	Supply Voltage	1.8V devices	-0.6	2.7	V
		3.3 V devices	-0.6	4.6	V

Note: (1). Minimum Voltage may undershoot to -2V for less than 20ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{CC} + 2V for less than 20ns during transitions on I/O pins.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 11, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 11: Operating and AC Measurement Conditions

Parameter		NAND Flash		Unit
		Min	Max	
Supply Voltage (V_{CC})	1.8V devices	1.7	1.95	V
	2.6V devices(1)	2.4	2.8	V
	3.3V devices	2.7	3.6	V
Ambient Temperature (T_A)	Commercial Temp.	0	70	°C
	Indurstrial Temp.	-40	85	°C
Load Capacitance (C_L) (1 TTL GATE and C_L)	1.8V devices	30		pF
	2.6V devices(1)	30		pF
	3.3V devices	100		pF
Input Pulses Voltages	1.8V devices	0	V_{CC}	V
	2.6V devices(1)	0	V_{CC}	V
	3.3V devices	0.4	2.4	V
Input and Output Timing Ref. Voltages	1.8V devices	$V_{CC}/2$		V
	2.6V devices(1)			V
	3.3V devices	1.5		V
Input Rise and Fall Times		5		ns

Note : (1). TBD

Table 12: Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V		10	pF

Note: T_A = 25°C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.

Table 13: DC Characteristics, 3.3V Device and 1.8V Device

Sym-bol	Parameter		Test Condition	3.3V Device			1.8V Device			Unit
				Min	Typ	Max	Min	Typ	Max	
I_{CC1}	Operating Current	Sequentia Read	t_{RLRL} minimum $\overline{CE}=V_{IL}$, I_{OUT} = 0 mA	-	10	20	-	8	15	mA
I_{CC2}		Program	-	-	10	20	-	8	15	mA
I_{CC3}		Erase	-	-	10	20	-	8	15	mA
I_{CC4}	Stand-by Current (TTL)		$\overline{CE}=V_{IH}$, $\overline{WP}$=0V/V_{CC}	-	-	1	-	-	1	mA
I_{CC5}	Stand-By Current (CMOS)		$\overline{CE}=V_{CC}$-0.2, $\overline{WP}$=0/V_{CC}	-	10	50	-	10	50	uA
I_{LI}	Input Leakage Current		V_{IN}= 0 to V_{CC}max	-	-	± 10	-	-	± 10	uA
I_{LO}	Output Leakage Current		V_{OUT}= 0 to V_{CC}max	-	-	± 10	-	-	± 10	uA
V_{IH}	Input High Voltage		-	2.0	-	V_{CC}+0.3	V_{CC}-0.4		V_{CC}+0.3	V
V_{IL}	Input Low Voltage		-	-0.3	-	0.8	-0.3		0.4	V
V_{OH}	Output High Voltage Level		3.3V I_{OH} = -400uA	2.4	-	-	V_{CC}-0.1	-	-	V
			1.8V I_{OH} = -100uA							
V_{OL}	Output Low Voltage Level		3.3V I_{OL} = 2.1mA	-	-	0.4	-	-	0.1	V
			1.8V I_{OL} = 100uA							
$I_{OL}(R\overline{B})$	Output Low Current ($R\overline{B}$)		3.3V V_{OL} = 0.4V	8	10	-	3	4	-	mA
			1.8V V_{OL} = 0.1V							
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)		-	-	-	2.5	-	-	1.5	V

Table 14: AC Characteristics for Command, Address, Data Input (3.3V and 1.8V Device)

Symbol	Alt. Symbol	Parameter			3.3V Device	1.8V Device	Unit
t_{ALLWL}	t_{ALS}	Address Latch Low to Write Enable Low	ALE Setup time	Min	0		ns
t_{ALHWL}		Address Latch Hith to Write Enable Low					
t_{CLHWL}	t_{CLS}	Command Latch High to Write Enable Low	CL Setup time	Min	0		ns
t_{CLLWL}		Command Latch Low to Write Enable Low					
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data Setup time	Min	20		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	$\overline{CE}$ Setup time	Min	0		ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	ALE Hold time	Min	10		ns
t_{WHALL}		Write Enable High to Address Latch Low					
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CLE hold time	Min	10		ns
t_{WHCLL}		Write Enable High to Command Latch Low					
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data Hold time	Min	10		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{CE}$ Hold time	Min	10		ns
t_{WHWH}	t_{WH}	Write Enable High to Write Enable Low	$\overline{WE}$ High Hold time	Min	15	20	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{WE}$ Pulse Width	Min	25(1)	60	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	50	80	ns

Note: 1. If t_{ELWL} is less than 10ns, t_{WLWH} must be minimum 35ns, otherwise, t_{WLWH} may be minimum 25ns.

Table 15: AC Characteristics for Operation (3.3V Device and 1.8V Device)

Alt. Sym-bol	Sym-bol	Parameter			3.3V Device	1.8V Device	Unit
t_{ALLRL1}	t_{AR1}	Address Latch Low to Read Enable Low	Read Electronic Signature	Min	10	25	ns
t_{ALLRL2}	t_{AR2}		Read cycle	Min	50	80	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20		ns
t_{BLBH1}	t_R	Ready/Busy Low to Ready/Busy High	Read Busy time, 512Mb, 1Gb[4]	Max	12	15	us
t_{BLBH2}	t_{PROG}		Program Busy time	Max	500		us
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	3		ms
t_{BLBH4}	t_{RST}		Reset Busy time, during ready	Max	5		us
			Reset Busy time, during read	Max	5		us
			Reset Busy time, during program	Max	10		us
			Reset Busy time, during erase	Max	500		us
t_{BLBH5}	t_{CBSY}		Cache Busy time	Typ	3		us
				Max	500		us
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10		ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0		ns
t_{EHBH}	t_{CRY}	Chip Enable High to Ready/Busy High (CE intercepted read)		Max	60+tr[1]		ns
t_{EHEL}	t_{CEH}	Chip Enable High to Chip Enable Low[2]		Min	100		ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	20		ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	75	ns
t_{RHBL}	t_{RB}	Read Enable High to Ready/Busy Low		Max	100		ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	15	20	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z		Min	15		ns
				Max	30		
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	Min	30	60	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	Min	50	80	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable Access time	Max	35	60	ns
	t_{READID}		Read ES Access time				

Alt. Sym-bol	Sym-bol	Parameter			3.3V Device	1.8V Device	Unit
t_{WHBH}	t_R	Write Enable High to Ready/Busy High		Max	12	15	us
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100		ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	60		ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	50	80	ns

Note: (1). The time to Ready depends on the value of the pull-up resistor tied to the Ready/Busy pin. See Figures 32, 33 and 34.

(2). To break the sequential read cycle, $\overline{CE}$ must be held High for longer than t_{EHEL}.

(3). ES = Electronic Signature.

(4). 1G DDP

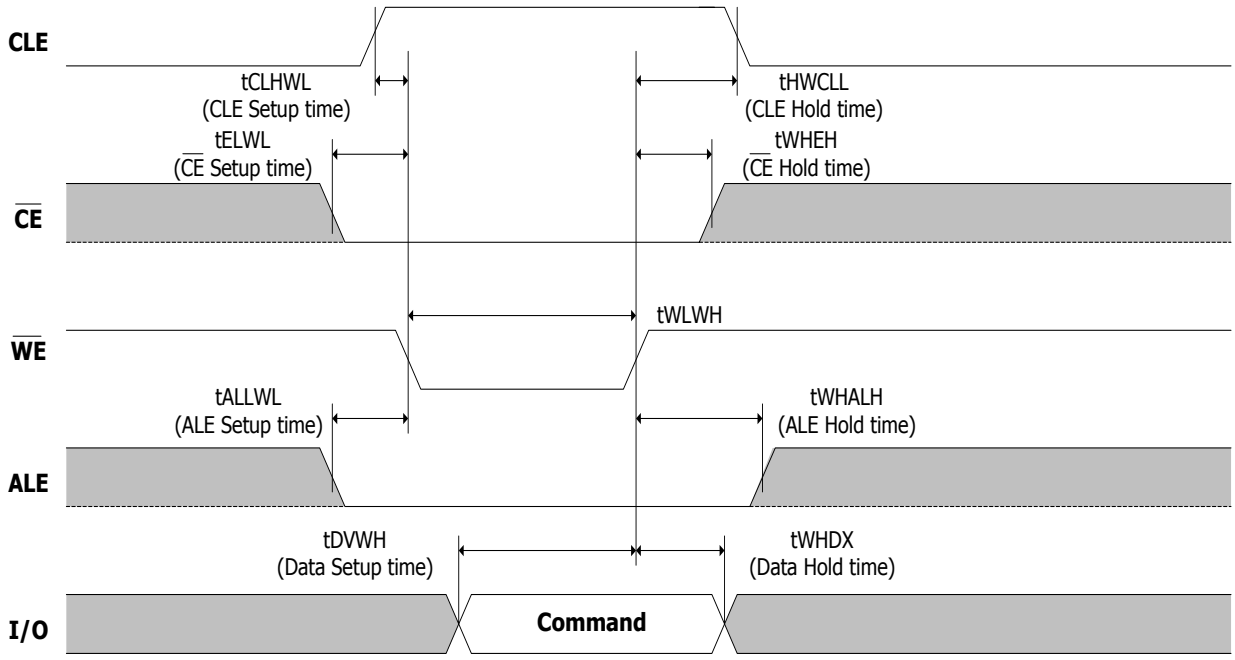


Figure 21. Command Latch AC Waveforms

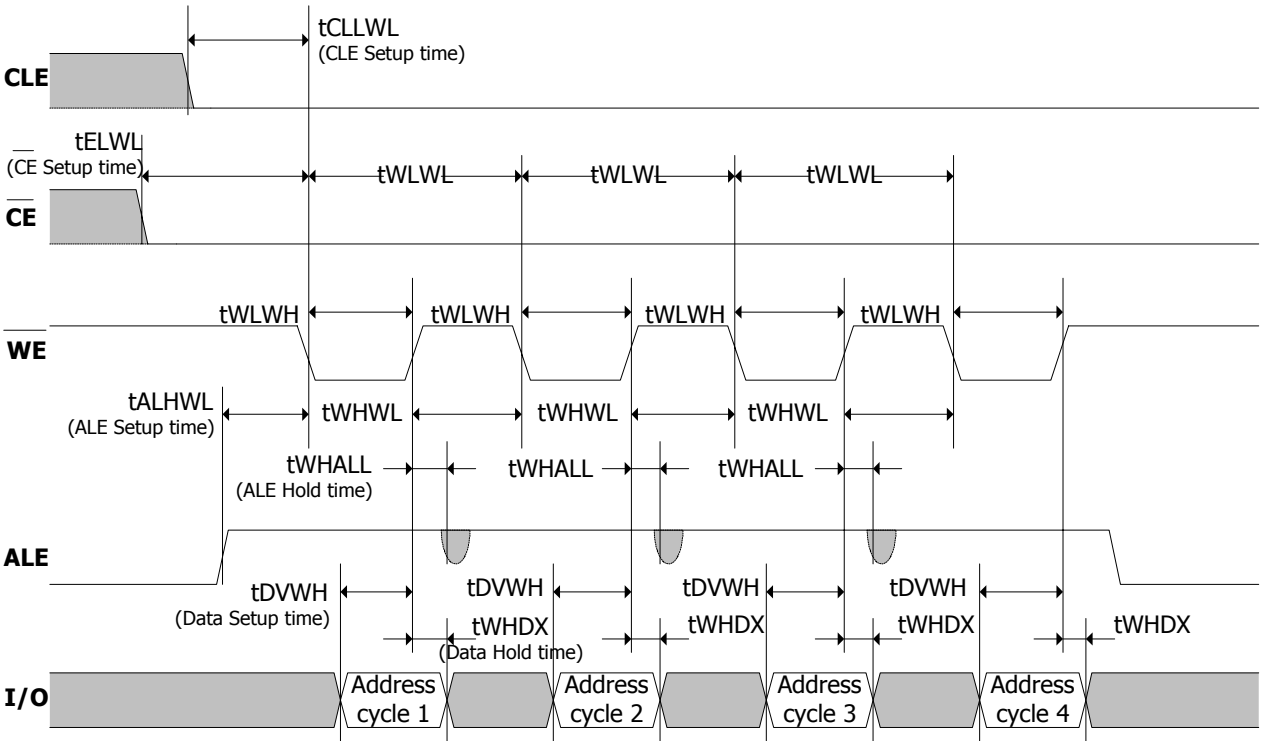


Figure 22. Address Latch AC Waveforms

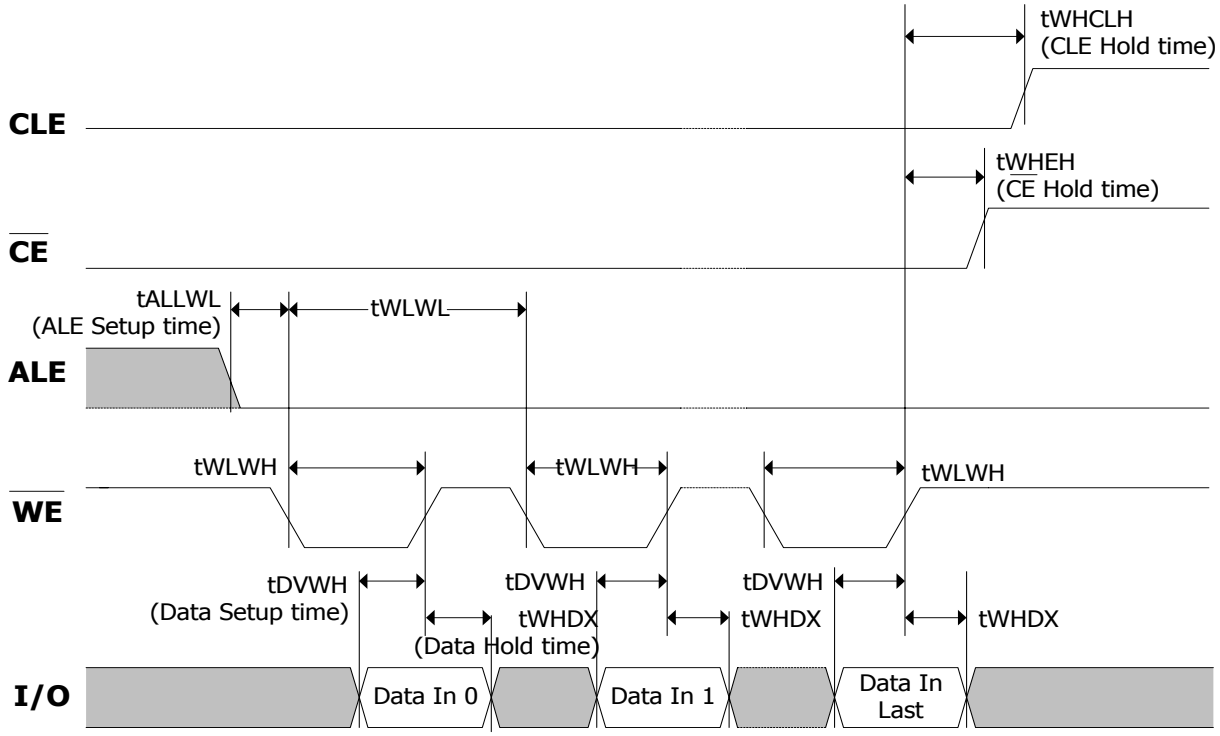


Figure 23. Data Input Latch AC Waveforms

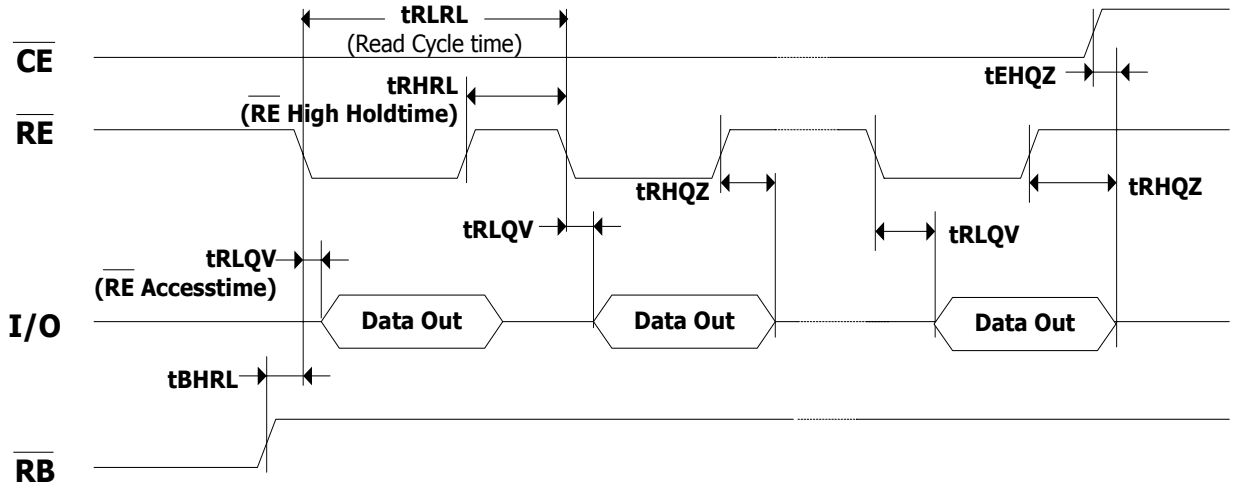


Figure 24. Sequential Data Output after Read AC Waveforms

Note:1. CLE = Low, ALE = Low, $\overline{WE}$ = High.

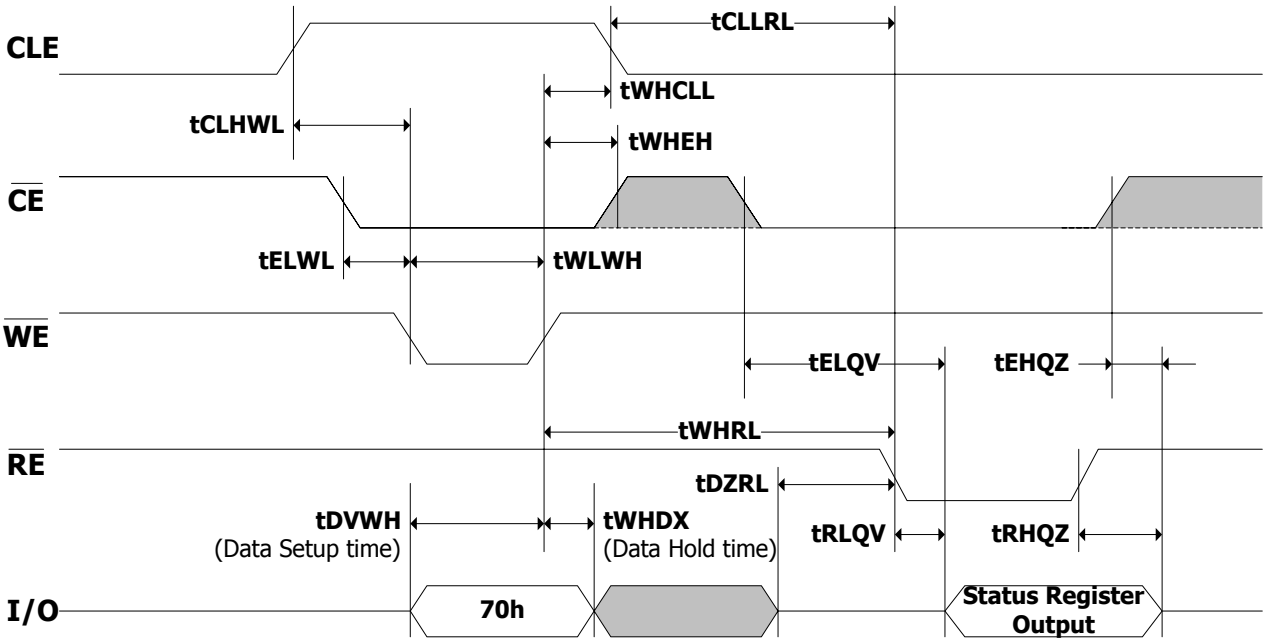


Figure 25. Read Status Register AC Waveform

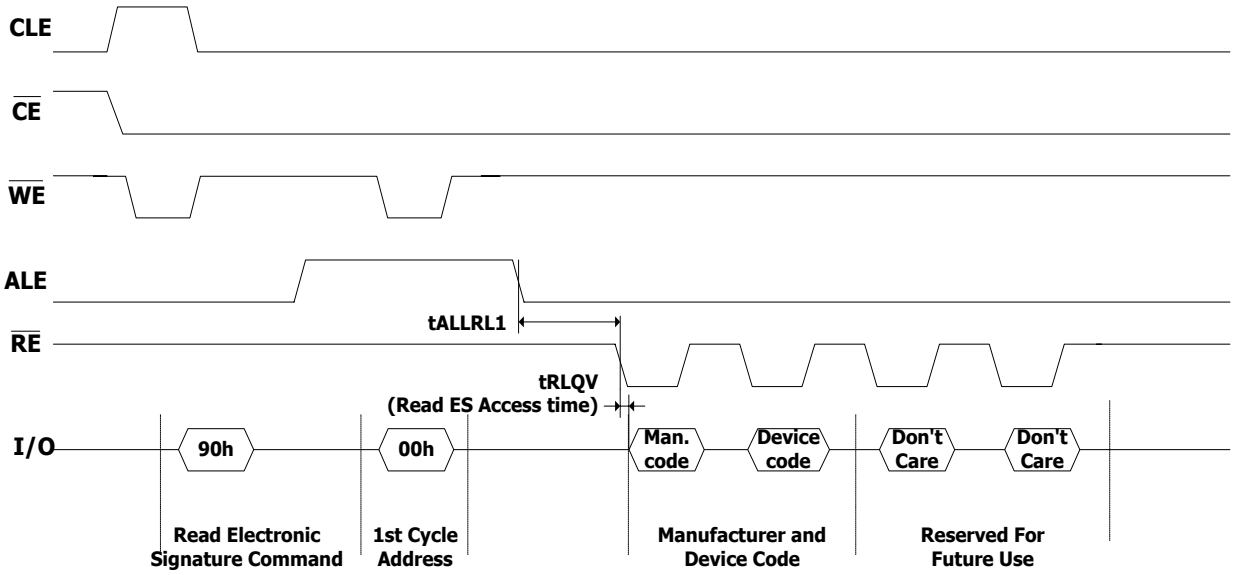


Figure 26. Read Electronic Signature AC Waveform

Note: Refer to table(To see Page 22) for the values of the manufacture and device codes.

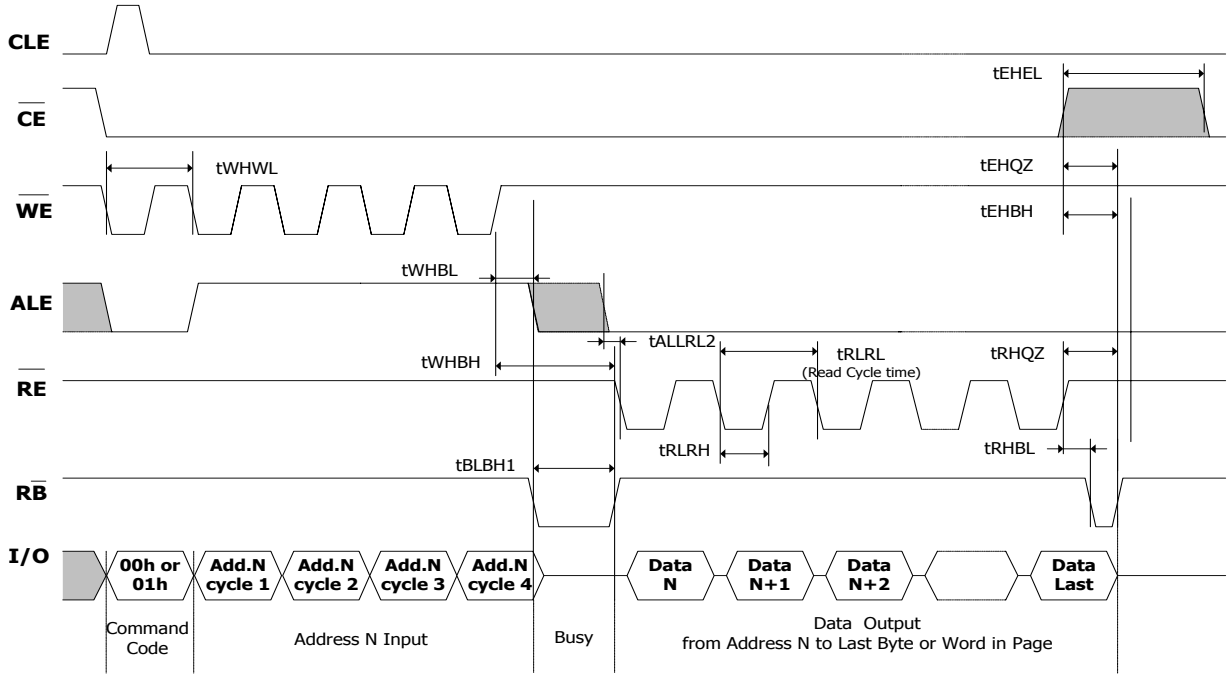


Figure 27. Read Read A/ Read B Operation AC Waveform

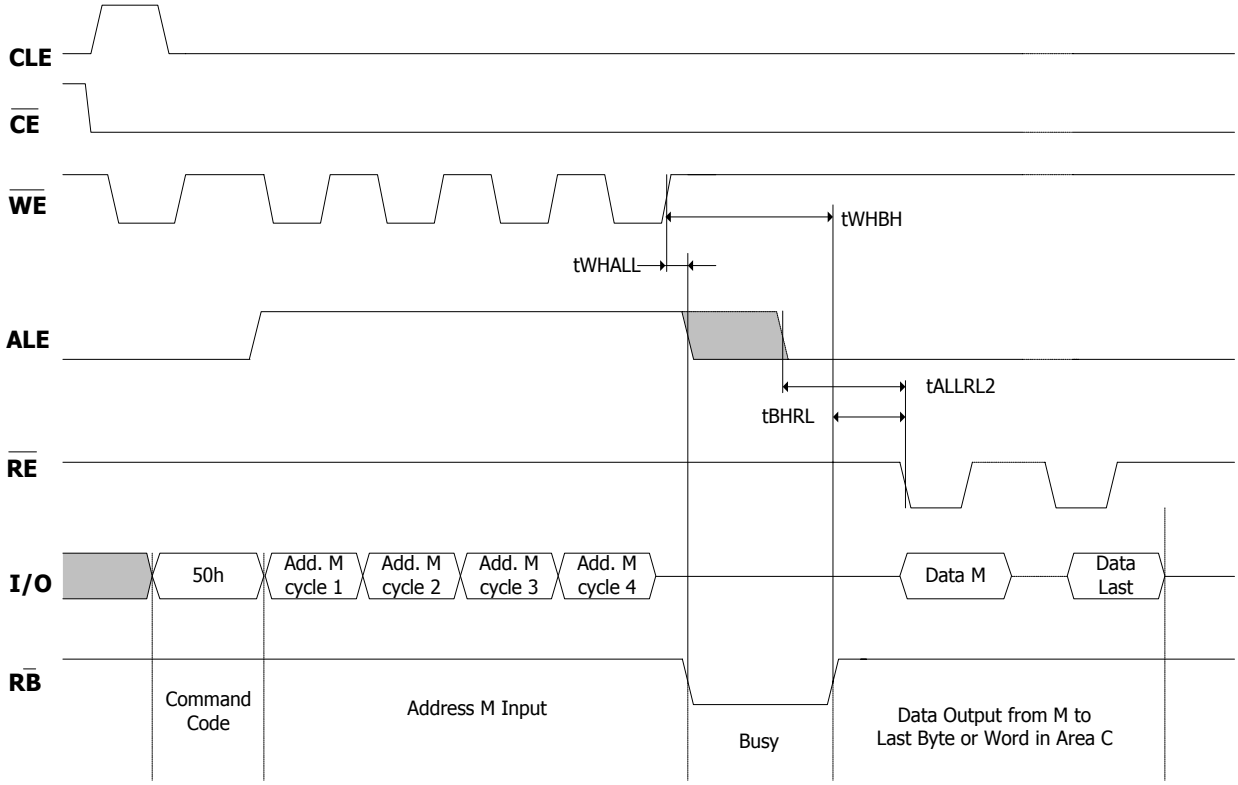


Figure 28. Read C Operation, One Page AC Waveform

Note: 1. A0-A7 is the address in the Spare Memory area, where A0-A3 are valid and A4-A7 are don't care.
2. Only address cycle 4 is required.

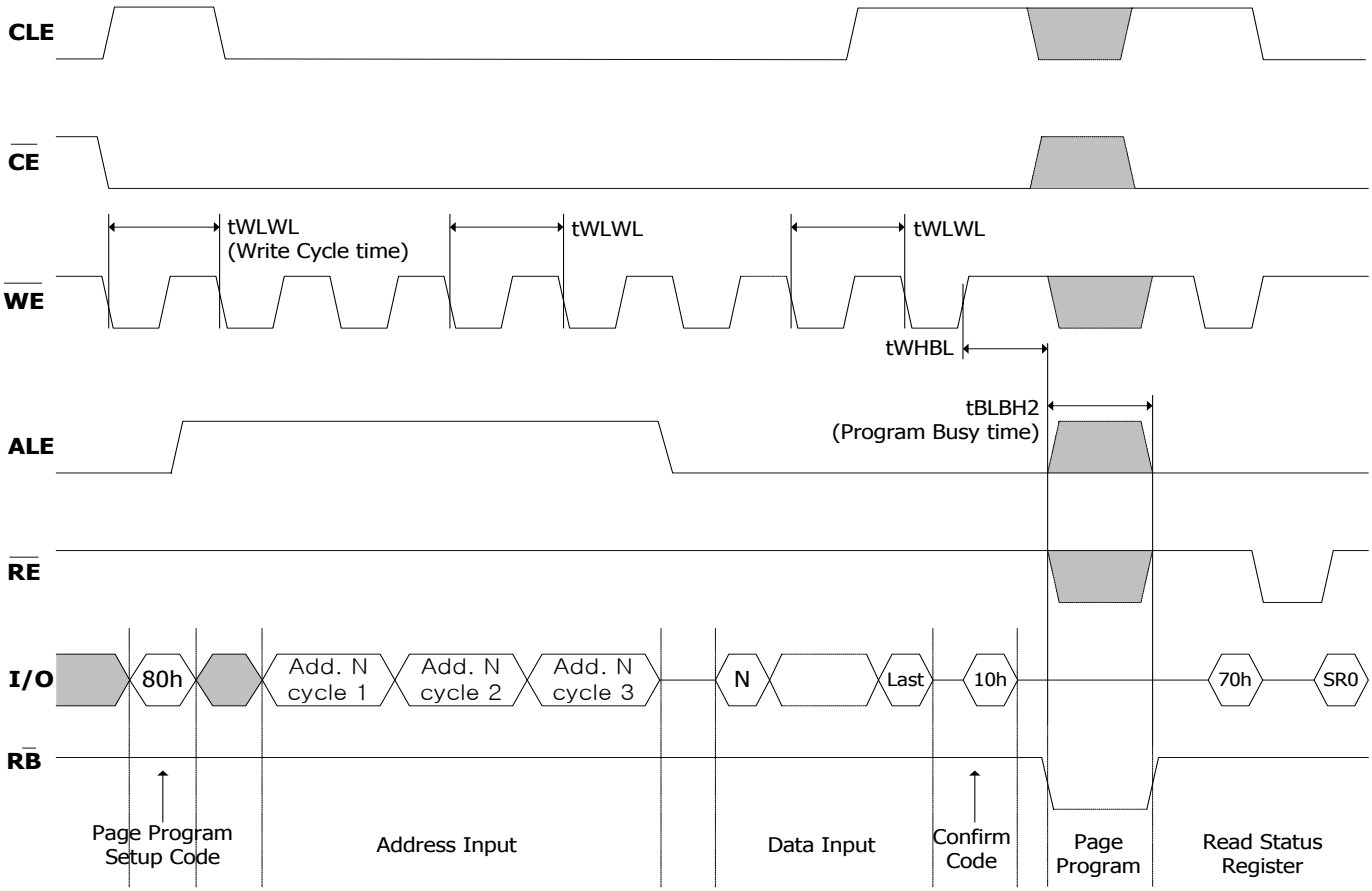


Figure 29. Page Program AC Waveform

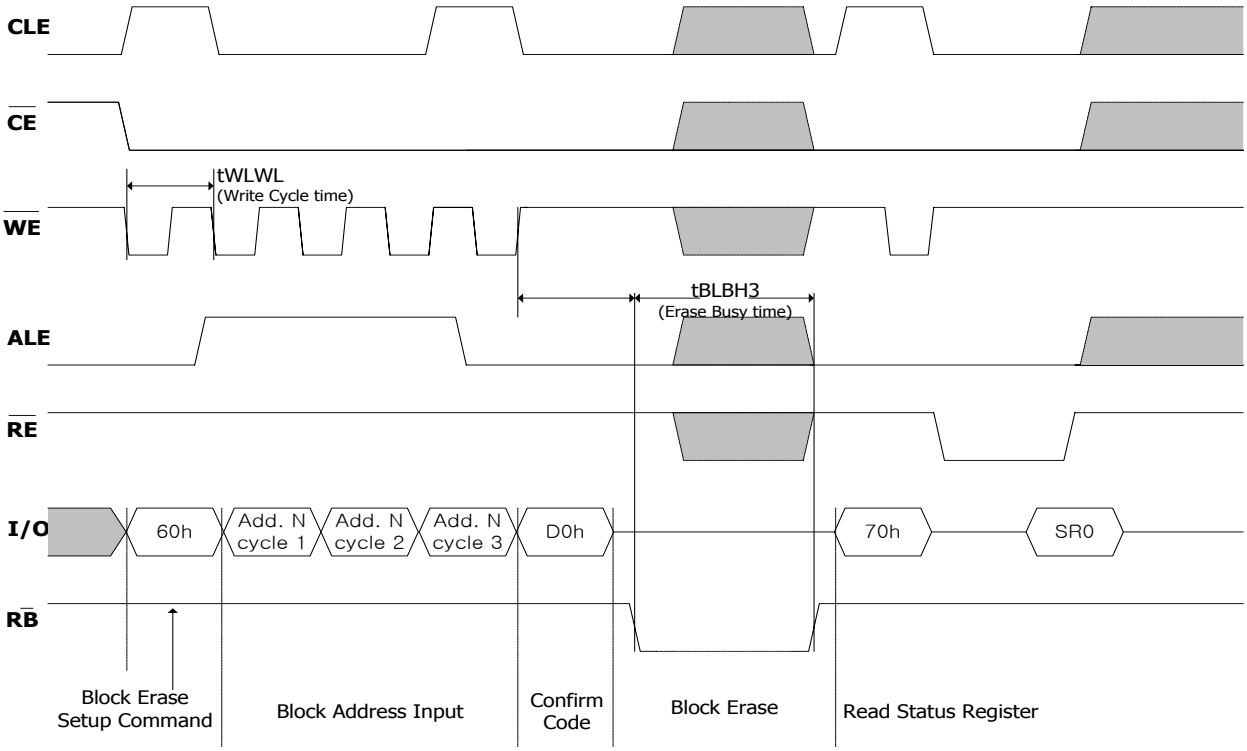


Figure 30. Block Erase AC Waveform

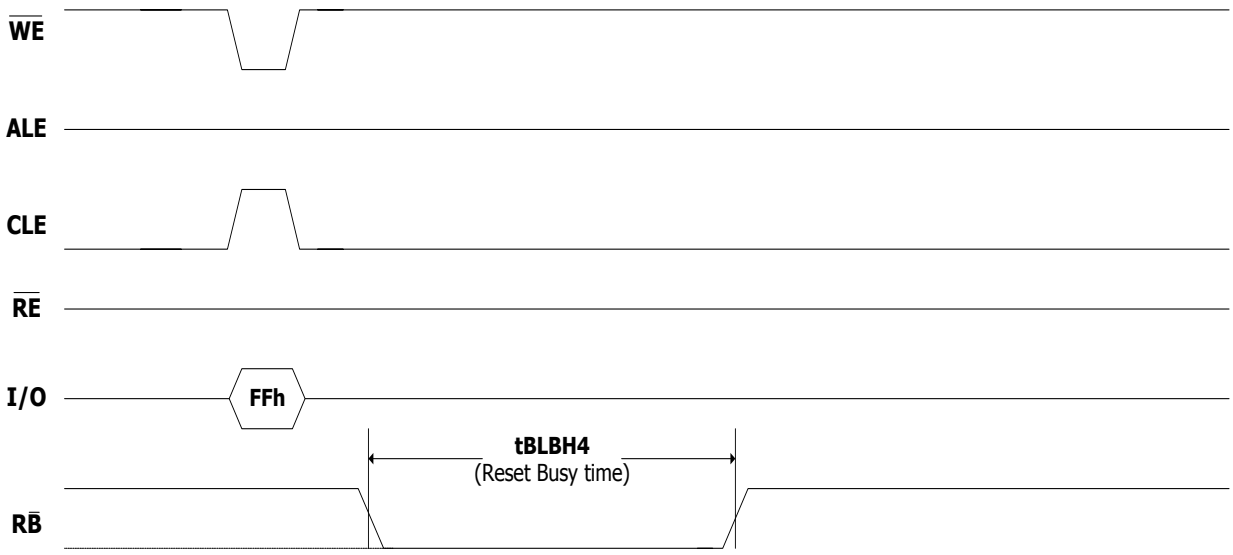


Figure 31. Reset AC Waveform

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care read operation was disabling of the automatic sequential read function.

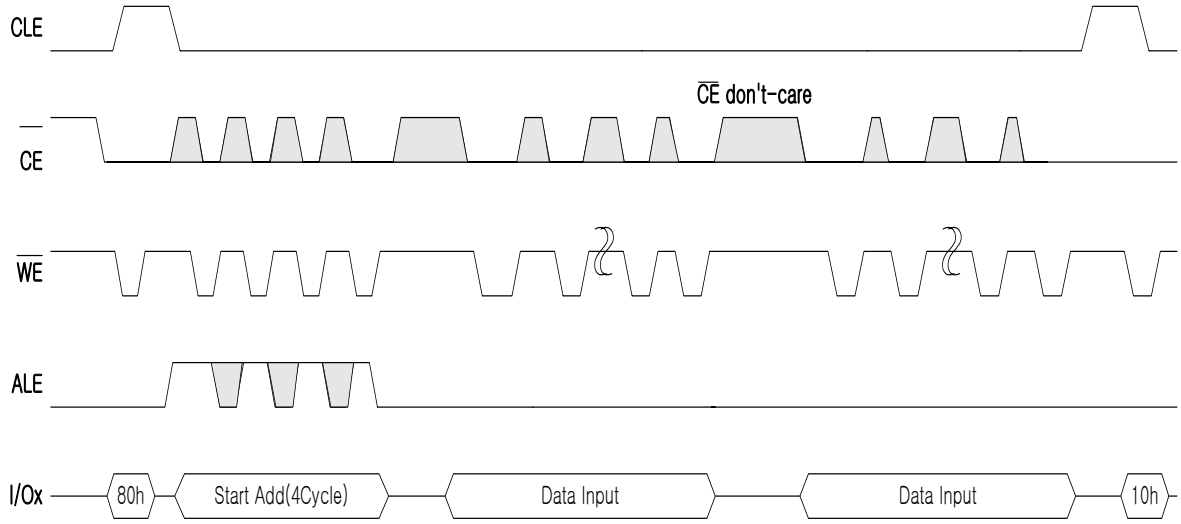


Figure 32. Program Operation with $\overline{CE}$ don't-care.

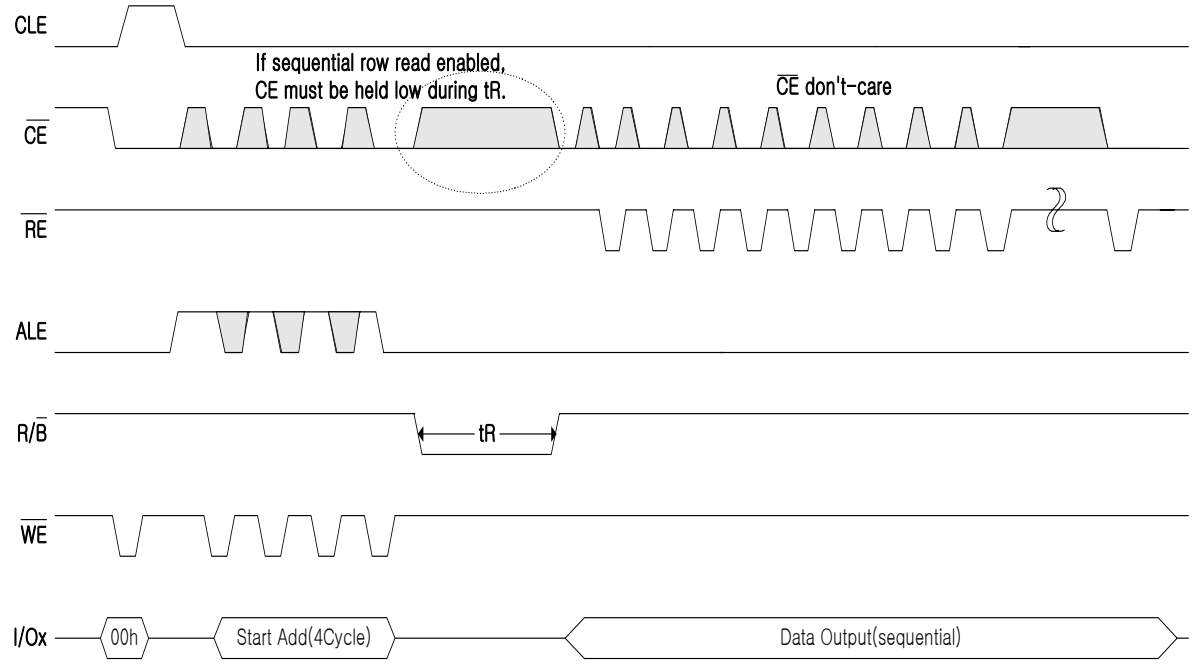


Figure 33. Read Operation with $\overline{CE}$ don't-care.

Ready/Busy Signal Electrical Characteristics

Figures 32, 33 and 34 show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{CCmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of tr.

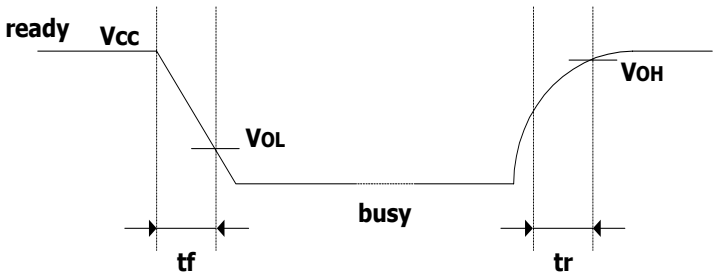


Figure 34. Ready/Busy AC Waveform

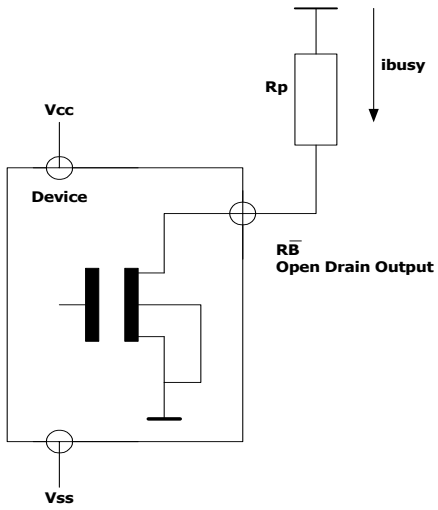


Figure 35. Ready/Busy Load Circuit

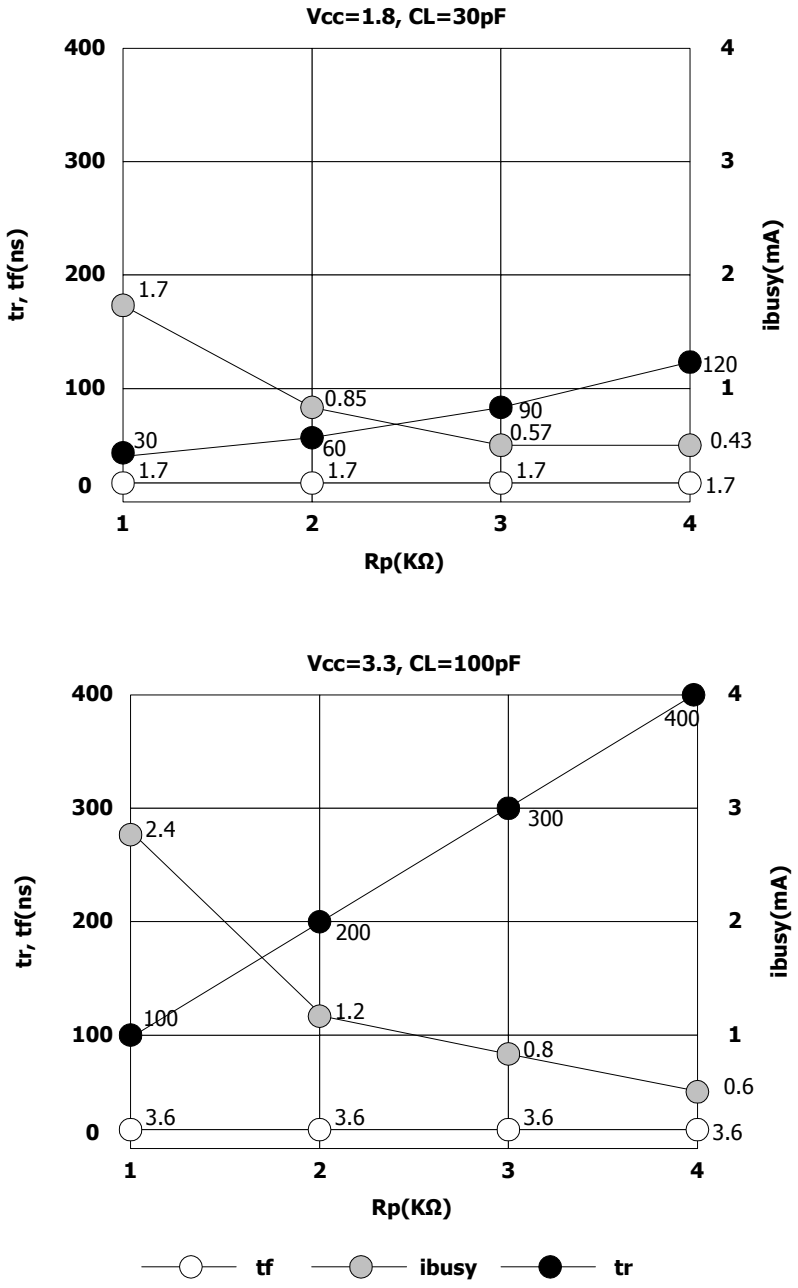


Figure 36. Resistor Value Waveform Timings for Ready/Busy Signal

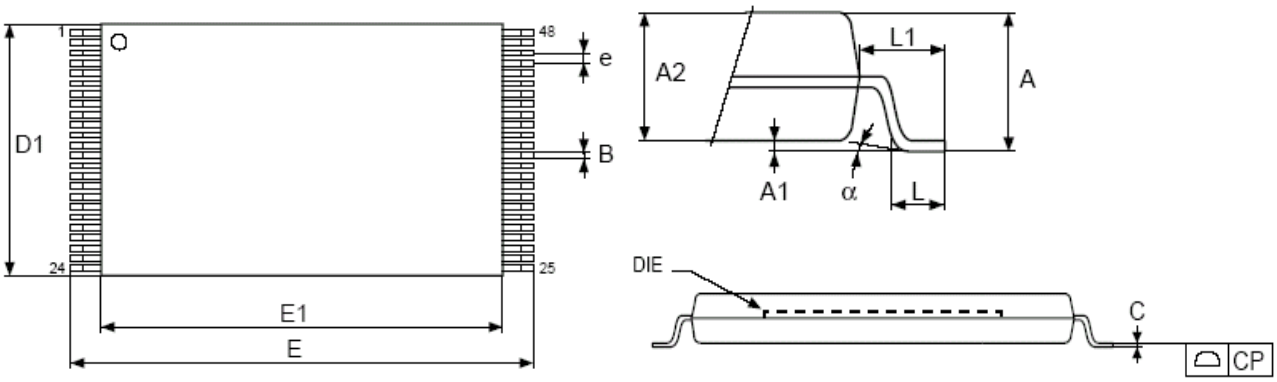


Figure 37. 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Table 16: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1	0.050	0.100	0.150	0.0020	0.0039	0.0059
A2	0.950	1.000	1.050	0.0374	0.0394	0.0413
B	0.170	0.220	0.270	0.0067	0.0087	0.0106
C	0.100		0.210	0.0039		0.0083
CP			0.080			0.0031
D1	11.900	12.000	12.100	0.4685	0.4724	0.4764
E	19.800	20.000	20.200	0.7795	0.7874	0.7953
E1	18.300	18.400	18.500	0.7205	0.7244	0.7283
e	-	0.500	-	-	0.0197	-
L	0.500	0.600	0.700	0.0197	0.0236	0.0276
L1	-	0.800	-		0.0315	
alpha	0	3	5	0	3	5

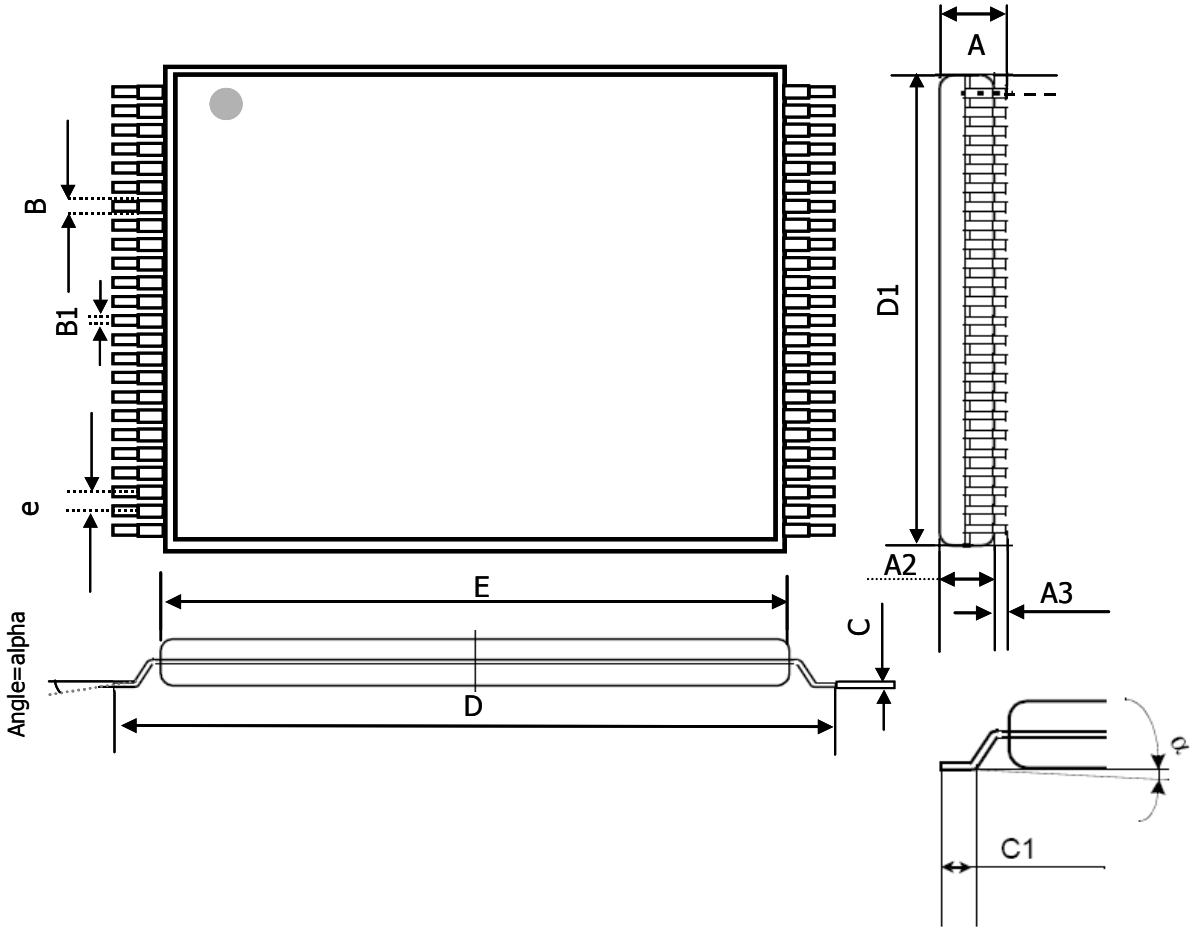


Figure 38. 48-WSOP1 - 48-lead Plastic Very Very Thin Small Outline, 12 x 17mm, Package Outline

Table 17: 48-WSOP1 - 48-lead Plastic Thin Small Outline, 12 x 17mm, Package Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			0.70			0.0276
A2	0.540	0.580	0.620	0.0213	0.0229	0.0244
A3			0.10			0.0039
B	0.170	0.200	0.270	0.0067	0.0079	0.0106
B1	0.130	0.160	0.230	0.0051	0.0063	0.0091
C	0.065	0.10	0.135	0.0026	0.0039	0.0053
C1	0.45		0.75	0.018		0.0300
D	16.80	17.00	17.20	0.6619	0.6698	0.6777
D1	11.90	12.00	12.10	0.4689	0.4728	0.4767
E	15.30	15.40	15.50	0.6028	0.6068	0.6107
e	0.44	0.50	0.56	0.0173	0.0197	0.0221
alpha	0		8	0		8

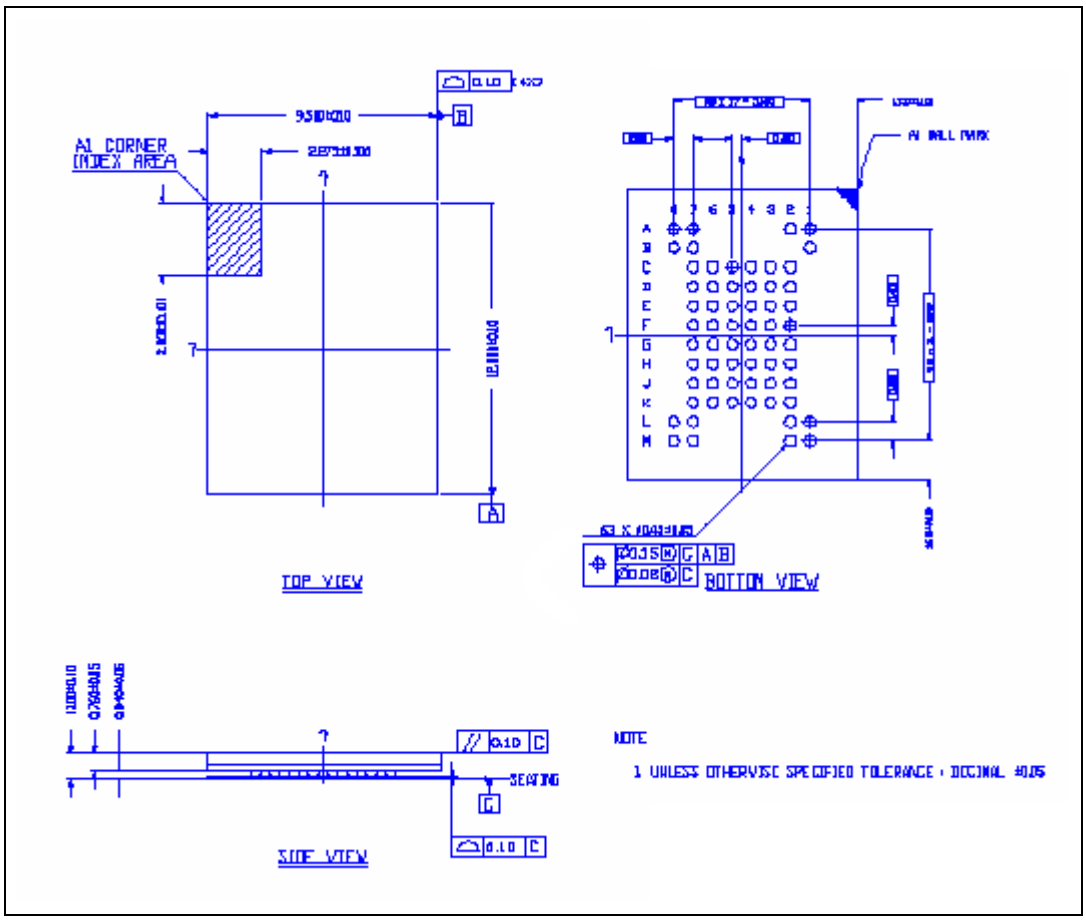
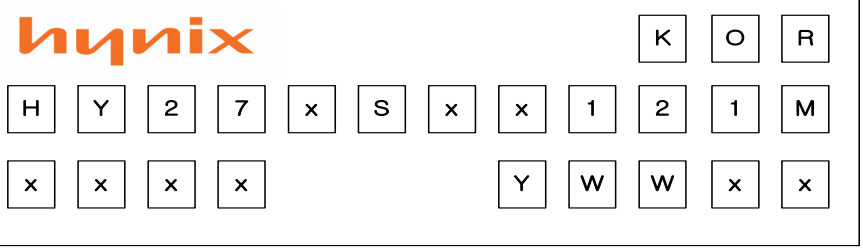


Figure 39. 63-FBGA - 8.5 x 15mm, 6x8 ball array 0.8mm pitch, Pakage Outline

Note: Drawing is not to scale.

MARKING INFORMATION

Package	Marking Example
TSOP1 / WSOP1 / FBGA	

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27xSxx121mTxB	: Part Number
HY: HYNIX	
27: NAND Flash	
x: Power Supply	: U(2.7V~3.6V), S(1.7V~2.2V)
S: Classification	: Single Level Cell+Single Die
xx: Bit Organization	: 08(x8), 16(x16)
12: Density	: 512Mb
1: Mode	: 1nCE & 1R/nB; CE don't care
M: Version	: 1st Generation
x: Package Type	: T(TSOP1), V(WSOP1), F(FBGA)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Operating Temperature	: C(0℃~70℃), E(-25℃~85℃) I(-40℃~85℃)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
- Y: Year (ex: 4=year 2004, 05= year 2005)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item