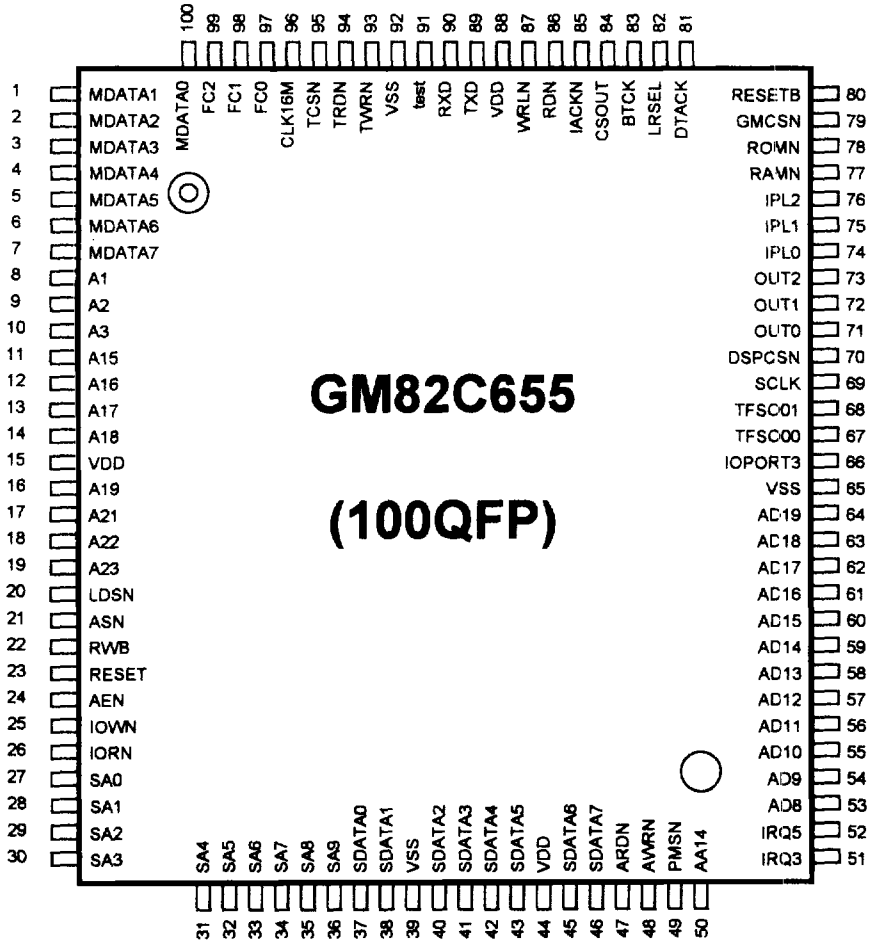
1. General Description

The GM82C655 is the single-chip integration of the interface modules between the PC and the Sound IC. It contains a UART (8250), a TIMER (8254), an MPU-401, and CPU Address Coding. With the GM82C655 and the GM82C650 Sound IC, the customer can build up a Sound Card, a Sound Module, or other types of sound-related systems by simply adding a CPU (62EC000) and DSP.

2. Feature

1. 68000 CPU Interface and Decoder Logic
2. MPU-401 Mode Support
3. PC Interface logic for DRAM Download
4. ADSP-2115 Interface Logic
5. Fully compatible UART (Universal Asynchronous Receiver/Transmitter) included
6. Programmable TIMER included
7. Fabricated on a high-performance, 0.8 micron, CMOS process
8. 100 pin QFP

3. Package configuration

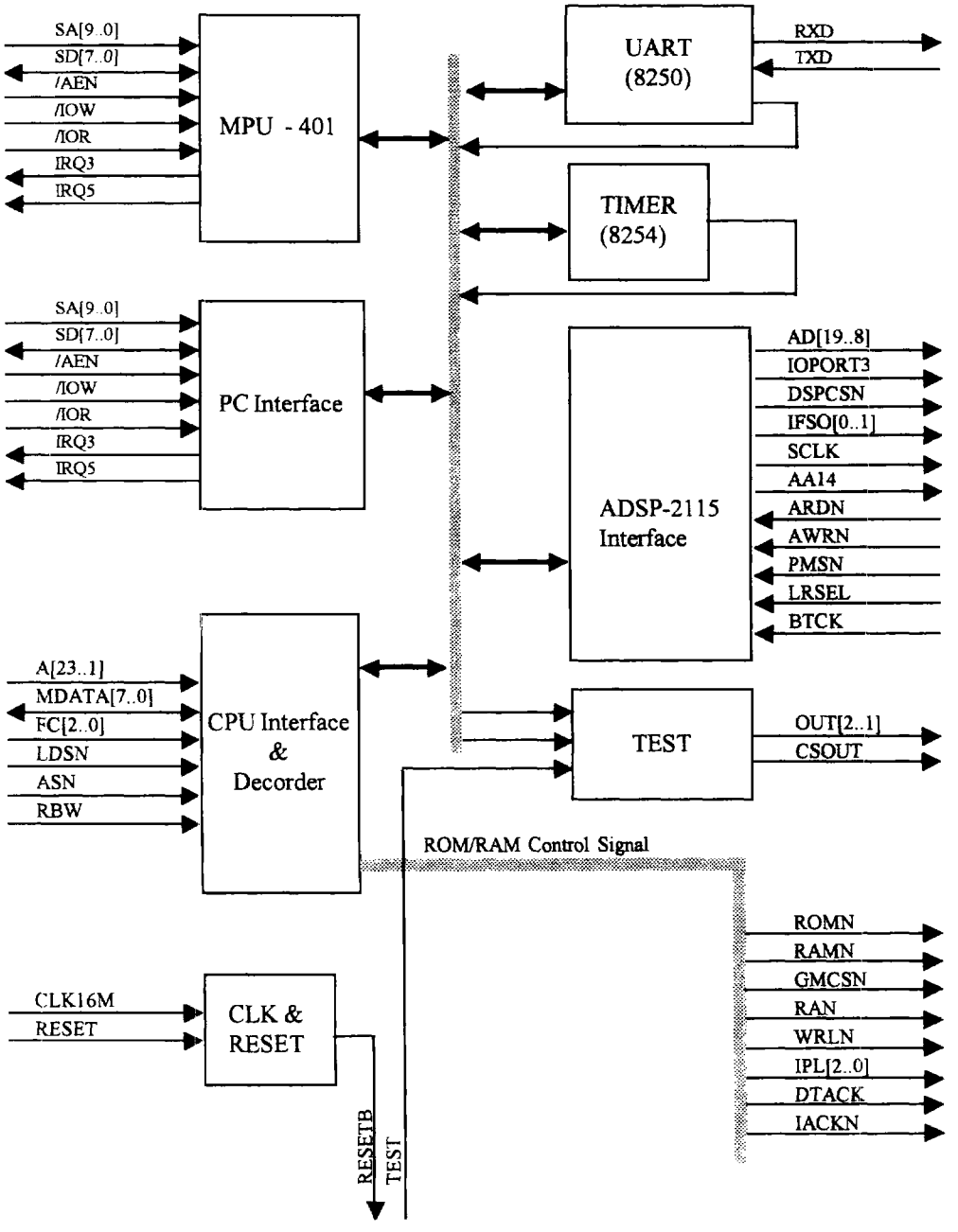


4. 82C655 Pin function & Description

Pin No.	Pin name	I/O	Pin function	Pin No.	Pin name	I/O	Pin function
1	MDATA1	I/O-PU	MPU DATA I	26	IORN	I-PU	PC Read enable
2	MDATA2	I/O-PU	MPU DATA 2	27	SA0	I	Slot Address 0
3	MDATA3	I/O-PU	MPU DATA 3	28	SA1	I	Slot Address 1
4	MDATA4	I/O-PU	MPU DATA 4	29	SA2	I	Slot Address 2
5	MDATA5	I/O-PU	MPU DATA 5	30	SA3	I	Slot Address 3
6	MDATA6	I/O-PU	MPU DATA 6	31	SA4	I	Slot Address 4
7	MDATA7	I/O-PU	MPU DATA 7	32	SA5	I	Slot Address 5
8	A1	I	MPU Address 1	33	SA6	I	Slot Address 6
9	A2	I	MPU Address 2	34	SA7	I	Slot Address 7
10	A3	I	MPU Address 3	35	SA8	I	Slot Address8
11	A15	I	MPU Address 15	36	SA9	I	Slot Address 9
12	A16	I	MPU Address 16	37	SDATA0	I/O-PU	Slot DATA 0
13	A17	I	MPU Address 17	38	SDATA1	I/O-PU	Slot DATA 1
14	A18	I	MPU Address 18	39	VSS		
15	VDD			40	SDATA2	I/O-PU	Slot DATA 2
16	A19	I	MPU Address 19	41	SDATA3	I/O-PU	Slot DATA 3
17	A21	I	MPU Address 21	42	SDATA4	I/O-PU	Slot DATA 4
18	A22	I	MPU Address 22	43	SDATA5	I/O-PU	Slot DATA 5
19	A23	I	MPU Address 23	44	VDD		
20	LDSN	I-PU	LOw strobe	45	SDATA6	I/O-PU	Slot DATA 6
21	ASN	I-PU	Address Strobe Enable	46	SDATA7	I/O-PU	Slot DATA 7
22	RWB	I	Read,Write select	47	ARDN	I-PU	Effect Read Select
23	RESET	I	Reset Signal	48	AWRN	I-PU	Effect Write Select
24	AEN	I-PU	PC Address Enable	49	PMSN	I-PU	Effect Program Select
25	IOWN	I-PU	PC Write Enable	50	AA14	O	Effect Address 14

Pin No.	Pin name	I/O	Pin function	Pin No.	Pin name	I/O	Pin function
51	IRQ3	O	PC Interrupt 3	76	IPL2	O	Interrupt Priority Level 2
52	IRQ5	O	PC Interrut 5	77	RAMN	O	RAM Select
53	AD8	O	Effect DATA 8	78	ROMN	O	ROM Select
54	AD9	O	Effect DATA 9	79	GMCSN	O	Sound Chip Select
55	AD10	O	Effect DATA 10	80	RESETB	O	Reset Low Active
56	AD11	O	Effect DATA 11	81	DTACK	O	DATA Transifer Acknowledge
57	AD12	O	Effect DATA 12	82	LRSEL	I	Left Right Select
58	AD13	O	Effect DATA 13	83	BTCK	I	Bit CLOCK
59	AD14	O	Effect DATA 14	84	GMCSN	O	Chip Select Out
60	AD15	O	Effect DATA 15	85	IACKN	O	Interrupt Acknowledge
61	AD16	O	Effect DATA 16	86	RDN	O	Read Enable
62	AD17	O	Effect DATA 17	87	WRLN	O	Write Enable
63	AD18	O	Effect DATA 18	88	VDD		
64	AD19	O	Effect DATA 19	89	TXD	O	Serial DATA Output
65	VSS			90	RXD	I	Serial DATA Input
66	IOPORT3	O	Effect Reset	91	test	I	Test Pin
67	TFSO0	O	Effect Transmit Frame Synchronization	92	VSS		
68	TFSO1	O	Effect Transmit Frame Synchronization	93	TWRN	I	Test Write Select
69	SCLK	O	Effect Serial Clock	94	TRDN	I	Test Read Select
70	DSPCSN	O	Effect Chip Select	95	TCSN	I	Test Chip Select
71	OUT0	O	Timer Output 0	96	CLK16M	I	CLOCK
72	OUT1	O	Timer Output 1	97	FC0	I	Function Select 0
73	OUT2	O	Timer Output 2	98	FC1	I	Function Select 1
74	IPL0	O	Interrupt Priority Level 0	99	FC2	I	Function Select 2
75	IPL1	O	Interrupt Priority Level 1	100	MDATA0	I/O-PU	MPU DATA 0

5. Function Block Diagram



6. Electrical Chracteristics.

6-1. Electronical Discharge Immunity

the circuit shall be tolerant of up to 2000V of electrostatic discharge at discharge cap 100pF and register 1.5kΩ(Military Standard)

6-2. Operating Characterstics

6-2-1. Absolute Maximum conditions (referenced to Vss)

symbol	Parameter	Limits	UNIT
V_{dd}	DC Supply Voltage	-0.3 to 7	V
Vi	Input Voltage	-0.3 to Vdd+0.3	V
Ii	DC Input Current	-10 to 10	mA
Tstg	Stroage Temp. Range	-40 to 125	℃

6-2-2. Recommanded Operating Conditions (referenced to Vss)

symbol	Parameter	Limits	UNIT
Vdd	DC Supply voltage	4.75 to 5.25	V
Ta	Operating Ambient Temp. Range	0 to 70	℃

6.3. DC characteristics

Symbol	Parameter	MIN	TPY	MAX	UNIT	Condition
Vih	High Level input Voltage				V	
	TTL level	2.0				
	CMOS level	0.7 V_{DD}				
	SCHMIT T triger		3.0	4.0		
Vil	Low Level input Voltage				V	
	TTL level			0.8		
	CMOS level			0.3 V_{DD}		
	SCHMIT T triger	1.0	1.5			
Iih	High Level input current				μA	Vin = Vdd
	TTL / CMOS input	-10		10		
	Input with pull-down		12			
Iil	Low Level output current				μA	Vin = Vss
	TTL / CMOS input	-10		10		
	Input with pull-down		-12			
Voh	High Level output voltage	2.4			V	
	Type B2					Ioh = -2mA
	Type B4					Ioh = -4mA
	Type B8					Ioh= -8mA
	Type B12					Ioh= -12mA
Vol	Low Level output voltage			0.4	V	
	Type B2					Iol = -2mA
	Type B4					Iol = -4mA
	Type B8					Iol= -8mA
	Type B12					Iol= -12mA
Ioz	Three-state output Leakage current	-10		-10	μA	Vout = Vss or Vdd
Idds	Quiescent supply current	User-Design Dependent				Vin = Vdd or Vss
Cin	Input Capacitance	Input Buffer Dependant			pF	any input
Cout	Output Capacitance	Output Buffer Dependant			pF	any output

7. General Discription

7.1 MPU-401 BLOCK

MPU-401 Interface block is used exclusively for communication MIDI and command data between the PC and the on-board synthesizer.

7.2 PC Interface BLOCK

PC interface is used for down loding of sample data. It includes handshake logic, data latch and address decoder

7.3 CPU interface and Decoder BLOCK

It includes address decoder logic ,M68000 CPU, ROM/RAM select signal and other peripherals decoder logic

7.4 ADSP-2115 Interface BLOCK

It includes ADSP-2115 effect DSP control logic generation, data latch and M68000 CPU interface logic

7.5 UART BLOCK

It is fully compatible UART (Intel 8250) but It is only used MIDI serial port. To support MIDI (31.25 Kbps, No Parity , 1 Stop bit, 8 Data bit) set your program driver

1) Write 80h in LCR(Line Control Register) , Access DLL(Divisor Latch LSB)
DLM(Divisor Latch MSB)

2) Write 00h in DLM

3) Write 04h in DLL ; Divisor # = FREQUENCY INPUT / (BAUD RATE * 16)
2MHz / (31.25k * 16) = 4

4) Write 03h LCR , Word length 8 bit (8 data bit)

5) Write 01h in IER (Interrupt Enable Register) , When data received RBR(Recever Buffer Register), Accept Interrupt

note : For data transferd. Use THR (Transmitter Holding Register)

7.6. TIMER BLOCK

GM82C655 include TIMER/ COUNTER. That is same Intel 82C54 which is designed to solve the timing control problems common in microcomputer system design. It provide three independent 16-bit counters. All mode are software programable

Counters are programed by writing a control word and then an initial count. The control word format is shown in Fig 8.1.

Fig 7.1. control word Format

Control word Format

A1,A0=11 /CS=0 /RD=1 /WR=0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	SCD

SC : Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2

M -Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW (Read / Write)

1	1	Read / Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16 Bits
1	binary coded Decimal (BCD) Counter (4 Decades)

EXAMPLE

Input CLK is 2MHz, To obtain 500MHz square wave from OUT 1 programing in your driver.

1. Initialize Counter 0

: Select Counter 0 , LSB and then MSB Read / Write Mode 3

Write 00110110b (36h) in control Word Register

Write 0 in COUNTER 0 → LSB WRITE
Write 2 in COUNTERODP → MSB WRITE

RESULT : 2,000,000 / 2 = 1,000,000 (=1MHz)

2.Initialize Counter 2

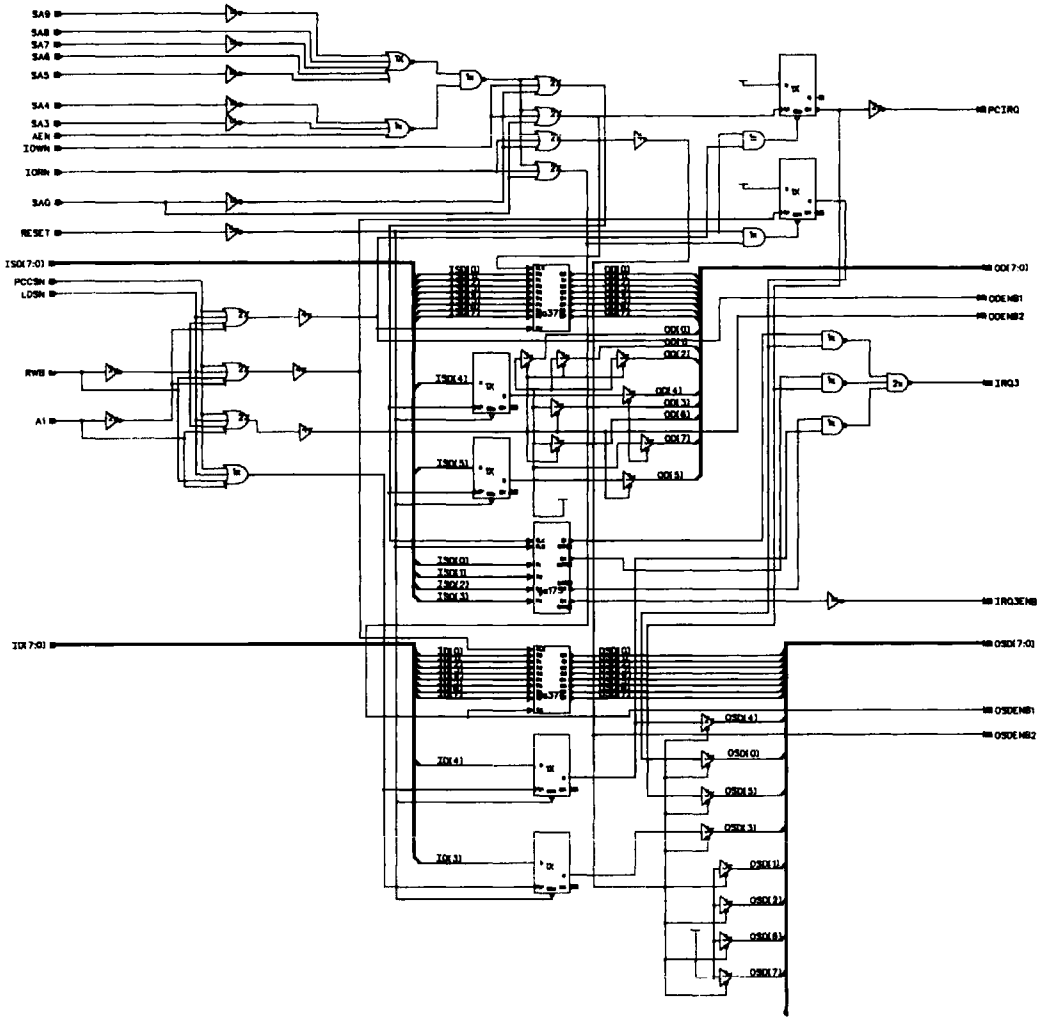
Write 01110110b (76h) in control Word Register : Select Counter 1 , LSB and then MSB Read / Write Mode 3

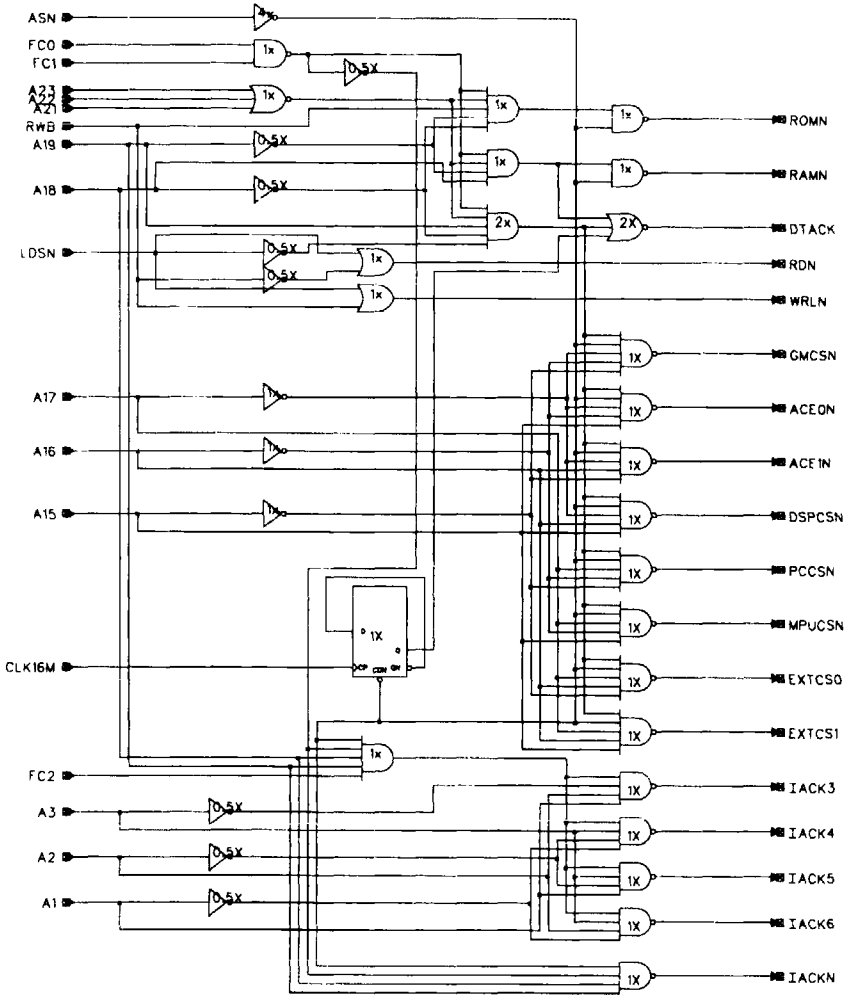
Write low 8 bit of 2000 in Counter 1 → LSB WRITE
Write high 8 bit of 2000 in counter 1 → MSB WRITE

RESULT : 1,000,000 / 2000 = 500 (=1MHz)

Referance : 82C54 SPEC.

Compass Design Automation plot [la]pcint by hscad on 13-Apr-95 at 2:45 A.M.




ASN
FC0
FC1
A23
A22
A21
RWB
A19
A18
LDSN
A17
A16
A15
CLK16M
FC2
A3
A2
A1
ROMN
RAMN
DTACK
RDN
WRLN
GMCSN
ACEON
ACEIN
DSPCSN
PCCSN
MPUCSN
EXTCS0
EXTCS1
IACK3
IACK4
IACK5
IACK6
IACKN

Compass Design Automation plot [la]dspint by hscad on 11-Apr-95 at 5:38 P.M.