2 Gigabit Stacked DDR2 SDRAM

DD53E 256Mb x 8

Features

- Low Profile 63 Ball Two-High Stacked Die *micropede*™ BGA.
- 8 x 11.5 x 1.35mm BGA Package
- 50% Space Savings Over Two 60 Ball BGA Packages
- Reduced Trace Lengths Over Two BGA Packages
- Lead Free—High Temperature Solder Balls
- Data Rates Up to 800 Mb per Second
- Organization: 8 Banks x 32M x 8 bits
- DDR2 Double Data Rate Fully Synchronous DRAM
- V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V
- JEDEC Standard 1.8V I/O (SSTL_18 Compatible)
- Differential Data Strobe (DQS, DQS#) Option
- Duplicate Output Strobe (RDQS) option
- DLL to align DQ and DQS Transitions with CK
- Eight Internal Banks for Concurrent Operation
- Programmable CAS Latency (CL)
- Posted CAS Additive Latency (AL)
- WRITE Latency = READ Latency –1 t_{CK}
- Programmable Burst Lengths: 4 or 8
- Adjustable Data-Output Drive Strength
- 64ms, 8,192-Cycle Refresh
- On-Die Termination (ODT)
- 16K Row Addressing (A0—A13)
- 8 Bank Addressing (BA0—BA2)
- 1K Column Addressing (A0-A9)
- Low Thermal Resistance: Theta (JB) = 5.9 °C/W

General Description

The device is a 1.8 volt, 2 gigabit (2,147,483,648 bit) high speed DDR2 Double Data Rate Synchronous DRAM memory module organized as 8 banks x 32M x 8 bits in a 63 ball *micropede*™ BGA.

The high speed throughput is achieved by minimizing the internal package interconnect. The *micropede*™ BGA has less than half of the inductance of a standard TSOP package. The *micropede*™, a CSP die stack, is mounted on a BGA substrate allowing two die to occupy the same board space as a single monolithic packaged part.

The high speed data throughput is also achieved by interconnecting the two 8-bit wide die with all signals in common except for the Chip Select, Clock Enable, and On-Die Termination pins. This scheme dramatically reduces the pin count, allows versatility, and supports future system upgrades utilizing the same pin-out.

The 2Gb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 32 bit prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 2Gb DDR2 SDRAM effectively consists of a single 32-bit-wide, one-clock cycle data transfer at the internal DRAM core and four corresponding *4*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS and DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 2Gb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed.

The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

Ordering Information

Part ID	Clock Frequency/Data Rate	CL-tRCD-tRP (t_{CK})
2D256M82U4BA9	200MHz/400Mbps @ CL3	3-3-3
2D256M82U4BA7	266MHz/533Mbps @ CL4	4-4-4
2D256M82U4BA5	333MHz/667Mbps @ CL5	5-5-5
2D256M82U4BA3	400MHz/800Mbps @ CL5	5-5-5

*CL = CAS (Read) Latency

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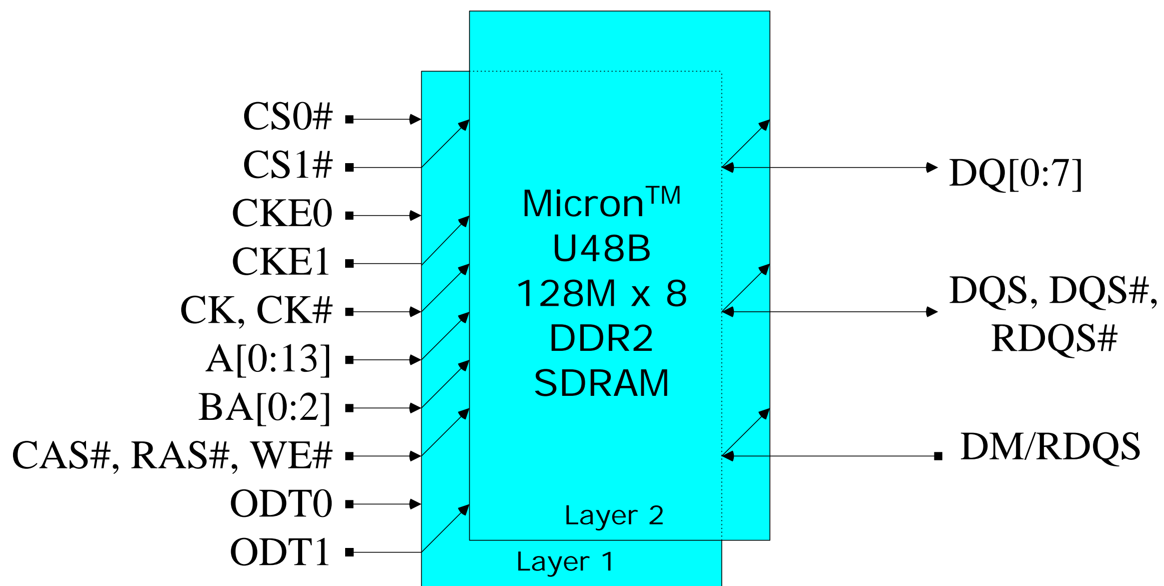
As with standard DDR SDRAMs, the pipelined, multi-bank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

The module has been designed to have low thermal resistance and exhibits less than a 5 °C internal temperature gradient during operation in still air under IDD7 conditions.

Block Diagram



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Ball Out Locations

63 Ball FBGA

	1	2	3	4	5	6	7	8	9
A	VDD	RDQS#	VSS				VSSQ	/DQS	VDDQ
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5
E	VDDL	VREF	VSS				VSSDL	CK	VDD
F		CKE0	WE#				RAS#	CK#	ODT0
G	BA2	BA0	BA1				CAS#	CS0#	CS1#
H	CKE1	A10/AP	A1				A2	A0	VDD
J	VSS	A3	A5				A6	A4	ODT1
K		A7	A9				A11	A8	VSS
L	VDD	A12	NC				NC	A13	

Top View
(Looking through the Package)

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micropede™ Package Mechanical Outline

63 Ball Lead-Free BGA
Notes:
1. All dimensions are in millimeters [inches]
2. Solder ball material: 96.5% Sn, 3% Ag, and 0.5% Cu
3. Symbol ▨ denotes a dummy land pad without a solder ball.