agere systems

Data Sheet
November 2006

USS2000 Four-Port USB2.0 PCI-to-USB Host Controller

1 Features

- 32-bit, 33 MHz PCI interface compliant with *PCI Local Bus Specification* Revision 2.2.
- Four downstream USB ports.
- Compliant with *Universal Serial Bus Specification* Revision 2.0.
- Embedded OHCI core compliant with *OpenHCI Open Host Controller Interface Specification for USB* Release 1.0a.
- Embedded EHCI core compliant with *Enhanced Host Controller Interface Specification* Revision 1.0.
- Compatible with *Microsoft Windows*® standard OpenHCI and EHCI drivers.
- Listed on *Windows* hardware compatibility list http://testedproducts.windowsmarketplace.com/.
- Supported on *Mac OS*®10.3 and higher and on *Linux*® 2.4.22 and higher.
- 3 V or 5 V switchable PCI signaling.
- Low-power mode and wake-up compatible with *PCI Power Management Interface Specification* Revision 1.1.
- Integrated high-speed, full-speed, and low-speed USB transceivers.
- Integrated PLL creates all required EHCI and OHCI clocks from 30 MHz clock input.
- Support for legacy keyboard and mouse.
- Available in two package types:
  — 128 TQFP.
  — 161 FSBGA*.
- Evaluation kit:
  — PCI card.
  — Schematics.
  — Gerber files.
  — Data sheets.
- 0.2 μm technology.
- Provides five USB host controllers:
  — Four OHCI (12 Mbits/s each).
  — One EHCI (480 Mbits/s).

* The term pin is used throughout the text, but if an FSBGA package is used, then the term ball is assumed to replace the term pin.

2 Applications

- Seamless integration with 3 V or 5 V PCI-based computer products.
- Supports high-speed, full-speed, or low-speed USB-compliant devices and hubs connected to any port.
- Simultaneous operation of multiple high-performance devices.

3 Description

The Agere USS2000 provides a single-chip, four-port PCI-to-universal serial bus (USB) 2.0 solution. The USS2000 interfaces directly to a 32-bit, 33 MHz PCI bus and is ideal for either onboard applications or add-in card applications. It can easily be configured to communicate in either a 3 V PCI environment or 5 V PCI environment simply by selecting the appropriate communications voltage level on the VIO input pin.

The USS2000 provides four downstream USB ports for connectivity with a USB2.0 compliant device or hub. High-speed (480 Mbits/s), full-speed (12 Mbits/s), or low-speed (1.5 Mbits/s) peripherals are supported along with all of the USB transfer types: control, interrupt, bulk, or isochronous. Split transaction support is also provided for communication with USB2.0 high-speed hubs. The USS2000's OpenHCI compliance offers USB performance benefits and reduced CPU overhead compared to many other USB host controllers. EHCI compliance provides connectivity of high-speed USB2.0 devices to operate up to 480 Mbits/s.

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3 Description (continued)

In addition, the USS2000 offers a performance advantage for full-speed and low-speed devices over single USB host controllers (both UHCI and OHCI) by providing four integrated OHCI host controllers, each with one port. Each OCHI host controller provides dedicated 12 Mbits/s for a total of 48 Mbits/s allowed for connected full-speed or low-speed devices. This can result in an increase in the number of devices that can feasibly be connected to a computer system as well as ensure that high-bandwidth devices, such as video cameras and audio devices, are always provided with the high bandwidth they need while other USB devices are in use.

The USS2000 provides support for legacy PC peripherals as defined in the *OpenHCI Open Host Controller Interface Specification for USB* Release 1.0a.

The USS2000 provides an advanced PCI power management interface as specified in the *Enhanced Host Controller Interface Specification* Revision 1.0, Appendix A. It offers a variety of power savings to a system while retaining the ability to wake upon specified wake events.

The USS2000 supports the port wake capabilities, port power controls, programmable frame list size, and light host controller reset as defined in *Enhanced Host Controller Interface Specification* Revision 1.0.

The USS2000 does not support the optional port indicator interface or 64-bit addressing as defined in *Enhanced Host Controller Interface Specification* Revision 1.0.

The USS2000 is compatible with the *Microsoft Windows* standard OpenHCI and EHCI drivers.

The USS2000 is a 3.3 V device fabricated in 0.2 μm technology.

The USS2000 is functional as a OHCI host controller in the absence of EHCI drivers installed in the host system.

3 Description (continued)

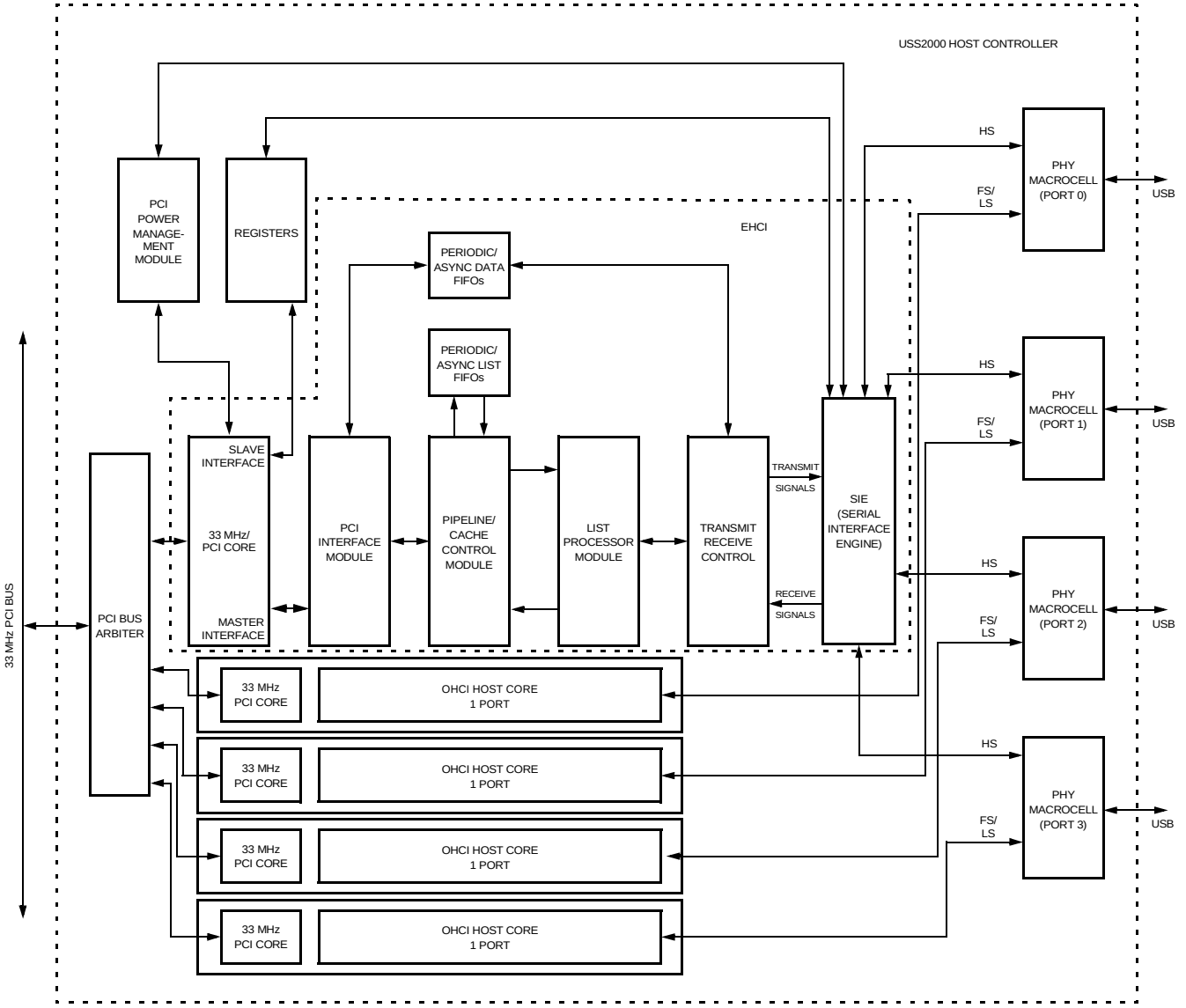

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Figure 1. USS2000 Block Diagram

4 Pin Information

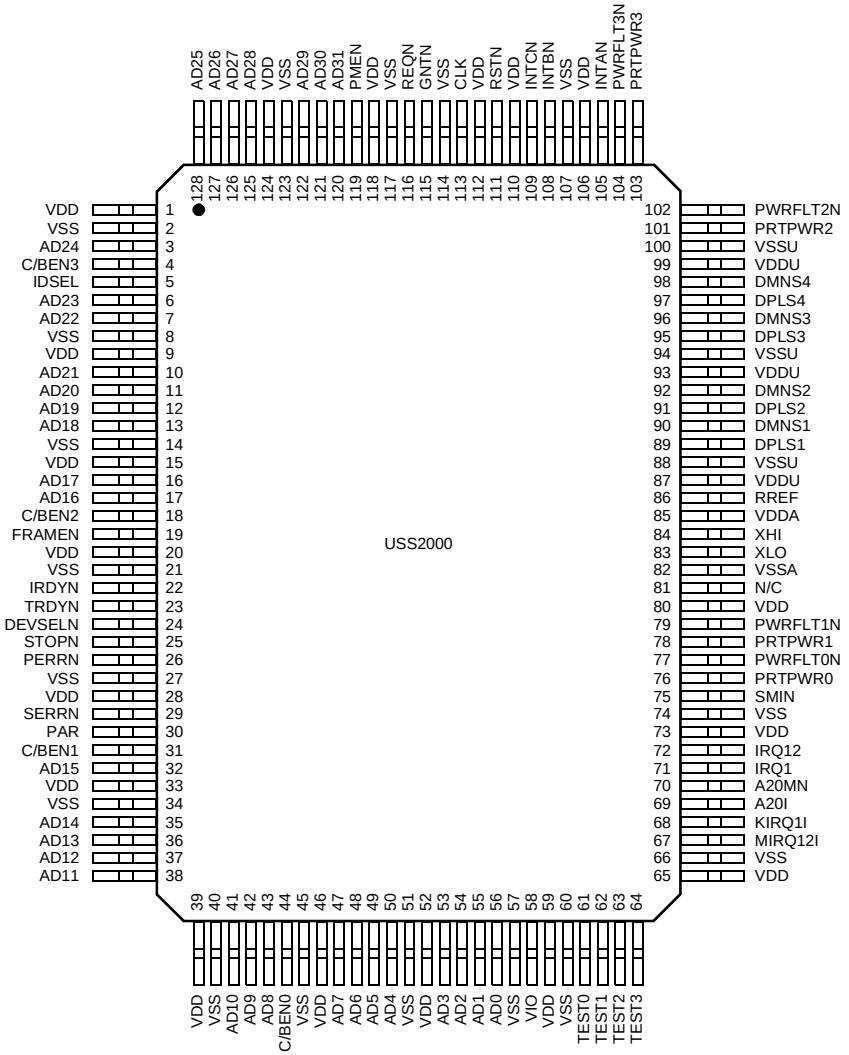

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Figure 2. USS2000 Pin Diagram

4 Pin Information (continued)

Table 1. Numeric Pin Cross Reference

Pin	Symbol*	Pin	Symbol*	Pin	Symbol*	Pin	Symbol*
1	VDD	33	VDD	65	VDD	97	DPLS3
2	VSS	34	VSS	66	VSS	98	DMNS3
3	AD24	35	AD14	67	MIRQ12I	99	VDDU
4	C/BEN3	36	AD13	68	KIRQ1I	100	VSSU
5	IDSEL	37	AD12	69	A20I	101	PRTPWR2
6	AD23	38	AD11	70	A20MN	102	PWRFLT2N
7	AD22	39	VDD	71	IRQ1	103	PRTPWR3
8	VSS	40	VSS	72	IRQ12	104	PWRFLT3N
9	VDD	41	AD10	73	VDD	105	INTAN
10	AD21	42	AD9	74	VSS	106	VDD
11	AD20	43	AD8	75	SMIN	107	VSS
12	AD19	44	C/BEN0	76	PRTPWR0	108	INTBN
13	AD18	45	VSS	77	PWRFLT0N	109	INTCN
14	VSS	46	VDD	78	PRTPWR1	110	VDD
15	VDD	47	AD7	79	PWRFLT1N	111	RSTN
16	AD17	48	AD6	80	VDD	112	VDD
17	AD16	49	AD5	81	N/C	113	CLK
18	C/BEN2	50	AD4	82	VSSA	114	VSS
19	FRAMEN	51	VSS	83	XLO	115	GNTN
20	VDD	52	VDD	84	XHI	116	REQN
21	VSS	53	AD3	85	VDDA	117	VSS
22	IRDYN	54	AD2	86	RREF	118	VDD
23	TRDYN	55	AD1	87	VDDU	119	PMEN
24	DEVSELN	56	AD0	88	VSSU	120	AD31
25	STOPN	57	VSS	89	DPLS0	121	AD30
26	PERRN	58	VIO	90	DMNS0	122	AD29
27	VSS	59	VDD	91	DPLS1	123	VSS
28	VDD	60	VSS	92	DMNS1	124	VDD
29	SERRN	61	TEST0	93	VDDU	125	AD28
30	PAR	62	TEST1	94	VSSU	126	AD27
31	C/BEN1	63	TEST2	95	DPLS2	127	AD26
32	AD15	64	TEST3	96	DMNS2	128	AD25

* Pins identified as NC are unused and should be left unconnected. Active-low signals within this document are indicated by an N following the symbol names.

5 Ball Information

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
—	PRT PWR3	PWR FLT4N	VDD	—	VSS	—	—	—	VSS	—	AD[28]	AD[25]	VDD	—	A
VSSU	—	PWRFL T3N	VSS	VSS	INTBN	—	—	—	PMEN	VDD	VDD	AD[26]	—	VSS	B
VSS	VDDU	—	PRTPW R4	INTAN	VSS	INTCN	—	REQN	VSS	AD[30]	VSS	—	C/BEN3	AD[24]	C
DMNS4	DMNS3	DPLS4	—	—	VSS	VDD	—	VSS	GNTN	—	—	AD[22]	AD[23]	IDSEL	D
—	VDDU	DMNS2	—	DPLS3	VSS	VDD	RSTN	CLK	AD[31]	VSS	—	VSS	VDD	—	E
DMNS1	DPLS2	DPLS1	VSSU	VSSU	VSS	VSS	VSS	VSS	VSS	AD[29]	AD[18]	AD[21]	AD[20]	AD[19]	F
—	—	VDDU	RREF	VDDA	VSS	VSS	VSS	VSS	AD[27]	VSS	VDD	AD[17]	—	—	G
—	—	—	—	VSSA	VDD	VSS	VSS	VSS	VSS	AD[16]	—	—	—	—	H
—	—	XHI	XLO	SMIN	VSS	VSS	VSS	VSS	VDD	VSS	C/BEN2	FRA-MEN	—	—	J
PWR FLT2N	PWR FLT1N	VSS	PRT PWR2	PRT PWR1	VSS	AD[3]	AD[6]	SERRN	AD[12]	VDD	STOPN	IRDYN	TRDYN	DEV SELN	K
—	VDD	IRQ1	—	TEST3	AD[2]	VSS	AD[5]	VSS	AD[8]	AD[14]	—	PERRN	VSS	—	L
IRQ12	KIRQI	A20MN	—	—	VDD	VDD	—	VSS	C/BEN0	—	—	VSS	C/BEN1	PAR	M
A20I	MIRQ12I	—	TEST0	VIO	VSS	AD[1]	—	AD[4]	VSS	VSS	VDD	—	AD[15]	VDD	N
VSS	—	VSS	TEST2	VSS	VSS	—	—	—	AD[7]	VSS	AD[9]	VSS	—	AD[13]	P
—	VSS	VDD	TEST1	—	AD[0]	—	—	—	VDD	—	AD[10]	VSS	AD[11]	—	R

Figure 3. Bottom View of USS2000 161-Ball FSBGA Package

5 Ball Information (continued)

Table 2. Ball Cross Reference by Signal

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
A20I	N15	AD[25]	A3	IRDYN	K3	VDD	R13	VSS	C10	VSS	K10
A20MN	M13	AD[26]	B3	IRQ1	L13	VDD	K5	VSS	G5	VSS	M7
AD[0]	R10	AD[27]	G6	IRQ12	M15	VDD	R6	VSS	L2	VSS	N10
AD[1]	N9	AD[28]	A4	KIRQI	M14	VDD	A12	VSS	P11	VSS	P3
AD[2]	L10	AD[29]	F5	MIRQ12I	N14	VDD	A2	VSS	A10	VSS	P5
AD[3]	K9	AD[30]	C5	PAR	M1	VDD	M10	VSS	B11	VSS	P10
AD[4]	N7	AD[31]	E6	PERRN	L3	VDD	B5	VSS	B12	VSS	P13
AD[5]	L8	C/BEN0	M6	PMEN	B6	VDD	G4	VSS	D10	VSS	R3
AD[6]	K8	C/BEN1	M2	PRTPWR1	K11	VDD	N1	VSS	E5	VSS	R14
AD[7]	P6	C/BEN2	J4	PRTPWR2	K12	VDD	B4	VSS	E10	VSS	C6
AD[8]	L6	C/BEN3	C2	PRTPWR3	A14	VDD	J6	VSS	F6	VSS	C15
AD[9]	P4	CLK	E7	PRTPWR4	C12	VDD	H10	VSS	F7	VSS	N5
AD[10]	R4	DEVSELN	K1	PWRFLT1N	K14	VDD	L14	VSS	F8	VSS	J5
AD[11]	R2	DMNS1	F15	PWRFLT2N	K15	VDD	D9	VSS	F9	VSS	C4
AD[12]	K6	DMNS2	E13	PWRFLT3N	B13	VDD	M9	VSS	F10	VSS	L7
AD[13]	P1	DMNS3	D14	PWRFLT4N	A13	VDD	E2	VSS	G7	VSS	D7
AD[14]	L5	DMNS4	D15	REQN	C7	VDD	E9	VSS	G8	VSS	K13
AD[15]	N2	DPLS1	F13	RREF	G12	VDD	N4	VSS	G9	VSS	M3
AD[16]	H5	DPLS2	F14	RSTN	E8	VDDA	G11	VSS	G10	VSS	E3
AD[17]	G3	DPLS3	E11	SERRN	K7	VDDU	E14	VSS	H6	VSS	L9
AD[18]	F4	DPLS4	D13	SMIN	J11	VDDU	G13	VSS	H7	VSSA	H11
AD[19]	F1	FRAMEN	J3	STOPN	K4	VDDU	C14	VSS	H8	VSSU	F11
AD[20]	F2	GNTN	D6	TEST0	N12	VIO	N11	VSS	H9	VSSU	F12
AD[21]	F3	IDSEL	D1	TEST1	R12	VSS	P15	VSS	J7	VSSU	B15
AD[22]	D3	INTAN	C11	TEST2	P12	VSS	B1	VSS	J8	XHI	J13
AD[23]	D2	INTBN	B10	TEST3	L11	VSS	N6	VSS	J9	XLO	J12
AD[24]	C1	INTCN	C9	TRDYN	K2	VSS	A6	VSS	J10	—	—

* Active-low signals within this document are indicated by an N following the symbol names.

5 Ball Information (continued)

Table 3. Ball Cross Reference by Ball Position

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A2	VDD	C12	PRTPWR4	F4	AD[18]	H9	VSS	K14	PWRFLT1N	N6	VSS
A3	AD[25]	C14	VDDU	F5	AD[29]	H10	VDD	K15	PWRFLT2N	N7	AD[4]
A4	AD[28]	C15	VSS	F6	VSS	H11	VSSA	L2	VSS	N9	AD[1]
A6	VSS	D1	IDSEL	F7	VSS	J3	FRAMEN	L3	PERRN	N10	VSS
A10	VSS	D2	AD[23]	F8	VSS	J4	C_BEN2	L5	AD[14]	N11	VIO
A12	VDD	D3	AD[22]	F9	VSS	J5	VSS	L6	AD[8]	N12	TEST0
A13	PWRFLT4N	D6	GNTN	F10	VSS	J6	VDD	L7	VSS	N14	MIRQ12I
A14	PRTPWR3	D7	VSS	F11	VSSU	J7	VSS	L8	AD[5]	N15	A20I
B1	VSS	D9	VDD	F12	VSSU	J8	VSS	L9	VSS	P1	AD[13]
B3	AD[26]	D10	VSS	F13	DPLS1	J9	VSS	L10	AD[2]	P3	VSS
B4	VDD	D13	DPLS4	F14	DPLS2	J10	VSS	L11	TEST3	P4	AD[9]
B5	VDD	D14	DMNS3	F15	DMNS1	J11	SMIN	L13	IRQ1	P5	VSS
B6	PMEN	D15	DMNS4	G3	AD[17]	J12	XLO	L14	VDD	P6	AD[7]
B10	INTBN	E2	VDD	G4	VDD	J13	XHI	M1	PAR	P10	VSS
B11	VSS	E3	VSS	G5	VSS	K1	DEVSELN	M2	C/BEN1	P11	VSS
B12	VSS	E5	VSS	G6	AD[27]	K2	TRDYN	M3	VSS	P12	TEST2
B13	PWRFLT3N	E6	AD[31]	G7	VSS	K3	IRDYN	M6	C/BEN0	P13	VSS
B15	VSSU	E7	CLK	G8	VSS	K4	STOPN	M7	VSS	P15	VSS
C1	AD[24]	E8	RSTN	G9	VSS	K5	VDD	M9	VDD	R2	AD[11]
C2	C_BEN3	E9	VDD	G10	VSS	K6	AD[12]	M10	VDD	R3	VSS
C4	VSS	E10	VSS	G11	VDDA	K7	SERRN	M13	A20MN	R4	AD[10]
C5	AD[30]	E11	DPLS3	G12	RREF	K8	AD[6]	M14	KIRQI	R6	VDD
C6	VSS	E13	DMNS2	G13	VDDU	K9	AD[3]	M15	IRQ12	R10	AD[0]
C7	REQN	E14	VDDU	H5	AD[16]	K10	VSS	N1	VDD	R12	TEST1
C9	INTCN	F1	AD[19]	H6	VSS	K11	PRTPWR1	N2	AD[15]	R13	VDD
C10	VSS	F2	AD[20]	H7	VSS	K12	PRTPWR2	N4	VDD	R14	VSS
C11	INTAN	F3	AD[21]	H8	VSS	K13	VSS	N5	VSS	—	—

* Active-low signals within this document are indicated by an N following the symbol names.

6 Pin/Ball Information

Table 4. PCI Signals

Pin	Ball	Symbol*	Type	Description
111	E8	RSTN	Input	**PCI Reset (Active-Low).**
113	E7	CLK	Input	**PCI System Clock (33 MHz).**
116	C7	REQN	Output/3-State	**PCI Request (Active-Low).**
115	D6	GNTN	Input	**PCI Grant (Active-Low).**
120, 121, 122, 125, 126, 127, 128, 3, 6, 7, 10, 11, 12, 13, 16, 17, 32, 35, 36, 37, 38, 41, 42, 43, 47, 48, 49, 50, 53, 54, 55, 56	E6, C5, F5, A4, G6, B3, A3, C1, D2, D3, F3, F2, F1, F4, G3, H5, N2, L5, P1, K6, R2, R4, P4, L6, P6, K8, L8, N7, K9, L10, N9, R10	AD[31:0]	Bidir	**PCI Address and Data.**
30	M1	PAR	Bidir	**PCI Parity.**
4, 18, 31, 44	C2, J4, M2, M6	C/BEN[3:0]	Bidir	**PCI Bus Command and Byte Enables.**
19	J3	FRAMEN	Bidir	**PCI Cycle Frame (Active-Low).**
22	K3	IRDYN	Bidir	**PCI Initiator Ready (Active-Low).**
23	K2	TRDYN	Bidir	**PCI Target Ready (Active-Low).**
25	K4	STOPN	Bidir	**PCI Stop (Active-Low).**
5	D1	IDSEL	Input	**PCI Initialization Device Select.**
24	K1	DEVSELN	Bidir	**PCI Device Select (Active-Low).**
26	L3	PERRN	Bidir	**PCI Parity Error (Active-Low).**
29	K7	SERRN	Output/Open Drain	**PCI System Error (Active-Low).**
105	C11	INTAN	Output/Open Drain	**PCI Interrupt A (Active-Low).**
108	B10	INTBN	Output/Open Drain	**PCI Interrupt B (Active-Low).**
109	C9	INTCN	Output/Open Drain	**PCI Interrupt C (Active-Low).**
119	B6	PMEN	Output/Open Drain	**Power Management Event (Active-Low).**
1, 9, 15, 20, 28, 33, 39, 46, 52, 59, 65, 73, 80, 106, 110, 112, 118, 124	A2, A12, B4, B5, D9, E2, E9, G4, H10, J6, K5, L14, M9, M10, N1, N4, R6, R13	VDD	Power	**3.3 V VDD.**
2, 8, 14, 21, 27, 34, 40, 45, 51, 57, 60, 66, 74, 107, 114, 117, 123	A6, A10, B1, B11, B12, C4, C6, C10, C15, D7, D10, E3, E5, E10, F6, F7, F8, F9, F10, G5, G7, G8, G9, G10, H6, H7, H8, H9, J5, J7, J8, J9, J10, K10, L2, L7, L9, M3, M7, N5, N6, N10, P3, P5, P11, P10, P13, P15, R3, R14, K13	VSS	Ground	**VSS.**
58	N11	VIO	Power	**PCI Environment Selection (3.3 V or 5 V).**

* An N following the symbol names indicates active-low for the USS2000.

6 Pin/Ball Information (continued)

Table 5. USB Port Signals

Pin	Ball	Symbol*	Type	Description
89	F13	DPLS1	Bidir	**USB Port 1 DPLUS.**
90	F15	DMNS1	Bidir	**USB Port 1 DMINUS.**
91	F14	DPLS2	Bidir	**USB Port 2 DPLUS.**
92	E13	DMNS2	Bidir	**USB Port 2 DMINUS.**
95	E11	DPLS3	Bidir	**USB Port 3 DPLUS.**
96	D14	DMNS3	Bidir	**USB Port 3 DMINUS.**
97	D13	DPLS4	Bidir	**USB Port 4 DPLUS.**
98	D15	DMNS4	Bidir	**USB Port 4 DMINUS.**
76	K11	PRTPWR1	Bidir	**USB Port 1 Power Enable (Active-Low).**
78	K12	PRTPWR2	Bidir	**USB Port 2 Power Enable (Active-Low).**
101	A14	PRTPWR3	Bidir	**USB Port 3 Power Enable (Active-Low).**
103	C12	PRTPWR4	Bidir	**USB Port 4 Power Enable (Active-Low).**
77	K14	PWRFLT1N	Input	**USB Port 1 Overcurrent (Active-Low).**
79	K15	PWRFLT2N	Input	**USB Port 2 Overcurrent (Active-Low).**
102	B13	PWRFLT3N	Input	**USB Port 3 Overcurrent (Active-Low).**
104	A13	PWRFLT4N	Input	**USB Port 4 Overcurrent (Active-Low).**
87, 93, 99	C14, E14, G13	VDDU	Power	**USB Transceiver VDD (3.3 V).**
88, 94, 100	B15, F11, F12	VSSU	Ground	**USB Transceiver VSS**.
86	G12	RREF	Input	**USB2.0 1 kΩ Precision Resistor Connection.** A 1 kΩ precision resistor ±1% should be connected to this pin. The opposite resistor end is connected to ground.
85	G11	VDDA	Power	**USB2.0 Analog Power.** PLL analog power (3.3 V).
82	H11	VSSA	Ground	**USB2.0 Analog Ground.** PLL analog ground.
84	J13	XHI	Output	**USB2.0 Crystal XHI Connection.** A 30 MHz (±100 PPM) crystal must be connected to this output.
83	J12	XLO	Input	**USB2.0 Crystal XLO Connection.** A 30 MHz (±100 PPM) crystal must be connected to this input.

* An N following the symbol names indicates active-low for the USS2000.

6 Pin/Ball Information (continued)

Table 6. Legacy Support Signals

Pin	Ball	Symbol*	Type	Description
68	M14	KIRQI	Input	**Legacy Keyboard Controller Interrupt (IRQ1 Input from Keyboard Controller).**
67	N14	MIRQ12I	Input	**Legacy Mouse Controller Interrupt (IRQ12 Input from Mouse Controller).**
69	N15	A20I	Input	**Legacy Gate A20 Input.**
70	M13	A20MN	Output/Open Drain	**Legacy Gate A20 Output (to Memory Controller).**
71	L13	IRQ1	Output/Open Drain	**System Keyboard Interrupt (Active-High).**
72	M15	IRQ12	Output/Open Drain	**System Mouse Interrupt (Active-High).**
75	J11	SMIN	Output/Open Drain	**System Management Interrupt (Active-Low).**

* An N following the symbol names indicates active-low for the USS2000.

Table 7. Chip Test Signals

Pin	Ball	Symbol*	Type	Description
61	N12	TEST0	Input	**Chip Test Signal.**
62	R12	TEST1	Input	**Chip Test Signal.**
63	P12	TEST2	Input	**Chip Test Signal.**
64	L11	TEST3	Input	**Chip Test Signal.**
81	—	NC	—	**No Connect.**

* An N following the symbol names indicates active-low for the USS2000.

7 System Configuration

Figure 4 depicts a standard system configuration using the USS2000. The USS2000 can interface directly with a 3 Vdc or 5 Vdc, 33 MHz, 32-bit PCI bus with no additional components required. The USS2000 is a port power-switched USB host controller providing the maximum control over USB device power consumption. This feature requires one 5 Vdc to 5 Vdc power switching regulator per USB port to allow the USS2000 to turn power on/off to each USB port under control of the operating system. The USS2000 contains four USB transceivers for direct connection of the USB DPLS and DMNS signals to the USB connector. Also included in the USS2000 is the legacy PS/2 mouse and keyboard interface as defined in the *OpenHCI Open Host Controller Interface Specification for USB* Release 1.0a. This legacy interface, along with standard USB BIOS drivers, allows USB mice and keyboards to operate in *MS-DOS*® mode. Legacy support need not be implemented by the system designer if not desired.

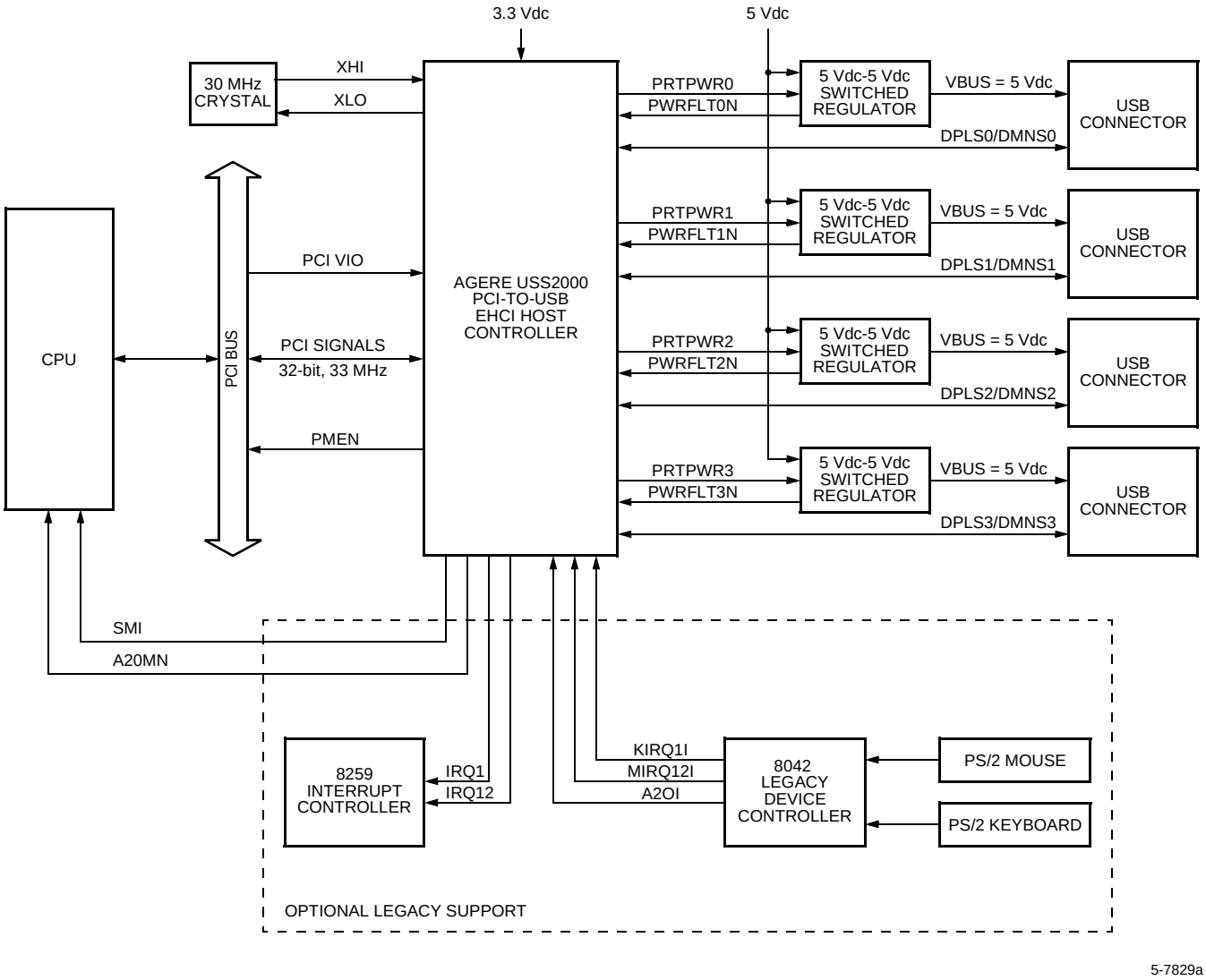

Figure 4. Standard System Configuration

8 PCI Register Overview

Table 8. PCI Bus Configuration Memory Summary

Function 0: OHCI
Function 1: OHCI
Function 2: OHCI
Function 3: OHCI
Function 4: EHCI

Refer to Tables 7—39 for more details on each of these registers.

Configuration Space Offset	Register Name	Read/ Write	Default Value (Reset)	
			OHCI	EHCI
00h—01h	Vendor ID	R	11C1h	11C1h
02h—03h	Device ID	R	5804h	5805h
04h—05h	Command	R/W	0000h	0000h
06h—07h	Status	R/W	230h	230h
08h	Revision ID*	R	12h	12h
09h—0Bh	Class Code	R	0C0310h	0C0320h
0Ch	Cache Line Size	R	10h	10h
0Dh	Latency Timer	R/W	40h	40h
0Eh	Header Type	R	80h	80h
0Fh	BIST	R	00h	00h
10h—13h	BAR 0	R/W	00000000h	00000000h
14h—17h	BAR 1	R	00000000h‡	00000000h‡
18h—1Bh	BAR 2	R	00000000h‡	00000000h‡
1Ch—1Fh	BAR 3	R	00000000h‡	00000000h‡
20h—23h	BAR 4	R	00000000h‡	00000000h‡
24h—27h	BAR 5	R	00000000h‡	00000000h‡
28h—2Bh	CardBus CIS Pointer	R	00000000h‡	00000000h‡
2Ch—2Dh	Subsystem Vendor ID	R/W†	11C1h	11C1h
2Eh—2Fh	Subsystem ID	R/W†	5804h	5805h
30h—33h	Expansion ROM Base Address	R	00000000h‡	00000000h‡
34h	Capabilities Pointer	R	50h	50h
3Ch	Interrupt Line	R/W	00h	00h
3Dh	Interrupt Pin	R	Test0 = 0b:01h Test0 = 1b:01h (Func. 0,1) :02h (Func. 2,3)	Test0 = 0b:01h Test0 = 1b:03h
3Eh	Min_Gnt	R	03h	10h
3Fh	Max_Lat	R	56h	20h
40h—43h	Wake-up Disable	R/W†	00000000h	NA
4Ch—4Fh	Special—Subsystem Write Capability	R/W	00000000h	00000000h
50h	Capabilities Identifier	R	01h	01h
51h	Next Item Pointer	R	00h	00h

* The revision can be identified electronically using the standard PCI revision ID register described in this table. The revision can also be identified by physical markings using the last letter of the USS2000 identifier code printed on the device. The USS2000 identifier code will be printed using the format USS2000XY, where X will identify the package type (T) and Y will identify the revision.

† This register is normally read only. Write capability of this register is available to system BIOS only.

‡ This register is not used. Read data of all zeros is returned to configuration read command.

8 PCI Register Overview (continued)

Table 8. PCI Bus Configuration Memory Summary (continued)

Configuration Space Offset	Register Name	Read/Write	Default Value (Reset)	
			OHCI	EHCI
52h—53h	Power Management Capabilities	R	7602h	FE02h
54h—55h	Power Management Control Status	R/W	2000h	6000h
56h	Control/Status-Bridge	R	00h	00h
57h	Data	R	32h	c0h
60h	Serial Bus Release Number	R	NA	20h
61h	Frame Length Adjust	R/W	NA	20h
62h—63h	Port Wake Capability	R/W	NA	001Fh
6Ch	Microframe Cache	R/W	NA	01h

9 PCI Configuration Registers—Detailed Definition

The reset/description values are identical for all functions, except where noted otherwise.

Table 9. Vendor ID Register (00h—01h)

This register is fixed as the Agere vendor ID assigned by the PCI SIG.

Bits	Field	Read/Write	Reset/Description
15:0	Vendor ID	R	Assigned 11C1h.

Table 10. Device ID Register (02h—03h)

This register is fixed as the Agere product USS2000.

Bits	Field	Read/Write	Reset/Description
15:0	Device ID	R	Assigned 5804h (function 0, 1, 2, 3). Assigned 5805h (function 4).

Table 11. Command Register (04h—05h)

All read-only bits represent nonconfigurable features of the USS2000.

Bits	Field	Read/Write	Reset/Description
15:10	Reserved	R	000000b
9	Fast Back-to-back Enable	R/W	0
8	SERRN Enable	R/W	0
7	Wait Cycle Control	R	0
6	Parity Error Response	R/W	0
5	VGA Palette Snoop	R	0
4	Memory Write and Invalidate Enable	R/W	0
3	Special Cycles	R	0
2	Bus Master	R/W	0
1	Memory Space	R/W	0
0	IO Space	R/W	0

Table 12. Status Register (06h—07h)

All read-only bits represent nonconfigurable features of the USS2000.

Bits	Field	Read/Write	Reset/Description
15	Detected Parity Error	R/W	0
14	Signaled System Error	R/W	0
13	Received Master Abort	R/W	0
12	Received Target Abort	R/W	0
11	Signaled Target Abort	R/W	0
10:9	DEVSEL Timing	R	01
8	Data Parity Error Detected	R/W	0
7	Fast Back-to-back Capable	R	0
6	UDF Support	R	0
5	66 MHz Capable	R	1
4	Capabilities	R	1
3:0	Reserved	R	0000b

9 PCI Configuration Registers—Detailed Definition (continued)

Table 13. Revision ID Register (08h)

Represents the current revision of the USS2000.

Bits	Field	Read/Write	Reset/Description
7:0	Revision ID*	R	12h

* The revision of the USS2000 can be identified either electronically or by physical markings. The revision can be identified electronically using the standard PCI revision ID register described in this table. The revision can also be identified by physical markings using the last letter of the USS2000 identifier code printed on the device. The USS2000 identifier code will be printed using the format USS2000VY, where Y will identify the revision.

Table 14. Class Code Register (09h—0Bh)

The PCI class code for all OpenHCI host controllers is defined in the OpenHCI specification.

Bits	Field	Read/Write	Reset/Description
23:16	Base Class	R	0Ch = Serial bus controller.
15:8	Subclass	R	03h = Universal serial bus.
7:0	Programming Interface	R	10h OHCI (function 0, 1, 2, 3). 20h EHCI (function 4).

Table 15. Cache Line Size Register (0Ch)

Cache line size is supported by the EHCI (function 4). The OHCIs (functions 0, 1, 2, 3) do not use this register.

Bits	Field	Read/Write	Reset/Description
7:0	Cache Line Size	R/W	10h

Table 16. Latency Timer Register (0Dh)

Controls the number of clock cycles the USS2000 may remain on the PCI bus after becoming bus master.

Bits	Field	Read/Write	Reset/Description
7:0	Latency Timer	R/W	Upper 5 bits are read/write. Lower 3 bits are read only. 40h

Table 17. Header Type Register (0Eh)

The USS2000 supports PCI header type 0 only.

Bits	Field	Read/Write	Reset/Description
7:0	Header Type	R	80h = Multifunction PCI device.

Table 18. BIST Register (0Fh)

BIST is not supported by the USS2000.

Bits	Field	Read/Write	Reset/Description
7:0	BIST	R	00h

9 PCI Configuration Registers—Detailed Definition (continued)

Table 19. Base Address Register 0 (10h—13h)

The base address register is used to specify to the PCI operating system the memory size of the USS2000 device. As recommended by the OpenHCI specification, the lower 12 bits are read only (fixed to logic 0) to indicate 4K (2^{12}) memory size.

Bits	Field	Read/Write	Reset/Description
31:0	BAR 0	R/W	Lower 12 bits are read only. Upper 20 bits are read/write.

Table 20. Base Address Register 1, 2, 3, 4, 5 (14h—17h), (18h—1Bh), (1Ch—1Fh), (20h—23h), (24h—27h)

These base address registers are unused by the USS2000 device.

Bits	Field	Read/Write	Reset/Description
31:0	BAR 1—5	R	00000000h

Table 21. Cardbus CIS Pointer Register (28h—2Bh)

Cardbus CIS pointer not required for the USS2000.

Bits	Field	Read/Write	Reset/Description
31:0	CardBus CIS Pointer	R	00000000h

Table 22. Subsystem Vendor ID Register (2Ch—2Dh)

The subsystem vendor ID is R/W for compliance with *Microsoft* PC98 specifications. On reset, this register is read only. System BIOS may write a 1 to special-subsystem write capability register (4Ch) bit 0 to enable write capability of this register. After configuring this register, the system BIOS must write a 0 to special-subsystem write capability register (4Ch) bit 0 to disable write capability of this register.

Bits	Field	Read/Write	Reset/Description
15:0	Subsystem Vendor ID	R/W	11C1h

Table 23. Subsystem ID Register (2Eh—2Fh)

The subsystem ID is R/W for compliance with *Microsoft* PC98 specifications. On reset, this register is read only. System BIOS may write a 1 to special-subsystem write capability register (4Ch) bit 0 to enable write capability of this register. After configuring this register, the system BIOS must write a 0 to special-subsystem write capability register (4Ch) bit 0 to disable write capability of this register.

Bits	Field	Read/Write	Reset/Description
15:0	Subsystem ID	R/W	5804h (function 0, 1, 2, 3). 5805h (function 4).

Table 24. Expansion ROM Base Address Register (30h—33h)

Expansion ROM not supported by the USS2000.

Bits	Field	Read/Write	Reset/Description
31:0	Expansion ROM Base Address	R	00000000h

9 PCI Configuration Registers—Detailed Definition (continued)

Table 25. Capabilities Pointer Register (34h)

The USS2000 has additional capabilities.

Bits	Field	Read/Write	Reset/Description
7:0	Cap_Ptr	R	50h

Table 26. Interrupt Line Register (3Ch)

This register is used to communicate interrupt line routing information.

Bits	Field	Read/Write	Reset/Description
7:0	Interrupt Line	R/W	00h

Table 27. Interrupt Pin Register (3Dh)

When input pin TEST0 = 0b (low), all functions share interrupt A. When input pin TEST0 = 1b (high), functions 0 and 1 use interrupt A, functions 2 and 3 use interrupt B, function 4 uses interrupt C.

Bits	Field	Read/Write	Reset/Description
7:0	Interrupt Pin	R	TEST0 = 0b: 01h. TEST0 = 1b: 01h (function 0,1). : 02h (function 2, 3). : 03h (function 4).

Table 28. Min_Gnt Register (3Eh)

This register specifies how long of a burst period the USS2000 function needs. (Expressed in 250 ns increments.)

Bits	Field	Read/Write	Reset/Description
7:0	Min_Gnt	R	03h OHCI (function 0, 1, 2, 3). 10h EHCI (function 4).

Table 29. Max_Lat Register (3Fh)

This register specifics how often the USS2000 function needs to gain access to the PCI bus. (Expressed in 250 ns increments.)

Bits	Field	Read/Write	Reset/Description
7:0	Max_Lat	R	56h OHCI (function 0, 1, 2, 3). 20h EHCI (function 4).

9 PCI Configuration Registers—Detailed Definition (continued)

9.1 Wake-Up Enable Register (40h) (Only OHCI Uses This Register)

This is a USS2000 unique register used to allow software control of which wake-up events are permitted to trigger PCI power management system wake-up (PMEN assertion). These bits default to 0 and are only writable when the special-vendor write bit is active. System BIOS may write a 1 to special-subsystem write capability register (4C) bit 0 to enable write capability of this register.

Table 30. Wake-Up Enable Register

Bits	Field	Read/Write	Reset/Description
31:3	Reserved	R	00000000h
2	Wake on Overcurrent Enable	R/W	0b 0 = Wake on overcurrent enable. 1 = Wake on overcurrent disable.
1	Wake on Disconnect Enable	R/W	0b 0 = Wake on disconnect enable. 1 = Wake on disconnect disable.
0	Wake on Connect Enable	R/W	0b 0 = Wake on connect enable. 1 = Wake on connect disable.

9.2 Special-Subsystem Write Capability Register (4Ch)

This is a special register implemented for compliance with *Microsoft* PC98 specification, chapter 9, item 11. Bit 0 is read/write to allow the system BIOS to enable write capability of subsystem vendor ID; subsystem ID registers; and the wake-up enable register.

Table 31. Special-Vendor Write Capability Register

Bits	Field	Read/Write	Reset/Description
31:1	Reserved	R	00000000h
0	Special-Vendor Write	R/W	0b 0 = Special-vendor write disabled. 1 = Special-vendor write enabled.

9 PCI Configuration Registers—Detailed Definition (continued)

9.3 Capabilities Identifier (Cap_ID) Register (50h)

Table 32. Capabilities Identifier (Cap_ID) Register

Bits	Default Value		Read/Write	Name/Description
	OHCI	EHCI		
7:0		01h	R	This capability is for the PCI power management data structure.

9.4 Next Item Pointer Register (51h)

Table 33. Next Item Pointer Register

Bits	Default Value		Read/Write	Name/Description
	OHCI	EHCI		
7:0		00h	R	No other PCI capabilities are implemented.

9 PCI Configuration Registers—Detailed Definition (continued)

9.5 Power Management Capabilities Register (52h—53h)

Table 34. Power Management Capabilities Register

Bits	Default Value		Read/Write	Name/Description
	OHCI	EHCI		
15:11		01111b	R	**PME_Support.** Specifies the states in which the PME signal can be asserted: XXXX1b—PME can be asserted in D0 state. XXX1Xb—PME can be asserted in D1 state. XX1XXb—PME can be asserted in D2 state. X1XXXb—PME can be asserted in $D3_{hot}$ state. 0XXXXb—PME cannot be asserted in $D3_{cold}$ state.
10		1b	R	**D2_Support.** This device supports the D2 power management state.
9		1b	R	**D1_Support.** This device supports the D1 power management state.
8:6		000b	R	**Aux_Current.** D3 cold state is not supported by this function. Therefore, this register is not applicable and returns 000b.
5		0b	R	**DSI.** No device-specific initialization sequence is required before using this device.
4		0b	R	**Reserved.**
3		0b	R	**PME Clock.** No clocks are required for this device to issue PMEN.
2:0		010b	R	**Version.** *PCI Power Management Interface Specification* Revision 1.1 compliant.

9.6 Power Management Control/Status Register (54h—55h)

Table 35. Power Management Control/Status Register

Bits	Default Value		Read/Write	Name/Description
	OHCI	EHCI		
15		0b	Read/Write-Clear	**PME_Status.** This bit is set when the function would normally assert the PMEN signal independent of the state of the PME_En bit. Writing a 1b to this bit will clear the PME_Status bit and force the function to stop asserting PMEN.
14:13		See Table 38	R	**Data Scale.** Variable based upon data select. See Table 38.
12:9		0000b	R/W	**Data_Select.** The system uses this register to select the appropriate data for reporting in the data scale register and data register.
8		0b	R/W	**PME_En**. When active (1b), the function is enabled to assert PMEN.
7:2		000000b	R	**Reserved.**
1:0		00b	R/W	**Power_State.** Represents the current power state of the function.

9 PCI Configuration Registers—Detailed Definition (continued)

9.7 Power Management Control/Status Bridge (56h)

Table 36. Power Management Control/Status Bridge

Bits	Default Value		Read/ Write	Name/Description
	OHCI	EHCI		
7		0b	R	**BPCC_En (Bus Power/Clock Control Enable).** This is not a PCI bridge function.
6		0b	R	**B2_B3# (B2/B3 Support for D3hot).** This is not a PCI bridge function.
5:0		000000b	R	**Reserved.**

9.8 Power Management Data Register (57h)

Table 37. Power Management Data Register

Bits	Default Value		Read/ Write	Name/Description
	OHCI	EHCI		
7:0		See Table 38	R	Represents the amount of power dissipated or consumed in various power management states. Variable based upon data select. See Table 38.

9.9 Power Consumption/Dissipation Reporting

Table 38. Power Consumption/Dissipation Reporting

Value In Data Select	Data Reported	Data	Data Scale	Units (Interpreting Data Scale)
0000b	D0 power consumed	coh	11b	mW
0001b	D1 power consumed	coh	11b	mW
0010b	D2 power consumed	10h	11b	mW
0011b	D3 power consumed	07h	11b	mW
0100b	D0 power dissipated	coh	11b	mW
0101b	D1 power dissipated	coh	11b	mW
0110b	D2 power dissipated	10h	11b	mW
0111b	D3 power dissipated	07h	11b	mW
1000b—1111b	Reserved (single-function PCI device configuration)	00000000b	00b	NA

9.10 Serial Bus Release Number (60h) (Only EHCI Uses This Register)

Read only register as defined in the EHCI specification.

Table 39. Serial Bus Release Number

Bits	Field	Read/Write	Reset/Description
7:0	SBRN	R	20h.

9 PCI Configuration Registers—Detailed Definition (continued)

9.11 Frame Length Adjust Register (61h) (Only EHCI Uses This Register)

See the EHCI specification for details on this register.

Table 40. Frame Length Adjust Register

Bits	Field	Read/Write	Reset/Description
7:6	Reserved	R	00b.
5:0	FLADJ	R/W	20h.

9.12 Port Wake Capability (62h) (Only EHCI Uses This Register)

This register is implemented by the EHCI host controller. Therefore, bit position 0 is set. In addition, each of the four downstream ports can be enabled as a wake-up port. Therefore, bits 1 through 4 are also set.

Table 41. Port Wake Capability

Bits	Field	Read/Write	Reset/Description
15:0	PORTWAKECAP	R/W	001Fh.

9.13 Microframe Cache (6Ch) (Only EHCI Uses This Register) Vendor Specific

The value read back in the EHCI register HCCPARAMS bits 7:4 (isochronous scheduling threshold) is determined by this bit. The default (bit 0 = 0) is for frame caching; HCCPARAMS 7:4 = 1000b. When microframe cache is selected (bit 0 = 1), HCCPARAMS 7:4 = 0001b.

Table 42. Microframe Cache

Bits	Field	Read/Write	Reset/Description
31:1	Reserved	R	00000000h.
0	Microframe cache	R/W	0b. 0 = Frame cache (default). 1 = Microframe cache.

10 OHCI Registers

Table 43. OHCI USB Operational Registers Summary

Each OHCI PCI function has one set of USB operational registers available through the memory-mapped base address register 0. Each set of USB operational registers represents one single-port OHCI USB host controller. Refer to Tables 41—62 for more details on each of these registers.

Offset	Register Name
00h	HcRevision
04h	HcControl
08h	HcCommandStatus
0Ch	HcInterruptStatus
10h	HcInterruptEnable
14h	HcInterruptDisable
18h	HcHCCA
1Ch	HcPeriodCurrentED
20h	HcControlHeadED
24h	HcControlCurrentED
28h	HcBulkHeadED
2Ch	HcBulkCurrentED
30h	HcDoneHead
34h	HcFmInterval
38h	HcFmRemaining
3Ch	HcFmNumber
40h	HcPeriodicStart
44h	HcLSThreshold
48h	HcRhDescriptorA
4Ch	HcRhDescriptorB
50h	HcRhStatus
54h	HcRhPortStatus1
100h	HceControl
104h	HceInput
108h	HceOutput
10Ch	HceStatus

Table 44. HcRevision Register (00h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
8	Legacy (L)	1b	R	R
7:0	Revision (REV)	10h	R	R

10 OHCI Registers (continued)

Table 45. HcControl Register (04h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
10	Remote Wake-up Enable (RWE)	0b	R/W	R
9	Remote Wake-up Connected (WC)	0b	R/W	R/W
8	Interrupt Routing (IR)	0b	R/W	R
7:6	Host Controller Functional State (HCFS): 00b: UsbReset 01b: UsbResume 10b: UsbOperational 11b: UsbSuspend	00b	R/W	R/W
5	Bulk List Enable (BLE)	0b	R/W	R
4	Control List Enable (CLE)	0b	R/W	R
3	Isochronous Enable (IE)	0b	R/W	R
2	Periodic List Enable (PLE)	0b	R/W	R
1:0	Control Bulk Service Ratio (CBSR)	00b	R/W	R

Table 46. HcCommandStatus Register (08h)

Bits	Field	Reset	HCD	HC
17:16	Scheduling Overrun Count (SOC)	0b	R	R/W
3	Ownership Change Request (OCR)	0b	R/W	R/W
2	Bulk List Filled (BLF)	0b	R/W	R/W
1	Control List Filled (CLF)	0b	R/W	R/W
0	Host Controller Reset (HCR)	0b	R/W	R/W

Table 47. HcInterruptStatus Register (0Ch)

Bits	Field	Reset	HCD	HC
30	Ownership Change (OC)	0b	R/W	R/W
6	Root Hub Status Change (RHSC)	0b	R/W	R/W
5	Frame Number Overflow (FNO)	0b	R/W	R/W
4	Unrecoverable Error (UE)	0b	R/W	R/W
3	Resume Detected (RD)	0b	R/W	R/W
2	Start of Frame (SF)	0b	R/W	R/W
1	Writeback Done Head (WDH)	0b	R/W	R/W
0	Scheduling Overrun (SO)	0b	R/W	R/W

10 OHCI Registers (continued)

Table 48. HcInterruptEnable Register (10h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Master Interrupt Enable (MIE): 0—Ignored by HC 1—Enables interrupt generation due to events specified in the other bits of this register	0b	R/W	R
30	Ownership Change (OC): 0—Ignore 1—Enable interrupt	0b	R/W	R
6	Root Hub Status Change (RHSC): 0—Ignore 1—Enable interrupt	0b	R/W	R
5	Frame Number Overflow (FNO): 0—Ignore 1—Enable interrupt	0b	R/W	R
4	Unrecoverable Error (UE): 0—Ignore 1—Enable interrupt	0b	R/W	R
3	Resume Detected (RD): 0—Ignore 1—Enable interrupt	0b	R/W	R
2	Start of Frame (SF): 0—Ignore 1—Enable interrupt	0b	R/W	R
1	Writeback Done Head (WDH): 0—Ignore 1—Enable interrupt	0b	R/W	R
0	Scheduling Overrun (SO): 0—Ignore 1—Enable interrupt	0b	R/W	R

10 OHCI Registers (continued)

Table 49. HcInterruptDisable Register (14h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Master Interrupt Enable (MIE): 0—Ignored by HC 1—Disables interrupt generation due to events specified in the other bits of this register	0b	R/W	R
30	Ownership Change (OC): 0—Ignore 1—Disable interrupt	0b	R/W	R
6	Root Hub Status Change (RHSC): 0—Ignore 1—Disable interrupt	0b	R/W	R
5	Frame Number Overflow (FNO): 0—Ignore 1—Disable interrupt	0b	R/W	R
4	Unrecoverable Error (UE): 0—Ignore 1—Disable interrupt	0b	R/W	R
3	Resume Detected (RD): 0—Ignore 1—Disable interrupt	0b	R/W	R
2	Start of Frame (SF): 0—Ignore 1—Disable interrupt	0b	R/W	R
1	Writeback Done Head (WDH): 0—Ignore 1—Disable interrupt	0b	R/W	R
0	Scheduling Overrun (SO): 0—Ignore 1—Disable interrupt generation	0b	R/W	R

10 OHCI Registers (continued)

Table 50. HcHCCA Register (18h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:8	Host Controller Communications Area (HCCA) Base Address: Bits 7:0 will always return a 0.	0h	R/W	R

Table 51. HcPeriodCurrentED Register (1Ch)

Bits	Field	Reset	HCD	HC
31:4	Period Current ED (PCED) Base Address: Bits 3:0 will always return a 0.	0h	R/W	R

Table 52. HcControlHeadED Register (20h)

Bits	Field	Reset	HCD	HC
31:4	Control Head ED (CHED) Base Address: Bits 3:0 will always return a 0.	0h	R/W	R

Table 53. HcControlCurrentED Register (24h)

Bits	Field	Reset	HCD	HC
31:4	Control Current ED (CCED) Base Address: Bits 3:0 will always return a 0.	0h	R/W	R/W

Table 54. HcBulkHeadED Register (28h)

Bits	Field	Reset	HCD	HC
31:4	Bulk Head ED (BHED) Base Address: Bits 3:0 will always return a 0.	0h	R/W	R

Table 55. HcBulkCurrentED Register (2Ch)

Bits	Field	Reset	HCD	HC
31:4	Bulk Current ED (BCED) Base Address: Bits 3:0 will always return a 0.	0h	R/W	R/W

Table 56. HcDoneHead Register (30h)

Bits	Field	Reset	HCD	HC
31:4	Done Head ED (DH) Base Address: Bits 3:0 will always return a 0.	0h	R	R/W

10 OHCI Registers (continued)

Table 57. HcFmInterval Register (34h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Frame Interval Toggle (FIT)	0b	R/W	R
30:16	FS Largest Data Packet (FSMPS)	0h	R/W	R
13:0	Frame Interval (FI)	2EDFh	R/W	R

Table 58. HcFmRemaining Register (38h)

Bits	Field	Reset	HCD	HC
31	Frame Remaining Toggle (FRT)	0b	R	R/W
13:0	Frame Remaining (FR)	0h	R	R/W

Table 59. HcFmNumber Register (3Ch)

Bits	Field	Reset	HCD	HC
15:0	Frame Number (FN)	0h	R	R/W

Table 60. HcPeriodicStart Register (40h)

Bits	Field	Reset	HCD	HC
13:0	Periodic Start (PS)	0h	R/W	R

Table 61. HcLSThreshold (44h)

Bits	Field	Reset	HCD	HC
11:0	LS Threshold	628h	R/W	R

Table 62. HcRhDescriptorA Register (48h)

Bits	Field	Reset	HCD	HC
31:24	Power On to Power Good Time (POTPGT)	10h	R/W	R
12	No Overcurrent Protection (NOCP)	0b	R/W	R
11	Overcurrent Protection Mode (OCPM)	1b	R/W	R
10	Device Type (DT)	0b	R	R
9	No Power Switching (NPS)	0b	R/W	R
8	Power Switching Mode (PSM)	1b	R/W	R
7:0	Number Downstream Ports (NDP)	01h	R	R

10 OHCI Registers (continued)

Table 63. HcRhDescriptorB Register (4Ch)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:16	Port Power Control Mask (PPCM)	0002h	R/W	R
15:0	Device Removable (DR)	0000h	R/W	R

Table 64. HcRhStatus Register (50h)

Bits	Field	Reset	HCD	HC
31	Clear Remote Wake-up Enable (CRWE)	0b	W	R
17	Overcurrent Indicator Change (OCIC)	0b	R/W	R/W
16	Local Power Status Change (LPSC)	0b	R/W	R
15	Device Remote Wake-up Enable (DRWE)	0b	R/W	R
1	Overcurrent Indicator (OCI)	0b	R	R/W
0	Local Power Status (LPS)	0b	R/W	R

Table 65. HcRhPortStatus1 Register (54h)

Bits	Field	Reset	HCD	HC
20	Port Reset Status Change (PRSC)	0b	R/W	R/W
19	Port Overcurrent Indicator Change (OCIC)	0b	R/W	R/W
18	Port Suspend Status Change (PSSC)	0b	R/W	R/W
17	Port Enable Status Change (PESC)	0b	R/W	R/W
16	Connect Status Change (CSC)	0b	R/W	R/W
9	Low-speed Device Attached (LSDA)	0b	R/W	R/W
8	Port Power Status (PPS)	0b	R/W	R/W
4	Port Reset Status (PRS)	0b	R/W	R/W
3	Port Overcurrent Indicator (POCI)	0b	R/W	R/W
2	Port Suspend Status (PSS)	0b	R/W	R/W
1	Port Enable Status (PES)	0b	R/W	R/W
0	Current Connect Status (CCS)	0b	R/W	R/W

11 Legacy Support Registers

The legacy support function and all registers described in this section are available on all four embedded USB host controllers. Four operational registers are used to provide the legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the respective host controller core operational registers with HceControl located at offset 100h.

Table 66. Legacy Support Registers

Offset	Register	Description
100h	HceControl	Used to enable and control the emulation hardware and report various status information.
104h	HceInput	Emulation side of the legacy input buffer register.
108h	HceOutput	Emulation side of the legacy output buffer register where keyboard and mouse data is to be written by software.
10Ch	HceStatus	Emulation side of the legacy status register.

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table 67.

Table 67. Emulated Registers

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0.
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

11.1 HceInput Register

Table 68. HceInput Register (104h)

Bit	Field	R/W	Description
31:8	Reserved	—	—
7:0	InputData	R/W	This register holds data that is written to I/O ports 60h and 64h.

I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the host controller’s operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

11 Legacy Support Registers (continued)

11.2 HceOutput Register

Table 69. HceOutput Register (108h)

Bit	Field	R/W	Description
31:8	Reserved	—	—
7:0	OutputData	R/W	This register hosts data that is returned when an I/O read of port 60h is performed by application software.

The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

11.3 HceStatus Register

Table 70. HceStatus Register (10Ch)

Bit	Field	R/W	Description
31:8	Reserved	—	—
7	Parity	R/W	Indicates parity error on keyboard/mouse data.
6	Time-out	R/W	Used to indicate a time-out.
5	AuxOutputFull	R/W	IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
4	Inhibit Switch	R/W	This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is not inhibited.
3	CmdData	R/W	The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h.
2	Flag	R/W	Nominally used as a system flag by software to indicate a warm or cold boot.
1	InputFull	R/W	Except for the case of a GateA20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0	OutputFull	R/W	The HC sets this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.

The contents of the HceStatus register are returned on an I/O read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the host controller’s operational register space. Accessing this register through its memory address produces no side effects.

11 Legacy Support Registers (continued)

11.4 HceControl Register

Table 71. HceControl Register (100h)

Bit	Field	Reset	R/W	Description
31:9	Reserved	—	—	Must read as zeros.
8	A20State	0b	R/W	Indicates current state of gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.
7	IRQ12Active	0b	R/W	Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
6	IRQ1Active	0b	R/W	Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
5	GateA20Sequence	0b	R/W	Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
4	ExternalIRQEn	0b	R/W	When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
3	IRQEn	0b	R/W	When set, the HC generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
2	CharacterPending	0b	R/W	When set, an emulation interrupt is generated when the OutputFull bit of the HceStatus register is set to 0.
1	EmulationInterrupt	—	R	This bit is a static decode of the emulation interrupt condition.
0	EmulationEnable	0b	R/W	When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.

12 EHCI Capability Registers

These registers specify the limits, restrictions, and capabilities of the host controller implementation.

Table 72. Enhanced Host Controller Capability Registers

Offset	Size	Mnemonic	Register Name
00h	1	CAPLENGTH	Capability Register Length
01h	1	Reserved	NA
02h	2	HCIVERSION	Interface Version Number
04h	4	HCSPARAMS	Structural Parameters
08h	4	HCCPARAMS	Capability Parameters
0Ch	8	HCSP-PORTROUTE	Companion Port Route Description

12.1 CAPLENGTH—Capability Registers Length

Address: Base+ (00h)
Default Value: 20h
Attribute: R
Size: 8 bits

This register is used as an offset to add to register base to find the beginning of the operational register space.

12.2 HCIVERSION—Host Controller Interface Version Number

Address: Base+ (02h)
Default Value: 0100h
Attribute: R
Size: 16 bits

This is a 2-byte register containing a BCD encoding of the version number of interface to which this host controller interface conforms.

12.3 HCSPARAMS—Structural Parameters

Address: Base+ (04h)
Default Value: 00004114h
Attribute: R
Size: 32 bits

This is a set of fields that are structural parameters: number of downstream ports, etc.

12 EHCI Capability Registers (continued)

Table 73. HCSPARAMS—Host Controller Structural Parameters

Bit	Description
31:24	**Reserved.** These bits are reserved and should be set to 0.
23:20	**Debug Port Number.** This optional feature is not supported.
19:17	**Reserved.** These bits are reserved and will return 0.
16	**Port Indicators (P_INDICATOR).** The USS2000 does not support port indicator control.
15:12	**Number of Companion Controller (N_CC).** This field indicates the number of companion controllers associated with this EHCI host controller. This field indicates that the USS2000 contains four companion OHCI host controller(s). Port-ownership hand-offs are supported. High-speed, full-speed, and low-speed devices are supported on the host controller root ports.
11:8	**Number of Ports per Companion Controller (N_PCC).** This field indicates the number of ports supported per companion host controller (one per port). It is used to indicate the port routing configuration to system software.
7	**Port Routing Rules.** This field indicates the method used by the USS2000 for how all ports are mapped to companion controllers. The value of this field (0) indicates that the USS2000 maps each port to the corresponding companion host controller, as follows: Port 1 is mapped to companion controller 0 (function 0). Port 2 is mapped to companion controller 1 (function 1). Port 3 is mapped to companion controller 2 (function 2). Port 4 is mapped to companion controller 3 (function 3). The USS2000 does not use explicit mapping with the HCSP-PORTROUTE array.
6:5	**Reserved.** These bits are reserved and will return 0.
4	**Port Power Control (PPC).** This field indicates that the USS2000 includes port power control and the ports have port power switches. The value of this field affects the functionality of the port power field in each port status and control register (see Table 83).
3:0	**N_PORTS.** This field specifies the number of physical downstream ports implemented by the USS2000 (4). The value of this field determines how many port registers are addressable in the operational register space (see Table 75).

12 EHCI Capability Registers (continued)

12.4 HCCPARAMS Capability Parameters

Address: Base+ (08h)
Default Value: 00000082h
Attribute: R
Size: 32 bits

Multiple mode control (time-base bit functionality), addressing capability.

Table 74. HCCPARAMS—Host Controller Capability Parameters

Bit	Description
31:8	**Reserved.** These bits are reserved and will return 0.
7:4	**Isochronous Scheduling Threshold.** Default = 1000b. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. Bit [7] is a 1, indicating the USS2000 caches an isochronous data structure for an entire frame. (See Microframe Cache bit description on page 27.)
3:2	**Reserved.** These bits are reserved and will return 0.
1	**Programmable Frame List Flag.** Default = 1b. Set to a 1 indicating that the system software can specify and use a smaller frame list and configure the host controller via the USBCMD register frame list size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	**64-bit Addressing Capability.** Default = 0b. This field documents the addressing range capability of the USS2000, and indicates that data structures use 32-bit address memory pointers.

12.4.1 HCSP-PORTROUTE—Companion Port Route Description

Address: Base+ (0Ch)
Default Value: 00000000 0000000h
Attribute: R
Size: 60 bits

This optional field is not used by the USS2000, since the port routing rules field in the HCSPARAMS register is set to a 0.

13 EHCI Operational Registers

This section defines the enhanced host controller operational registers. These registers are located after the capabilities registers. The operational register base is DWord aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the enhanced host controller register address space. All registers are 32 bits in length. Software should read and write these registers using only DWord accesses.

Table 75. Host Controller Operational Registers

Offset	Mnemonic	Register Name
00h	USBCMD	USB Command
04h	USBSTS	USB Status
08h	USBINTR	USB Interrupt Enable
0Ch	FRINDEX	USB Frame Index
10h	CTRLDSSEGMENT	4G Segment Selector (not supported)
14h	PERIODICLISTBASE	Frame List Base Address
18h	ASYNCLISTADDR	Next Asynchronous List Address
1C—3Fh	Reserved	—
40h	CONFIGFLAG	Configured Flag Register
44h	PORTSC1	Port Status/Control—Port 1
48h	PORTSC2	Port Status/Control—Port 2
4Ch	PORTSC3	Port Status/Control—Port 3
50h	PORTSC4	Port Status/Control—Port 4

13.1 USBCMD—USB Command Register

Address: Operational Base+ (00h)
Default Value: 00080000h
Attribute: R, R/W (field dependent), WO
Size: 32 bits

The command register indicates the command to be executed by the serial bus enhanced host controller. Writing to the register causes a command to be executed.

13 EHCI Operational Registers (continued)

Table 76. USBCMD—USB Command Register Bit Definitions

Bit	Description
31:24	**Reserved.** These bits are reserved and will return 0.
23:16	**Interrupt Threshold Control**—**R/W.** Default 08h. This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. **Value** **Maximum Interrupt Interval** 00h Reserved 01h 1 microframe 02h 2 microframes 04h 4 microframes 08h 8 microframes (default, equates to 1 ms) 10h 16 microframes (2 ms) 20h 32 microframes (4 ms) 40h 64 microframes (8 ms) Software modifications to this bit while HCHalted bit is equal to 0 results in undefined behavior.
15:8	**Reserved.** These bits are reserved and will return 0.
7	**Light Host Controller Reset**—**R/W.** This optional feature is supported by the USS2000. It allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers. For example, the PORTSC registers are not reset to their default values and the CF bit setting does not go to 0 (retaining port ownership relationships). A host software read of this bit as 0 indicates the light host controller reset has completed and it is safe for host software to reinitialize the host controller. A host software read of this bit as a 1 indicates the light host controller reset has not yet completed.
6	**Interrupt on Async Advance Doorbell**—**R/W.** This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the interrupt on async advance status bit in the USBSTS register. If the interrupt on async advance enable bit in the USBINTR register is a 1, then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a 0 after it has set the interrupt on async advance status bit in the USBSTS register to a 1. Software should not write a 1 to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.
5	**Asynchronous Schedule Enable**—**R/W.** Default 0b. This bit controls whether the host controller skips processing the asynchronous schedule. Values mean: 0b Do not process the asynchronous schedule. 1b Use the ASYNCLISTADDR register to access the asynchronous schedule.

13 EHCI Operational Registers (continued)

Table 76. USBCMD—USB Command Register Bit Definitions (continued)

Bit	Description
4	**Periodic Schedule Enable—R/W.** Default 0b. This bit controls whether the host controller skips processing the periodic schedule. Values mean: 0b Do not process the periodic schedule. 1b Use the PERIODICLISTBASE register to access the periodic schedule.
3:2	**Frame List Size**—**R/W.** Default 00b. This field is R/W since the programmable frame list flag in the HCCPARAMS registers is set to a 1. This field specifies the size of the frame list. The size of the frame list controls which bits in the frame index register should be used for the frame list current index. Values mean: 00b 1024 elements (4096 bytes) default value. 01b 512 elements (2048 bytes). 10b 256 elements (1024 bytes)—for resource-constrained environments. 11b Reserved.
1	**Host Controller Reset (HCRESET)**—**R/W.** This control bit is used by software to reset the host controller. The effects of this on root hub registers are similar to a chip hardware reset. When software writes a 1 to this bit, the host controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register. Software should not set this bit to a 1 when the HCHalted bit in the USBSTS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior.
0	**Run/Stop (RS)**—**R/W.** Default 0b. 1 = run. 0 = stop. When set to a 1, the host controller proceeds with execution of the schedule. The host controller continues execution as long as this bit is set to a 1. When this bit is set to 0, the host controller completes the current and any actively pipelined transactions on the USB and then halts. The host controller will halt within 16 microframes after software clears the run bit. The HCHalted bit in the status register indicates when the host controller has finished its pending pipelined transactions and has entered the stopped state. Software should not write a 1 to this field unless the host controller is in the halted state (i.e., HCHalted in the USBSTS register is a 1).

13 EHCI Operational Registers (continued)

13.2 USBSTS—USB Status Register

Address: Operational Base + (04h)
Default Value: 00001000h
Attribute: R, R/W, R/WC, (field dependent)
Size: 32 bits

This register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to 0 in this register by writing a 1 to it.

Table 77. USBSTS USB Status Register Bit Definitions

Bit	Description
31:16	**Reserved**. These bits are reserved and will return 0.
15	**Asynchronous Schedule Status**—**R.** 0 = default. The bit reports the current real status of the asynchronous schedule. If this bit is a 0, then the status of the asynchronous schedule is disabled. If this bit is a 1, then the status of the asynchronous schedule is enabled. The host controller does not immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the USBCMD register. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0).
14	**Periodic Schedule Status**—**R.** 0 = default. The bit reports the current real status of the periodic schedule. If this bit is a 0, then the status of the periodic schedule is disabled. If this bit is a 1, then the status of the periodic schedule is enabled. The host controller does not immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the USBCMD register. When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0).
13	**Reclamation—R.** 0 = default. This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	**HCHalted**—**R.** 1 = default. This bit is a 0 whenever the run/stop bit is a 1. The host controller sets this bit to 1 after it has stopped executing as a result of the run/stop bit being set to 0, either by software or by the host controller hardware (e.g., internal error).
11:6	**Reserved**. These bits are reserved and will return 0.
5	**Interrupt on Async Advance**—**R/WC.** 0 = default. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the interrupt on asynchronous advance doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	**Host System Error**—**R/WC.** The host controller sets this bit to 1 when a serious error occurs during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI parity error, PCI master abort, and PCI target abort. When this error occurs, the host controller clears the run/stop bit in the command register to prevent further execution of the scheduled TDs.
3	**Frame List Rollover**—**R/WC.** The host controller sets this bit to a 1 when the frame list index rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the frame list size field of the USBCMD register) is 1024, the frame index register rolls over every time FRINDEX[13] toggles. Similarly, if the size is 512, the host controller sets this bit to a 1 every time FRINDEX[12] toggles.

13 EHCI Operational Registers (continued)

Table 77. USBSTS USB Status Register Bit Definitions (continued)

Bit	Description
2	**Port Change Detect—R/WC.** The host controller sets this bit to a 1 when any port for which the port owner bit is set to 0 (see Table 83) has a change bit transition from a 0 to a 1 or a force port resume bit transition from a 0 to a 1 as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the connect status change being set to a 1 after system software has relinquished ownership of a connected port by writing a 0 to a port's port owner bit. On a D3-to-D0 transition of the USS2000 device, this bit is loaded with the OR of all of the PORTSC change bits (including force port resume, overcurrent change, enable/disable change, and connect status change).
1	**USB Error Interrupt (USBERRINT)—R/WC.** The host controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set.
0	**USB Interrupt (USBINT)—R/WC.** The host controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a transfer descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

13.3 USBINTR—USB Interrupt Enable Register

Address: Operational Base + (08h)
Default Value: 00000000h
Attributes: R/W
Size: 32 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USBSTS to allow the software to poll for events.

13 EHCI Operational Registers (continued)

Table 78. USBINTR—USB Interrupt Enable Register

Bit	Interrupt Source	Description
31:6	Reserved	These bits are reserved and will return 0.
5	Interrupt on Async Advance Enable	When this bit is a 1, and the interrupt on async advance bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the interrupt on async advance bit.
4	Host System Error Enable	When this bit is a 1, and the host system error status bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the host system error bit.
3	Frame List Rollover Enable	When this bit is a 1, and the frame list rollover bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the frame list rollover bit.
2	Port Change Interrupt Enable	When this bit is a 1, and the port change detect bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the port change detect bit.
1	USB Error Interrupt Enable	When this bit is a 1, and the USBERRINT bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	USB Interrupt Enable	When this bit is a 1, and the USBINT bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

Note: For all enable register bits, 1 = enabled, 0 = disabled.

13.4 FRINDEX—Frame Index Register

Address: Operational Base + (0Ch)
Default Value: 00000000h
Attribute: R/W (Writes must be DWord Writes)
Size 32 Bits

This register is used by the host controller to index into the periodic frame list. The register updates every 125 μs (once each microframe).

13 EHCI Operational Registers (continued)

Table 79. FRINDEX—Frame Index Register

Bit	Description
31:14	**Reserved.**
13:0	**Frame Index.** The value in this register increments at the end of each time frame (e.g., micro-frame). Bits [N:3] are used for the frame list current index. This means that each location of the frame list is accessed eight times (frames or microframes) before moving to the next index. The following illustrates values of N based on the value of the frame list size field in the USBCMD register. **USBCMD[Frame List Size]** — **Number Elements** — **N** 00b — (1024) — 12 01b — (512) — 11 10b — (256) — 10 11b — Reserved

13.5 CTRLDSSEGMENT—Control Data Structure Segment Register

Address: Operational Base + (10h)
Default Value: 00000000h
Attribute: R/W (Writes must be DWord Writes)
Size: 32 bits

This register is not used.

13 EHCI Operational Registers (continued)

13.6 PERIODICLISTBASE—Periodic Frame List Base Address Register

Address: Operational Base + (14h)
Default Value: 00000000h
Attribute: R/W (Writes must be DWord Writes)
Size: 32 bits

This 32-bit register contains the beginning address of the periodic frame list in the system memory.

Table 80. PERIODICLISTBASE—Periodic Frame List Base Address Register

Bit	Description
31:12	**Base Address (Low).** These bits correspond to memory address signals [31:12], respectively.
11:0	**Reserved.** Must be written as zeros. During run time, the values of these bits are undefined.

13.7 ASYNCLISTADDR—Current Asynchronous List Address Register

Address: Operational Base + (18h)
Default Value: 00000000h
Attribute: Read/Write (Writes must be DWord Writes)
Size: 32 bits

This 32-bit register contains the address of the next asynchronous queue head to be executed.

Table 81. ASYNCLISTADDR—Current Asynchronous List Address Register

Bit	Description
31:5	**Link Pointer Low (LPL).** These bits correspond to memory address signals [31:5], respectively. This field may only reference a queue head (QH).
4:0	**Reserved.** These bits are reserved, and their value has no effect on operation.

13 EHCI Operational Registers (continued)

13.8 CONFIGFLAG—Configure Flag Register

Address: Operational Base+ (40h)
Default Value: 00000000h
Attribute R/W
Size 32 bits

It is only reset by hardware when the power is initially applied or in response to a host controller reset.

Table 82. CONFIGFLAG—Configure Flag Register Bit Definitions

Bit	Description
31:1	**Reserved.** These bits are reserved and should be set to 0.
0	**Configure Flag (CF)**—**R/W.** Default 0b. Host software sets this bit as the last action in its process of configuring the host controller. This bit controls the default port-routing control logic. Bit values and side effects are listed below: 0b Port-routing control logic default-routes each port to its OHCI host controller. 1b Port-routing control logic default-routes all ports to this host controller.

13.9 PORTSC—Port Status and Control Registers

Address: Operational Base + (44h, 48h, 4Ch, 50h)
Default: 00002000h
Attribute: R, R/W, R/WC (field dependent)
Size 32 bits

There are four registers implemented in the USS2000, one for each port.

13 EHCI Operational Registers (continued)

Table 83. PORTSC—Port Status and Control

Bit	Description
31:23	**Reserved.** These bits are reserved for future use and return a value of 0 when read.
22	**Wake on Overcurrent Enable (WKOC_E)—R/W.** Default = 0b. Writing this bit to a 1 enables the port to be sensitive to overcurrent conditions as wake-up events. This field is 0 if port power is 0.
21	**Wake on Disconnect Enable (WKDSCNNT_E)—R/W.** Default = 0b. Writing this bit to a 1 enables the port to be sensitive to device disconnects as wake-up events. This field is 0 if port power is 0.
20	**Wake on Connect Enable (WKCNNT_E)—R/W.** Default = 0b. Writing this bit to a 1 enables the port to be sensitive to device connects as wake-up events. This field is 0 if port power is 0.
19:16	**Port Test Control—R/W.** Default = 0000b. When this field is 0, the port is not operating in a test mode. A nonzero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b—1111b are reserved): **Bits — Test Mode** 0000b — Test Mode Not Enabled. 0001b — Test J_STATE. 0010b — Test K_STATE. 0011b — Test SE0_NAK. 0100b — Test Packet. 0101b — Test FORCE_ENABLE.
15:14	**Port Indicator Control.** Default = 0b. This feature is not supported.
13	**Port Owner—R/W** Default = 1b. This bit unconditionally goes to a 0b when the configured bit in the CONFIGFLAG register makes a 0b-to-1b transition. This bit unconditionally goes to 1b whenever the configured bit is 0. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port.
12	**Port Power (PP)—R/W.** The function of this bit depends on the value of the port power control (PPC) field in the HCSPARAMS register. Since PPC = 1, the USS2000 has port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (i.e., PP equals a 0), the port is nonfunctional and will not report attaches, detaches, etc. When an overcurrent condition is detected on a powered port, the PP bit in each affected port will be transitioned by the host controller from a 1 to 0 (removing power from the port).
11:10	**Line Status—R.** These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to a 1. The encoding of the bits are: **Bits — [11:10] USB State Interpretation** 00b — SE0 not low-speed device, perform EHCI reset 10b — J-state not low-speed device, perform EHCI reset 01b — K-state low-speed device, release ownership of port 11b — Undefined not low-speed device, perform EHCI reset This value of this field is undefined if port power is 0.

13 EHCI Operational Registers (continued)

Table 83. PORTSC—Port Status and Control (continued)

Bit	Description
9	**Reserved.** This bit is reserved for future use, and will return a value of 0 when read.
8	**Port Reset—R/W**. 1 = port is in reset. 0 = port is not in reset. Default = 0. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note that when software writes this bit to a 1, it must also write a 0 to the port enable bit. Note that when software writes a 0 to this bit there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g., set the port enable bit to a 1). The host controller will terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a 1 to a 0. The HCHalted bit in the USBSTS register should be a 0 before software attempts to use this bit. The host controller may hold port reset asserted to a 1 when the HCHalted bit is a 1. This field is 0 if port power is 0.
7	**Suspend—R/W.** 1 = port in suspend state. 0 = port not in suspend state. Default = 0. Port enabled bit and suspend bit of this register define the port states as follows: **Bits [Port Enabled, Suspend]** — **Port State** 0X — Disable. 10 — Enable. 11 — Suspend. When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of 0 to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a 0 when: ■ Software sets the force port resume bit to a 0 (from a 1). ■ Software sets the port reset bit to a 1 (from a 0). If host software sets this bit to a 1 when the port is not enabled (i.e., port enabled bit is a 0), the results are undefined. This field is 0 if port power is 0.

13 EHCI Operational Registers (continued)

Table 83. PORTSC—Port Status and Control (continued)

Bit	Description
6	**Force Port Resume—R/W.** 1 = resume detected/driven on port. 0 = no resume (K-state) detected/driven on port. Default = 0. This functionality defined for manipulating this bit depends on the value of the suspend bit. For example, if the port is not suspended (suspend and enabled bits are a 1) and software transitions this bit to a 1, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The host controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the port change detect bit in the USBSTS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the port change detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed K) is driven on the port as long as this bit remains a 1. Software must appropriately time the resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle. The host controller will complete this transition within 2 ms of software setting this bit to a 0. This field is 0 if port power is 0.
5	**Overcurrent Change—R/WC.** Default = 0. 1 = this bit gets set to a 1 when there is a change to overcurrent active. Software clears this bit by writing a 1 to this bit position.
4	**Overcurrent Active—R.** Default = 0. 1 = this port currently has an overcurrent condition. 0 = this port does not have an overcurrent condition. This bit will automatically transition from a 1 to a 0 when the overcurrent condition is removed.
3	**Port Enable/Disable Change—R/WC.** 1 = port enabled/disabled status has changed. 0 = no change. Default = 0. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (see Chapter 11 of the USB Specification for the definition of a port error). Software clears this bit by writing a 1 to it. This field is 0 if port power is 0.
2	**Port Enabled/Disabled—R/W.** 1 = enable. 0 = disable. Default = 0. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this field. The host controller will only set this bit to a 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled (0b), downstream propagation of data is blocked on this port, except for reset. This field is 0 if port power is 0.

13 EHCI Operational Registers (continued)

Table 83. PORTSC—Port Status and Control (continued)

Bit	Description
1	**Connect Status Change—R/WC.** 1 = change in current connect status. 0 = no change. Default = 0. Indicates a change has occurred in the port's current connect status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, if the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting an already set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. This field is 0 if port power is 0.
0	**Current Connect Status—R.** 1 = device is present on port. 0 = no device is present. Default = 0. This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit (bit 1) to be set. This field is 0 if port power is 0.

14 Connection Instructions

Figure 4 shows a typical connection of the USS2000 to provide four USB ports and full legacy support to a PCI-based system. For each of the following sections, refer to Figure 4 for guidance.

14.1 PCI Connection Instructions

The USS2000 interfaces directly with any 32-bit, 33 MHz PCI bus simply by connecting all PCI related signals directly to the signals on the host motherboard or card edge of an expansion card. The PCI signaling level for all PCI signals of the USS2000 is selected by connecting the VIO signal to the signaling voltage on the motherboard or VIO pin on the card edge of the expansion card. The VIO pin will select the PCI signaling level as indicated in Table 84. A 5 V reference voltage is not required for the USS2000 to be 5 V compatible.

Table 84. PCI Signaling Levels

VIO Pin Input Voltage	USS2000 PCI Signaling Level (All PCI Signals)
4.75 V—5.25 V	5 V signaling
3.0 V—3.6 V	3.3 V signaling

14.2 USB Connection Instructions

The USS2000 host controller is designed to use an external switchable power regulator to supply downstream USB port power controlled by the USS2000. The power regulator interface has been designed to interface directly with commonly used USB power regulators with very little additional circuitry. The PRTPWR[0, 1, 2, 3] output signal is used as the switch for the power regulator. The PRTPWR[0, 1, 2, 3] signal must be bootstrapped with a pull-up or pull-down resistor to select the appropriate power switch polarity. Bootstrapping with a pull-up resistor will select an active-low power switch while bootstrapping with a pull-down will select an active-high power switch. Figure 5 depicts a typical board connection for both power regulator enable polarities.

The PWRFLT[0, 1, 2, 3]N can be connected directly to an active-low power fault regulator output to inform the USS2000 of a USB port overcurrent condition.

DPLS[0, 1, 2, 3] and DMNS[0, 1, 2, 3] are related to the integrated USB transceiver and are connected directly to the USB port connector. Figure 6 shows complete detail of the USS2000 connection to USB.

14 Connection Instructions (continued)

14.3 Test Mode Connections

The input test pins (TEST [3:0]) provide the USS2000 user with various options and test modes. These pins are decoded to select interrupt sharing; PCI signaling; and NAND tree test. These pins may be directly connected to VDD or ground as needed. If a system designer wishes to implement NAND tree test mode; it is recommended that pull-down resistors be used at pins TEST3 and TEST1. This will allow an in-circuit tester to drive them high; activating NAND tree test mode. It is also recommended that all NAND tree pins have corresponding PWB traces that can be probed by the in-circuit tester.

Table 85. Test Mode Decode

TEST [3:0]	Description
0XX0	**Share Interrupt A.** (Optional for PCI bus). All controllers share interrupt pin INTAN. Configuration reads of interrupt pin register (3Dh) return 01h.
0XX1	**Multiple Interrupt Pins.** (Optional for PCI Bus). ■ OHCI controller functions 0 and 1 share interrupt pin INTAN. Configuration reads of interrupt pin register (3Dh) return 01h. ■ OHCI controller functions 2 and 3 share interrupt pin INTBN. Configuration reads of interrupt pin register (3Dh) return 02h. ■ EHCI controller function 4 uses interrupt pin INTCN. Configuration reads of interrupt pin register (3Dh) return 03h.
00xx	**PCI Bus Signaling.** PCI bus signaling/slew rate is used. Signal level is determined by voltage (5.0 V or 3.3 V) applied to the VIO pin.
101x	**NAND Test.**

14 Connection Instructions (continued)

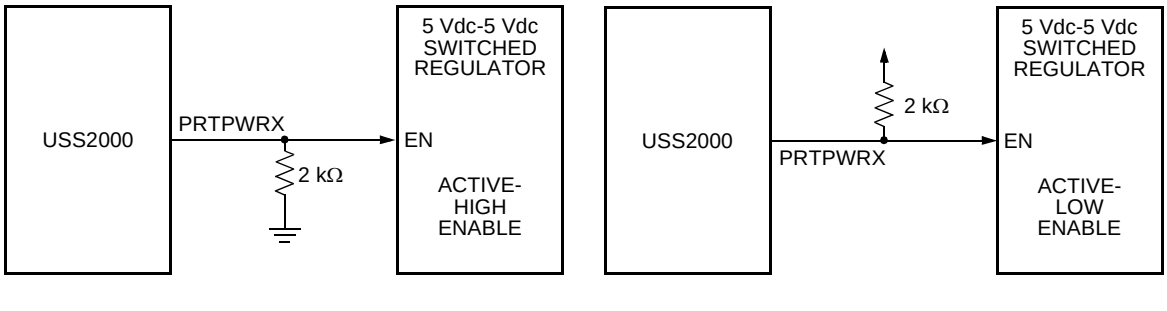

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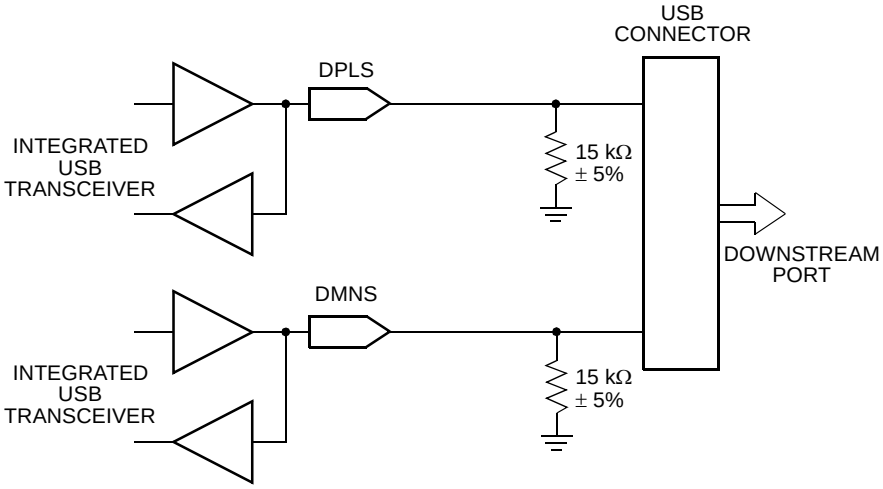
Figure 5. Typical Board Connection for Both Power Regulator Enable Polarities



5-9289 (F)a

Figure 6. USB Transceiver Connection

15 Power Connection Recommendations

The USS2000 is a 3.3 V device. Therefore, all VDD inputs must be connected to an appropriate 3.3 V source. VDDU provides all transceiver power and must be connected to a 3.3 V source. It is recommended that the system designer undertake special board routing and filtering of VDDU and VDDS to isolate these power inputs from noise induced by other components.

16 Crystal Selection Considerations

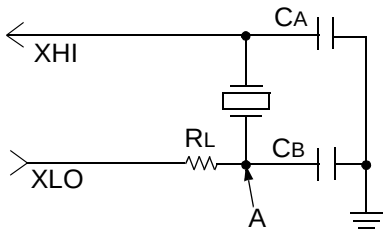
The USS2000 is designed to use an external 30 MHz crystal connected between the XHI and XLO terminals to provide the reference for an internal oscillator circuit. It is recommended that an oscillator with a nominal 100 ppm or less frequency tolerance be used.

The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ±100 ppm.

16.1 Load Capacitance

The frequency of oscillation is dependent upon the load capacitance specified for the crystal, in parallel resonant mode crystal circuits. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also capacitances from the USS2000 board traces and capacitances of the other USS2000 connected components. The values for load capacitors (C_A and C_B) should be calculated using this formula:

$C_A = C_B = (C_L - C_{stray}) \times 2$



Where:
C_L = load capacitance specified by the crystal manufacturer.

C_{stray} = capacitance of the board and the USS2000, typically 2 pF—3 pF.

R_L = load resistance; nominal value is 470 Ω; the best value to be used can be determined by customer testing.

Figure 7. Crystal Circuitry

16.2 Adjustment to Crystal Loading

The resistor (R_L) in Figure 7 is recommended for fine-tuning the crystal circuit. The nominal value for this resistor is approximately 470 Ω. A more precise value for this resistor is dependent on the specific crystal used. Please refer to the crystal manufacturer's data sheet and application notes to determine an appropriate value for R_L. A more precise value for this resistor can be obtained by placing different values of R_L on a production board and using an oscilloscope to view the resultant clock waveform at node A for each resistor value. The desired waveform should have the following characteristics: the waveform should be sinusoidal, with an amplitude as large as possible, but not greater than 3.3 V.

16.3 Crystal/Board Layout

The layout of the crystal circuit is important for obtaining the correct frequency and minimizing noise introduced into the PLL. The crystal, resistor R_L and two load capacitors (C_A + C_B) should be considered as a unit during layout. They should be placed as close as possible to one another, while minimizing the loop area created by the combination of the three components. Minimizing the loop area minimizes the effect of the resonant current that flows in this resonant circuit. This layout unit (crystal, resistor R_L, and load capacitors) should then be placed as close as possible to the XHI and XLO terminals to minimize trace lengths. Vias should not be used to route the XHI and XLO signals.

17 Power Management Interface

An advanced power management capabilities interface compliant with *PCI Bus Power Management Interface Specification* Revision 1.1 has been incorporated into each of the USS2000 controllers. This interface allows the USS2000 to be placed in various power management states offering a variety of power savings for a host system.

Table 86 highlights the USS2000 support for power management states and features supported for each of the power management states. The USS2000 has the ability to internally gate off the CLK, disable the USB transceivers, and assert USB resume signaling asynchronously (without active CLK) in response to upstream USB resume being detected. The USS2000 will assert PMEN and retain chip context in accordance with the rules defined in the *PCI Bus Power Management Interface Specification* Revision 1.1.

Table 86. USS2000 Support for Power Management States

Power Management State	State Required/ Optional	Clk Active Internally	USB Transceiver Active	Async Resume Logic Active	PMEN Assert Enabled	Chip Context Maintained	Comments
D0	Required	X	X	—	X	X	Fully awake backwards-compatible state. All logic in full-power mode.
D1	Optional	X	X	—	X	X	Fully awake state with PCI bus master capabilities turned off by host. All logic in full-power mode because of low latency returning to D0 state.
D2	Optional	—	—	X*	X	X	USB sleep state with PCI bus master capabilities turned off by host. PCI clocks may be turned off by the system.
$D3_{hot}$	Required	—	—	X*	X	—	Deep USB sleep state with PCI bus master capabilities turned off by host. PCI clocks may be turned off by the system.
$D3_{cold}$	Not Supported	—	—	—	—	—	—

* Asynchronous resume logic active only when PME_Enable register bit is active.

A wake-up event (power management event) detected by a USB host controller is considered either an upstream resume detected or a connect status change (device disconnecting/connecting) detected. Any of these events detected by the USS2000 while the power management event is enabled will cause PMEN to be issued.

This power management feature is considered an extension of the PCI specification and is always present. The PCI configuration space status register, bit 4, will read as logic 1 (capabilities list present).

PMEN is an open collector output allowing wire-OR of several PMEN signals.

18 NAND Tree Mode

The USS2000 can be placed in a NAND tree mode of operation for board-level production testing. The NAND tree is designed to allow board-level contact testing of inputs and bidirectional pins of the USS2000.

To activate the NAND tree in the USS2000, force pins 64 and 62 (TEST3 and TEST1) to a logic high and force pin 63 (TEST2) to a logic low. Pin 61 (TEST0) may be high or low. No clocks are required. When this is performed, the NAND tree will be active and follow the order of the map presented in Table 87. Figure 8 shows the NAND tree logic structure.

Table 87. NAND Tree

Order Assignment	Pin Number	Ball Number	Pin/Ball Name	Order Assignment	Pin Number	Ball Number	Pin/Ball Name
1 (Start)	83	G12	XLO	40	11	D2	AD20
2	75	J11	SMIN	41	12	E4	AD19
3	76	H10	PRTPWR0	42	13	E1	AD18
4	77	J9	PWRFLT0N	43	16	F2	AD17
5	78	H9	PRTPWR1	44	17	E3	AD16
6	79	H12	PWRFLT1N	45	18	F1	C/BEN2
7	89	E9	DPLS0	46	19	F3	FRAMEN
8	90	D9	DMNS0	47	22	G3	IRDYN
9	91	E10	DPLS1	48	23	H3	TRDYN
10	92	E11	DMNS1	49	24	G2	DEVSELN
11	95	D10	DPLS2	50	25	H1	STOPN
12	96	D11	DMNS2	51	26	H4	PERRN
13	97	C12	DPLS3	52	29	J4	SERRN
14	98	C11	DMNS3	53	30	J1	PAR
15	101	A12	PRTPWR2	54	31	J3	C/BEN1
16	102	B11	PWRFLT2N	55	32	K3	AD15
17	103	A11	PRTPWR3	56	35	K1	AD14
18	104	A10	PWRFLT3N	57	36	K2	AD13
19	105	C9	INTAN	58	37	L1	AD12
20	108	B9	INTBN	59	38	M1	AD11
21	109	A8	INTCN	60	41	L3	AD10
22	111	B8	RSTN	61	42	M3	AD9
23	113	A7	CLK	62	43	L4	AD8
24	115	C7	GNTN	63	44	M4	C/BEN0
25	116	A6	REQN	64	47	M5	AD7
26	119	B6	PMEN	65	48	K5	AD6
27	120	C5	AD31	66	49	L6	AD5
28	121	A5	AD30	67	50	M6	AD4
29	122	B5	AD29	68	53	M7	AD3
30	125	A3	AD28	69	54	K7	AD2
31	126	C4	AD27	70	55	L7	AD1
32	127	A2	AD26	71	56	M8	AD0
33	128	A1	AD25	72	67	M12	MIRQ12I
34	3	C2	AD24	73	68	L12	KIRQI
35	4	B3	C/BEN3	74	69	K12	A20I
36	5	C1	IDSEL	75	70	K10	A20MN
37	6	C3	AD23	76	71	K11	IRQ1
38	7	D3	AD22	Output Pin	72	J10	IRQ12
39	10	D4	AD21	—	—	—	—

18 NAND Tree Mode (continued)

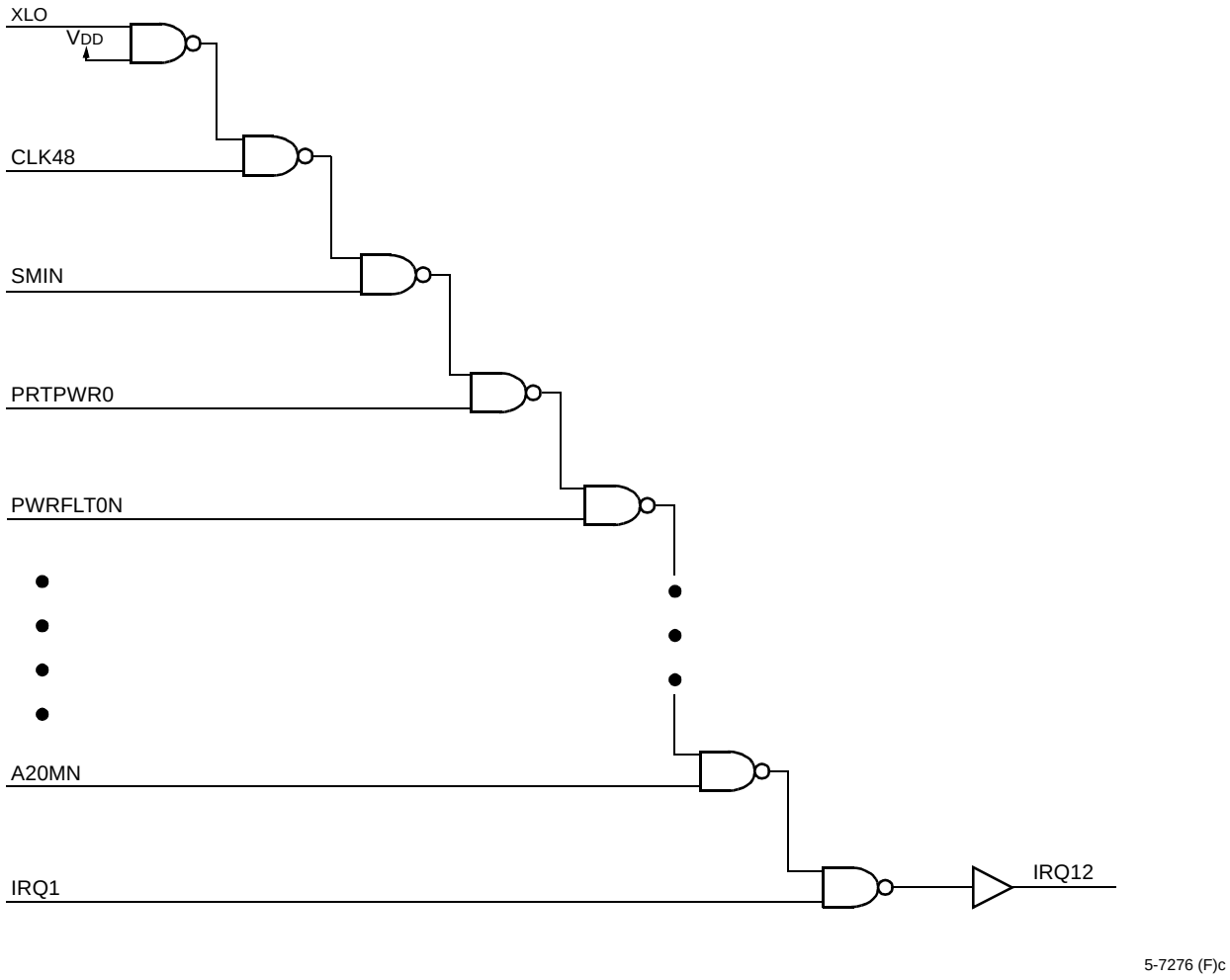


Figure 8. NAND Tree Logic Structure

19 Absolute Maximum Ratings

Table 88. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature Range	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	125	°C
Voltage on Any Pin with Respect to Ground	—	VSS – 0.3	5.5	V
VDD	—	3.0	3.6	V
VDDU	—	3.135	3.465	V
VIO (3.3 V operation)	—	3.0	3.6	V
VIO (5 V operation)	—	4.75	5.25	V

20 Electrical Characteristics

Table 89. Power Dissipation

Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation	P_D	TBD	840	TBD	mW

20.1 PCI Electrical Characteristics

20.1.1 PCI Timing Specifications

The clock waveform must be delivered to each PCI component in the system. In the case of expansion boards, compliance with the clock specification is measured at the expansion board component, not at the connector slot. Figure 9 shows the clock waveform and required measurement points for both 5 V and 3.3 V signaling environments. Table 90 summarizes the clock specifications.

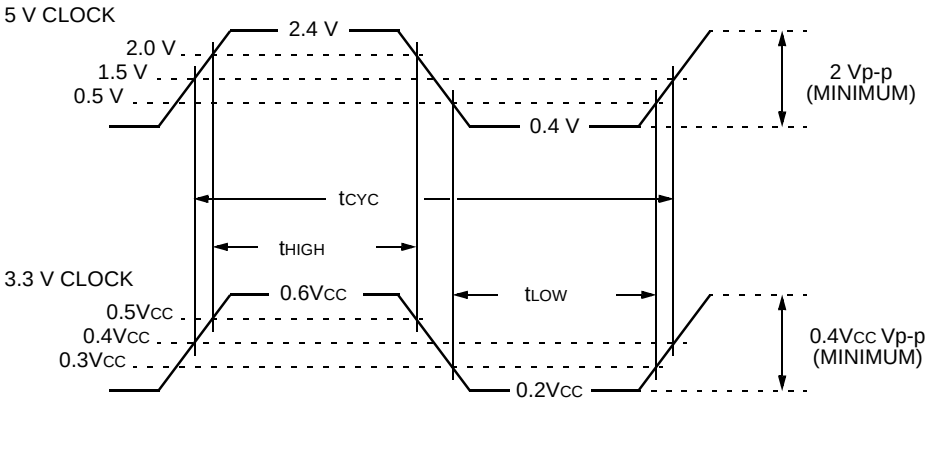


Figure 9. Clock Waveforms

20.1.2 PCI Timing Parameters

Table 90. Clock and Reset Specifications

Symbol	Parameter	Min	Max	Unit
t_{CYC}	CLK Cycle Time[1]	30	∞	ns
t_{HIGH}	CLK High Time	11	—	ns
t_{LOW}	CLK Low Time	11	—	ns
—	CLK Slew Rate[2]	1	4	V/ns
—	RSTN Slew Rate[3]	50	—	mV/ns

1. In general, all PCI components must work with any clock frequency between nominal dc and 33 MHz. Device operational parameters at frequencies under 16 MHz may be guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system, as long as the clock edges remain clean (monotonic), and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state. A variance on this specification is allowed for components designed for use on the system motherboard only. These components may operate at any single fixed frequency up to 33 MHz and may enforce a policy of no frequency changes.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform, as shown in Figure 9.
3. The minimum RSTN slew rate applies only to the rising (deassertion) edge of the reset signal and ensures that system noise cannot render an otherwise monotonic signal to appear to bounce in the switching range.

20 Electrical Characteristics (continued)

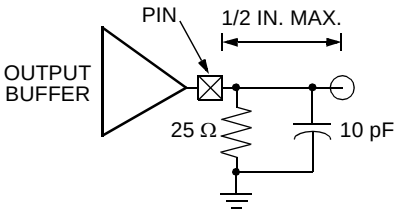
Table 91. 5 V and 3.3 V PCI Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{VAL}	CLK to Signal Valid Delay—Bused Signals[1, 2, 3]	2	11	ns
$t_{VAL(ptp)}$	CLK to Signal Valid Delay—Point to Point[1, 2, 3]	2	12	ns
t_{ON}	Float to Active Delay[1, 7]	2	—	ns
t_{OFF}	Active to Float Delay[1, 7]	—	28	ns
t_{SU}	Input Setup Time to CLK—Bused Signals[3, 4]	7	—	ns
$t_{SU(ptp)}$	Input Setup Time to CLK—Point to Point[3, 4]	10, 12	—	ns
t_{H}	Input Hold Time from CLK[4]	0	—	ns
t_{RST}	Reset Active Time After Power Stable[5]	1	—	ns
$t_{RST-CLK}$	Reset Active Time After CLK Stable[5]	100	—	ns
$t_{RST-OFF}$	Reset Active to Output Float Delay[5, 6, 7]	—	40	ns
t_{RRSU}	REQN to RSTN Setup Time	$10 \times t_{CYC}$	—	ns
t_{RRH}	RSTN to REQN Hold Time	0	50	ns

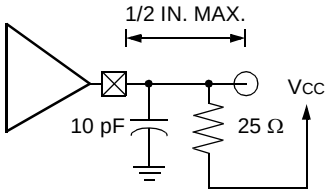
1. See the timing measurement conditions in Figure 4-8 of PCI Specification Revision 2.1.
2. For parts compliant to the 5 V signaling environment:
   Minimum times are evaluated with 0 pF equivalent load; maximum times are evaluated with 50 pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications. Note that faster buffers may exhibit some ring back when attached to a 50 pF lump load, which should be of no consequence as long as the output buffers are in full compliance with slew rate and V/I curve specifications.

   For parts compliant to the 3.3 V signaling environment:
   Minimum times are evaluated with same load used for slew rate measurement (see PCI Specification, Rev. 2.1s); maximum times are evaluated with the following load circuits, for high-going and low-going edges, respectively.

T_{VAL}(MAX) RISING EDGE



T_{VAL}(MAX) FALLING EDGE



3. REQN and GNTN are point-to-point signals and have different output valid delay and input setup times than bused signals. GNTN has a setup time of 10 ns; REQN has a setup time of 12 ns. All other signals are bused.
4. See the timing measurement conditions in Figure 4-8 of PCI Specification Revision 2.1.
5. RSTN is asserted and deasserted asynchronously with respect to CLK.
6. All output drivers must be asynchronously floated when RSTN is active.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

20 Electrical Characteristics (continued)

20.2 USB Electrical Characteristics

Table 92. Input Levels for High Speed

Parameter	Symbol	Condition	Min	Max	Unit
High-speed Squelch Detection Threshold (differential signal amplitude)	V_{HSSQ}	See Section 7.1.7.2 of the *USB2.0 Specification*. (Specification refers to differential signal amplitude.)	100	150	mV
High-speed Disconnect Detection Threshold (differential signal amplitude)	V_{HSDSC}	See Section 7.1.7.2 of the *USB2.0 Specification*. (Specification refers to differential signal amplitude.)	525	625	mV
High-speed Differential Input Signaling Levels	—	See Section 7.1.7.2 of the *USB2.0 Specification*. Specified by eye pattern templates.	—	—	—
High-speed Data Signaling Common-mode Voltage Range (guideline for receiver)	V_{HSCM}	See Section 7.1.4.2 of the *USB2.0 Specification*.	–50	500	mV

Table 93. Output Levels for High Speed

Parameter	Symbol	Condition	Min	Max	Unit
High-speed Idle Level	V_{HSOI}	See Section 7.1.7.2 of the *USB2.0 Specification*.	–10	10	mV
High-speed Data Signaling High	V_{HSOH}	See Section 7.1.7.2 of the *USB2.0 Specification*.	360	440	mV
High-speed Data Signaling Low	V_{HSOL}	See Section 7.1.7.2 of the *USB2.0 Specification*.	–10	10	mV
Chirp J Level (differential voltage)	V_{CHIRPJ}	See Section 7.1.7.2 of the *USB2.0 Specification*.	700	1100	mV
Chirp K Level (differential voltage)	V_{CHIRPK}	See section 7.1.7.2 of the *USB2.0 Specification*.	–900	–500	mV

20 Electrical Characteristics (continued)

Table 94. High-Speed Source Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Rise Time (10%—90%)	THSR	See Section 7.1.2 of *USB2.0 Specification*.	500	—	ps
Fall Time (10%—90%)	THSF	See Section 7.1.2 of *USB2.0 Specification*.	500	—	ps
Driver Waveform Requirements	—	See specified by eye pattern templates in Section 7.1.2 of *USB2.0 Specification*.	—	—	—
Driver Output Resistance (which also serves as high-speed termination)	ZHSDRV	See Section 7.1.1.1 of *USB2.0 Specification*.	40.5	49.5	Ω
Clock Timings					
High-speed Data Rate	THSDRAT	See Section 7.1.11 of *USB2.0 Specification*.	479.760	480.240	Mbits/s
Microframe Interval	THSFRAM	See Section 7.1.12 of *USB2.0 Specification*.	124.9375	125.0625	µs
Consecutive Microframe Interval Difference	THSRFI	See Section 7.1.12 of *USB2.0 Specification*.	—	4 high-speed bit times	—
High-Speed Data Timings					
Data Source Jitter	—	Source and receiver jitter specified by the eye pattern templates in Section 7.1.2.2 of the *USB2.0 Specification*.			
Receiver Jitter Tolerance					

Table 95. Full-Speed Source USB Electrical Characteristics

Parameter	Symbol	Conditions[1, 2, 3]	Min	Max	Unit
Driver Characteristics					
Transition Time[4, 5]:					
Rise Time	tR	CL = 50 pF	4	20	ns
Fall Time	tF	CL = 50 pF	4	20	ns
Rise/Fall Time Matching	tRFM	(TR/TF)	90	110	%
Output Signal Crossover Voltage	VCRS	—	1.3	2.0	V
Driver Output Resistance	ZDRV	Steady-State Drive	28	43	Ω
Data Source Timings					
Full-speed Data Rate	tDRATE	Average Bit Rate (12 Mbits/s ± 0.25%)	11.97	12.03	Mbits/s
Frame Interval	tFRAME	1.0 ms ± 0.05%	0.9995	1.0005	ms

1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
3. Full-speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.
4. Measured from 10% to 90% of the data signal.
5. The rising and falling edges should be smoothly transitioning (monotonic).

20 Electrical Characteristics (continued)

Table 96. Low-Speed Source USB Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Driver Characteristics					
Transition Time[1, 2]:					
Rise Time	t_R	CL = 50 pF	75	—	ns
		CL = 350 pF	—	300	ns
Fall Time	t_F	CL = 50 pF	75	—	ns
		CL = 350 pF	—	300	ns
Rise/Fall Time Matching	t_{RFM}	(TR/TF)	80	120	%
Output Signal Crossover Voltage	V_{CRS}	—	1.3	2.0	V
Data Source Timings					
Low-speed Data Rate	t_{DRATE}	Average Bit Rate (1.5 Mbits/s ± 1.5%)	1.4775	1.5225	Mbits/s

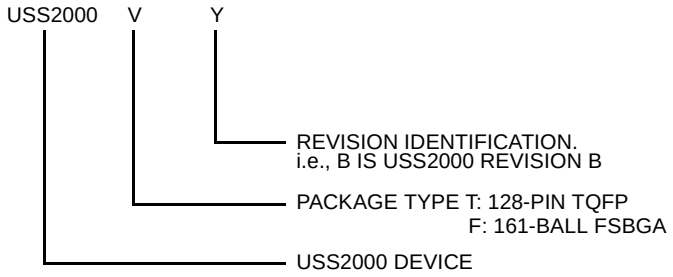
1. Measured from 10% to 90% of the data signal.
2. The rising and falling edges should be smoothly transitioning (monotonic).

20.3 CLK30 Clock Specification

A 30 MHz crystal (±100 PPM or better) must be connected across the XHI/XLO input pins.

21 Physical Markings

Each USS2000 will be physically marked as follows:

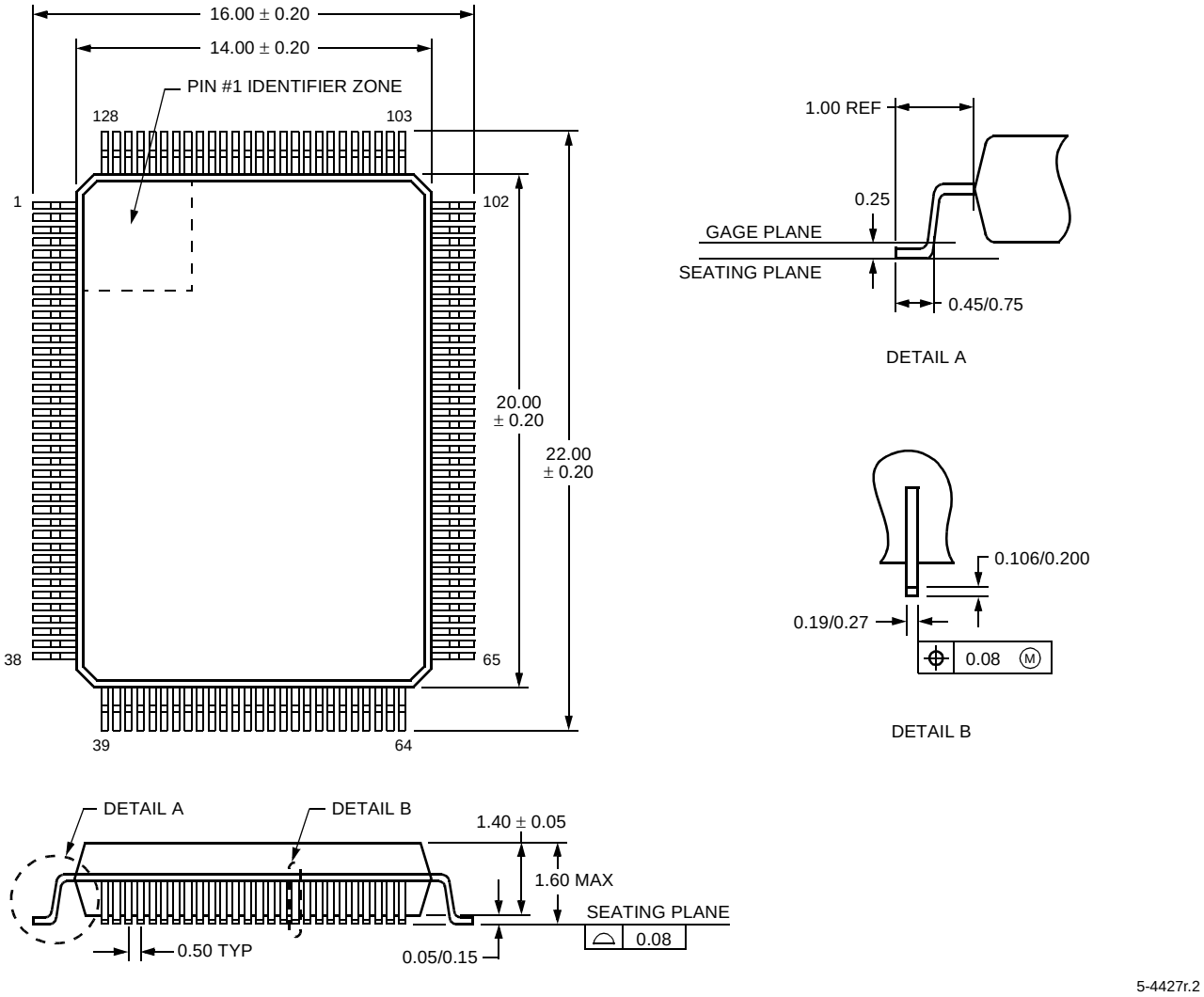


5-8116a

22 Outline Diagram

22.1 128-Pin TQFP

Dimensions are in millimeters.

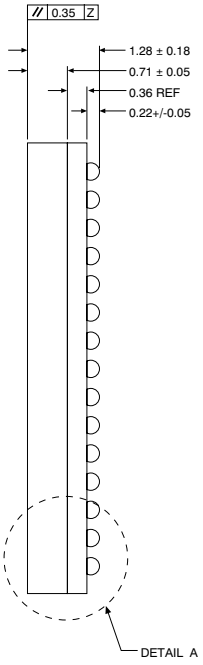


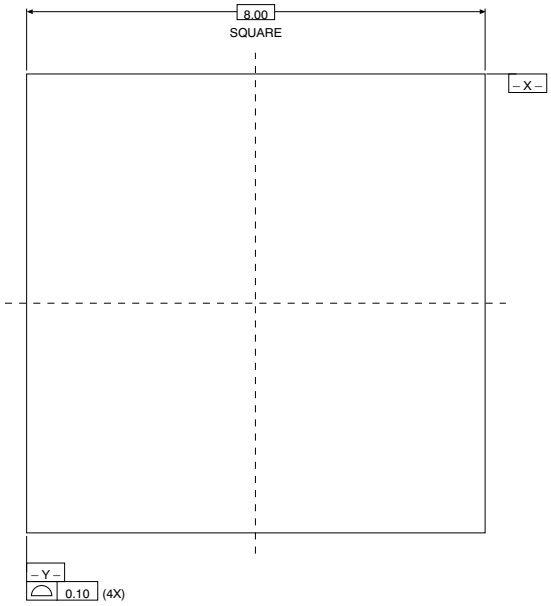
5-4427r.2

22 Outline Diagram (continued)

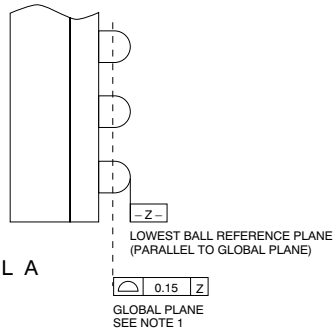
22.2 161-Ball FSBGA

Dimensions are in millimeters.

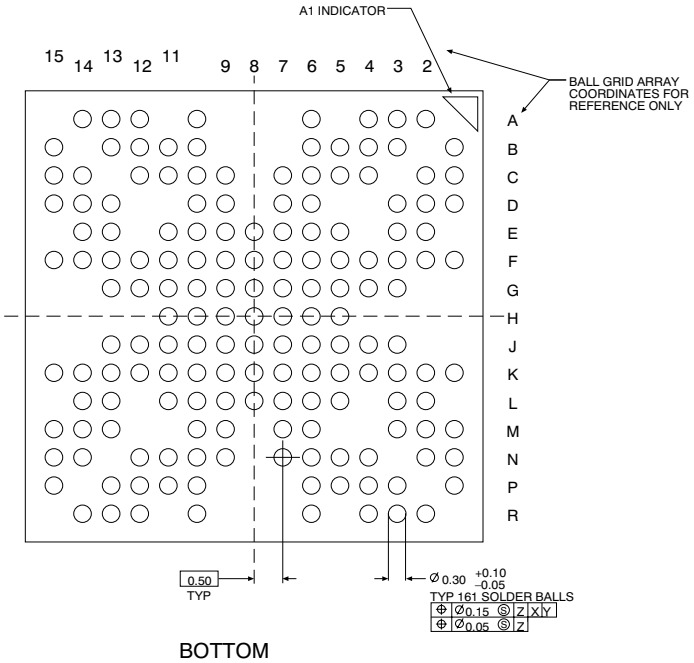




TOP



DETAIL A



BOTTOM

23 Ordering Information

Device	Device Code	Package	Comcode
USS2000	L-USS2000V5-T128-DB*†	128-Pin TQFP	700085014
	L-USS2000V5-F161-DB*†	161-Ball FSBGA	700077381

* Lead-free: No intentional addition of lead, and less than 1000 ppm.

† Agere Systems lead-free devices are fully compliant with the Restriction of Hazardous Substances (RoHS) directive that restricts the content of six hazardous substances in electronic equipment in the European Union. Beginning July 1, 2006, electronic equipment sold in the European Union must be manufactured in accordance with the standards set by the RoHS directive.

24 Applicable Documents and Specifications

- *PCI Local Bus Specification* Revision 2.2., December 18, 1998. PCI Special Interest Group.
- *Universal Serial Bus Specification* Revision 2.0., April 27, 2000. *Compaq*®/Digital Equipment Corporation/*IBM PC Company*®/*Intel*®/*Microsoft*/*NEC*®/*Nortel Networks*®.
- *OpenHCI Open Host Controller Interface Specification for USB* Release 1.0a., February 29, 2000. *Compaq*/*Microsoft*/*National Semiconductor*®.
- *PCI Bus Power Management Interface Specification* Revision 1.1., May 4, 1998. PCI Special Interest Group.
- *Enhanced Host Controller Interface Specification for Universal Serial Bus* Revision 1.0., November 10, 2000. Intel Corporation.

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