54F/74F676

16-Bit Serial/Parallel-In, Serial-Out Shift Register

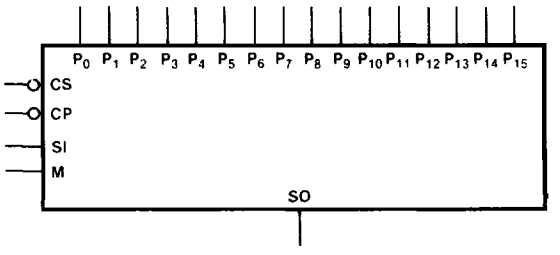
Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0-P_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

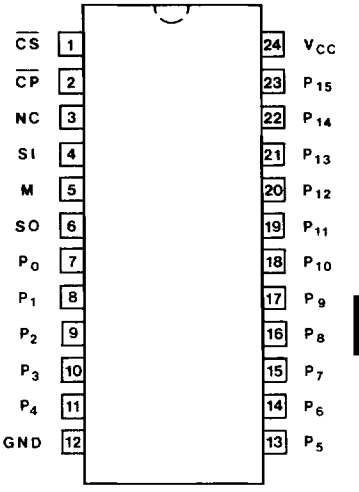
- **16-Bit Parallel-to-Serial Conversion**
- **16-Bit Serial-In, Serial-Out**
- **Chip Select Control**
- **Slim 24 Lead 300 mil Package**

Ordering Code: See Section 5

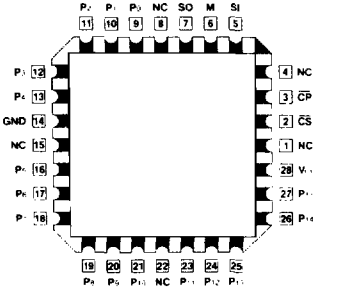
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
P_0-P_{15}	Parallel Data Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active LOW)	0.5/0.375
M	Mode Select Input	0.5/0.375
SI	Serial Data Input	0.5/0.375
SO	Serial Output	25/12.5

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load—data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load—data present on P_0-P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

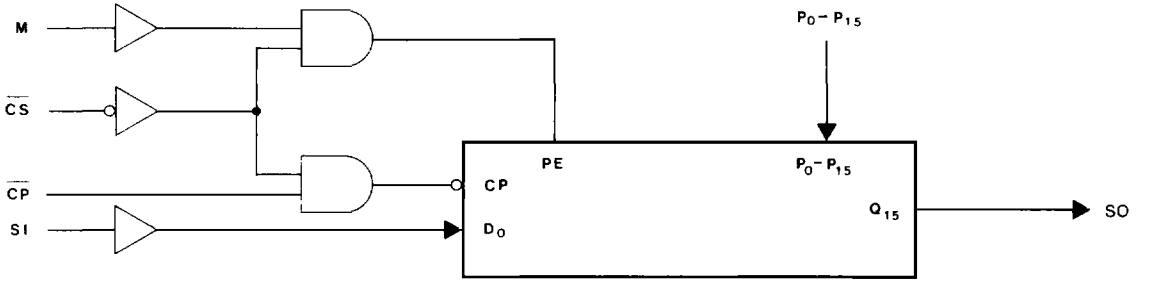
To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial Load
L	H	↓	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = HIGH-to-LOW Transition

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		48	72	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100 110	75	90	MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to SO	4.5 9.0 11.0 5.0 9.0 12.5	4.5 17.0 5.0 14.5	4.5 12.0 5.0 13.5	ns	3-1 3-8

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AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI to $\overline{CP}$	4.0 4.0	4.0 4.0	4.0 4.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI to $\overline{CP}$	4.0 4.0	4.0 4.0	4.0 4.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{CP}$	3.0 3.0	3.0 3.0	3.0 3.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{CP}$	4.0 4.0	4.0 4.0	4.0 4.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW M to $\overline{CP}$	8.0 8.0	8.0 8.0	8.0 8.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW M to $\overline{CP}$	2.0 2.0	2.0 2.0	2.0 2.0		
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{CP}$	10.0	12.0	10.0	ns	3-6
$t_h(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{CP}$	10.0	10.0	10.0		
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	4.0 6.0	5.0 8.0	4.0 6.0	ns	3-8