T-46-23-12

HYBRID
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8Kx 8 SRAM

MSM88U-15/20

Issue 3.0 : November 1988

8, 192 x 8 CMOS High Speed Static RAM

Features

- Fast Access Times of 150/200 nS
- Full CMOS Design-6 transistor cell
- Standard 28 pin DIL/32 pin LCC footprint
- Completely Static Operation
- Equal Access and Cycle Times
- Standby Current of 1μA
- Battery back-up capability
- Directly TTL compatible
- Common data inputs & outputs
- May be Screened in accordance with BS9400 and MIL-STD-883C (suffix MB)

Pin Definitions

Block Diagram

Package Details Dimensions in mm (inches)

32 Pin LCC ('W' Package)

28 Pin DIL ('S' Package)

Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-0.3V to +7	V
Power Dissipation	P_t	2	W
Storage Temperature	T_{stg}	-65 to +150	°C

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{cc}	4.5	5.0	5.5	V
Input High Voltage	V_{ih}	2.2	-	6.0	V
Input Low Voltage	V_{il}	-0.3	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_{ai}	-40	-	85	°C (88CI)
	T_{am}	-55	-	125	°C (88CM,MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{li}	V_{in}=Gnd to V_{cc}	-	-	5.0	uA
Output Leakage Current	I_{lo}	$\overline{CS1}=V_{ih}$ or CS2=V_{il} or $\overline{OE}=V_{ih}$, $V_{I/O}$=Gnd to V_{cc}	-	-	5.0	uA
Operating Power Supply Current	I_{cc}	$\overline{CS1}=V_{il}$,CS2=V_{ih},$I_{I/O}$=0mA,	-	50	70	mA
Standby Power Supply Current	I_{cc1}	$\overline{CS1}\geq V_{ih}$or CS2$\leq V_{il}$	-	2.0	10	mA
	I_{cc2}	$\overline{CS1}\geq$Vcc-0.2V or CS2$\leq$0.2V $V_{in}\geq$Vcc-0.2V or $V_{in}\leq$0.2V	-	1	100	uA
Output Voltage	V_{ol}	I_{ol}=2.1mA	-	-	0.4	V
	V_{oh}	I_{oh}=-1.0mA	2.4	-	-	V

Note 1: Typical values are at V_{cc}=5.0V,T_a=25°C and specified loading.

Capacitance (V_{cc}=5V±10%,T_a=25°C)

Parameter	*Symbol*	*Test Condition*	*LCC max*	*DIL max*	*Unit*
Input Capacitance:	C_{in}	V_{in}=0V	6	10	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	8	12	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

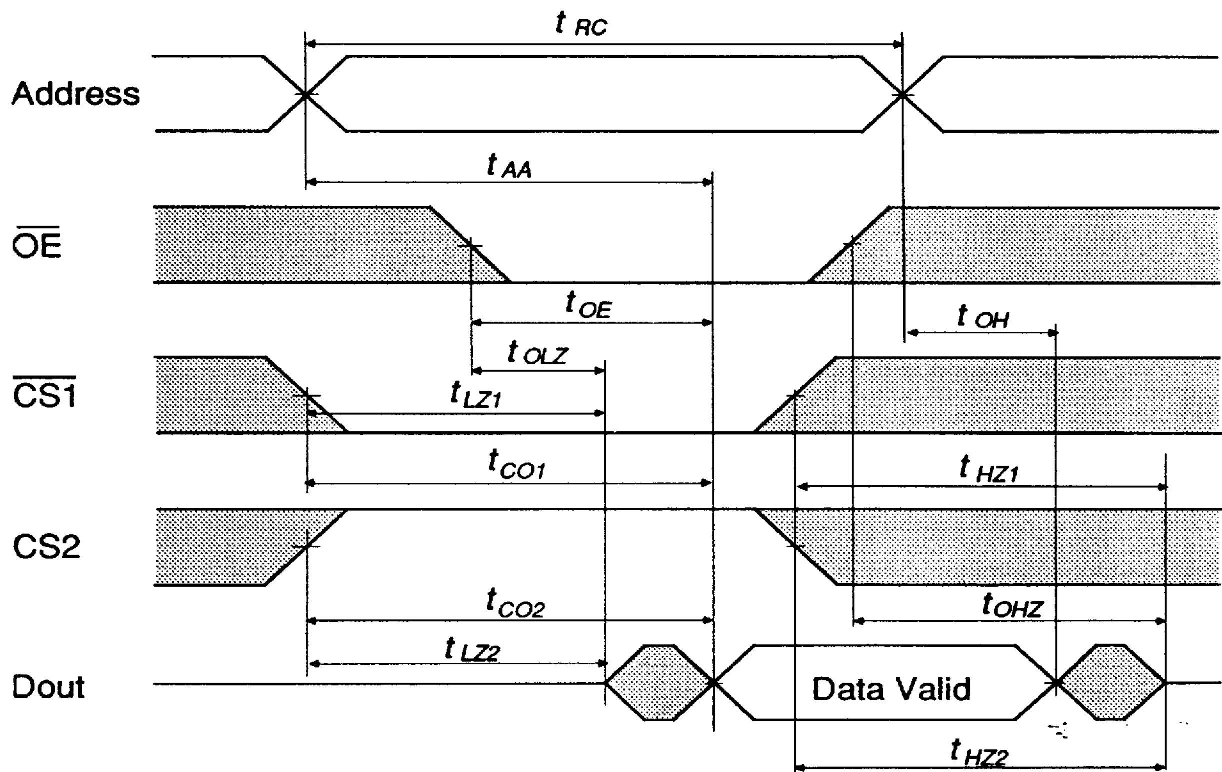
* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF (including scope & jig)
* Vcc=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	Unit
Read Cycle Time	t_{RC}	150	-	200	-	ns
Address Access Time	t_{AA}	-	150	-	200	ns
Chip Selection to Output ($\overline{CS1}$)	t_{CO1}	-	150	-	200	ns
Chip Selection to Output (CS2)	t_{CO2}	-	150	-	200	ns
Output Enable to Output Valid	t_{OE}	-	70	-	100	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns
Chip Selection to Output in Low Z($\overline{CS1}$)	t_{LZ1}	10	-	10	-	ns
Chip Selection to Output in Low Z(CS2)	t_{LZ2}	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	10	-	ns
Chip Deselection to Output in High Z($\overline{CS1}$)	t_{HZ1}	0	50	0	70	ns
Chip Deselection to Output in High Z(CS2)	t_{HZ2}	0	50	0	70	ns
Output Disable to Output in High Z	t_{OHZ}	0	50	0	70	ns

Read Cycle Timing Waveform (1,2,3)



Notes:

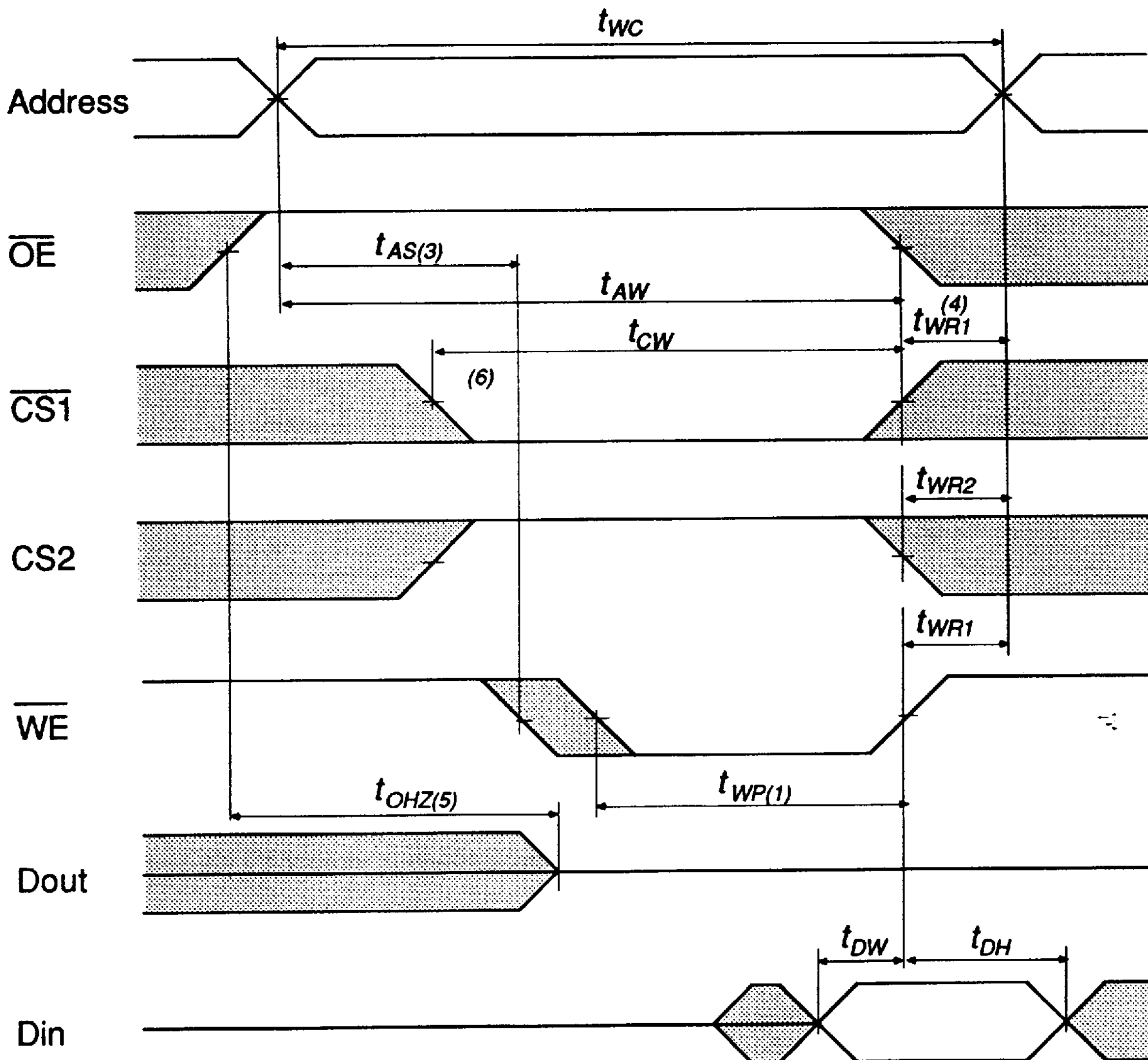
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for Read Cycle.

T-46-23-12

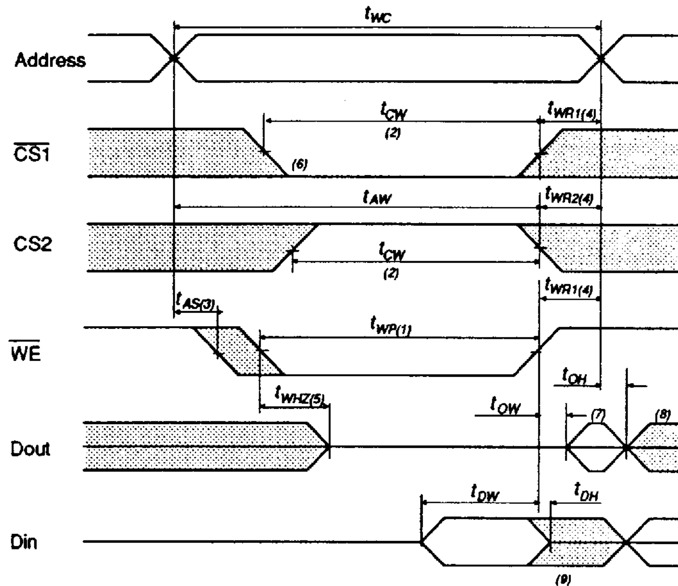
Write Cycle

Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	Unit
Write Cycle Time	t_{WC}	150	-	200	-	ns
Chip Selection to End of Write	t_{CW}	100	-	120	-	ns
Address Valid to End of Write	t_{AW}	100	-	120	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	90	-	110	-	ns
Write Recovery Time ($\overline{WE}$, $\overline{CS1}$)	t_{WR1}	10	-	10	-	ns
Write Recovery Time (CS2)	t_{WR2}	10	-	10	-	ns
Write to Output in High Z	t_{WHZ}	0	50	0	70	ns
Data to Write Time Overlap	t_{DW}	60	-	80	-	ns
Data Hold from Write Time	t_{DH}	10	-	10	-	ns
Output Active from End of Write	t_{OW}	5	-	10	-	ns

Write Cycle No.1 Timing Waveform: $\overline{OE}$ Clock



Write Cycle No.2 Timing Waveform: $\overline{OE}$ Low Fix



Notes:

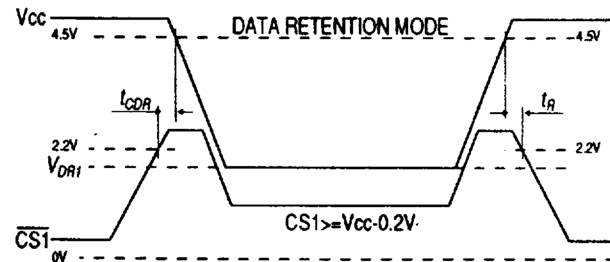
1. A write occurs during the overlap (t_{wp}) of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{wp} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{as} is measured from the address valid to the beginning of write.
4. t_{wr} is measured from the end of write to the address change. t_{wr1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high. t_{wr2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therefore input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is in the same phase as written data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

Low V_{cc} Data Retention Characteristics - LP Version Only (t_a=-55 to +125°C)

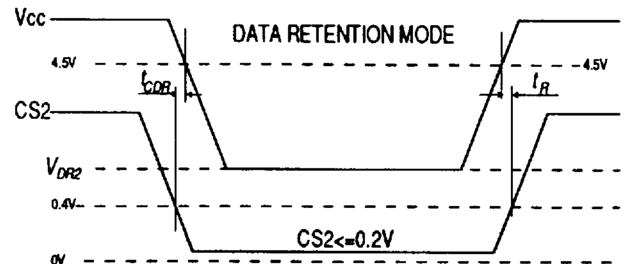
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Data Retention Voltage	V_{DR1}	$\overline{CS1}$,CS2≥V_{cc}-0.2V or CS2≤0.2V	2.0	-	5.5	V
	V_{DR2}	CS2≤0.2V	2.0	-	5.5	V
Data Retention Current	I_{CCDR1}	Vcc=3.0V,$\overline{CS1}$≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V	-	-	100*	µA
	I_{CCDR2}	Vcc=3.0V,CS2≤0.2V				
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}**	-	-	ns

* For t_a=25°C,$I_{CCDR1,2}$=0.2µA, t_a=60°C,$I_{CCDR1,2}$=1.0µA
** t_{RC}=Read Cycle Time

Waveform 1 ($\overline{CS1}$ Controlled)



Waveform 2 (CS2 Controlled)



Military Screening Procedure

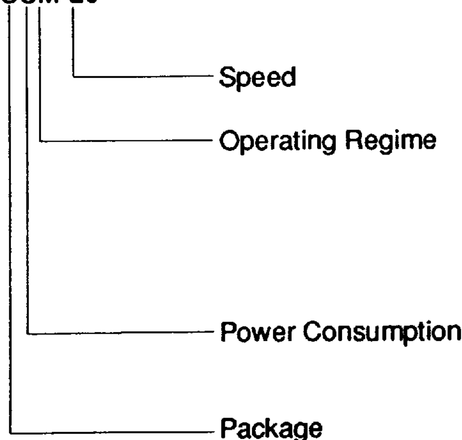
Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW		
SCREEN	*TEST METHOD (Per MIL 883C)*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ 150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to 150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at Ta=+25°C	100%
Burn-in	Method 1015,Condition D,Ta=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable(PDA)	Calculated at post-burn-in at Ta=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Note: For BS Approved part, ask for the Detail Specification relevant to this part.

Ordering Information

MSM88SUM-20



Operating Regime:
Blank = Commercial
I = Industrial
M = Military
MB = BS or MIL-STD-883
BS = Full BS approved part

Power Consumption:
Blank = Commercial
U = Ultra Low Power part

Package:
W = Leadless Chip-Carrier
S = Side-Brazed DIL

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